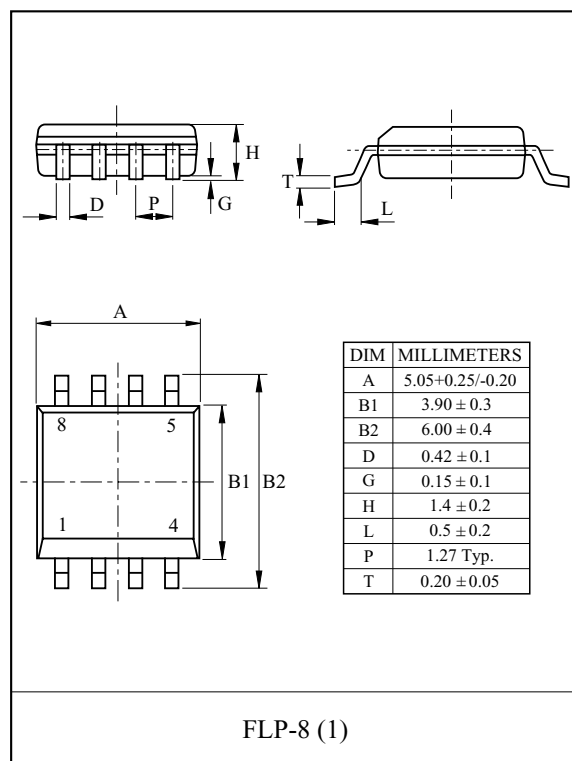


General Description

Switching regulator and DC-DC Converter applications.
It s mainly suitable for power management in PC,
portable equipment and battery powered systems.

FEATURES

- N-Channel
 - : $V_{DSS}=30V$, $I_D=5.5A$.
 - : $R_{DS(ON)}=40m\ \Omega$ (Max.) @ $V_{GS}=10V$
 - : $R_{DS(ON)}=50m\ \Omega$ (Max.) @ $V_{GS}=4.5V$
- P-Channel
 - : $V_{DSS}=-30V$, $I_D=-4.5A$.
 - : $R_{DS(ON)}=55m\ \Omega$ (Max.) @ $V_{GS}=-10V$
 - : $R_{DS(ON)}=85m\ \Omega$ (Max.) @ $V_{GS}=-4.5V$
- Super High Dense Cell Design.
- Reliable and rugged.

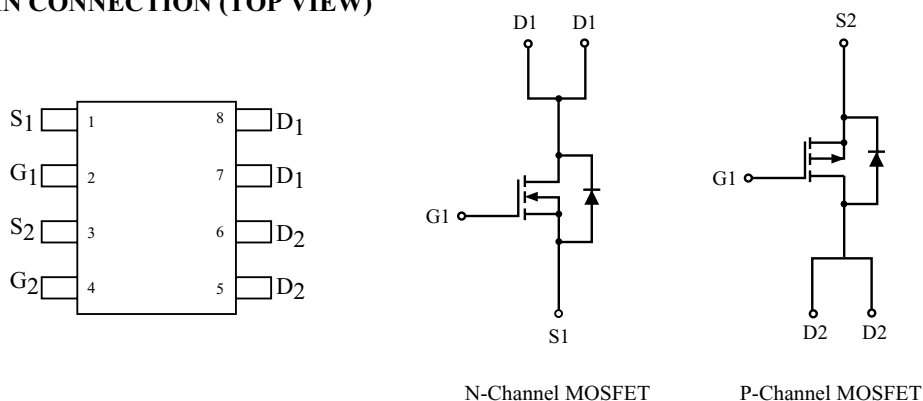


MAXIMUM RATING (Ta=25 °C)

CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D^*	5.5	-4.5	A
	Pulsed (Note1)	I_{DP}	23	-18	
Source-Drain Diode Current		I_S	1.7	-1.7	A
Drain Power Dissipation		P_D^*	2		W
Maximum Junction Temperature		T_j	150		°C
Storage Temperature Range		T_{stg}	-55 ~ 150		°C
Thermal Resistance, Junction to Ambient		R_{thJA}	62.5		°C/W

* : Surface Mounted on FR4 Board, $t \leq 10sec$.

PIN CONNECTION (TOP VIEW)



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ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	N-Ch	30	-	-	V
		I _D =-250μA, V _{GS} =0V	P-Ch	-30	-	-	
Drain Cut-off Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V	N-Ch	-	-	1	μA
		V _{DS} =-24V, V _{GS} =0V	P-Ch	-	-	-1	
Gate Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V	N-Ch	-	-	±100	nA
			P-Ch	-	-	±100	
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =250μA	N-Ch	0.8	-	1.8	V
		V _{DS} =V _{GS} , I _D =-250μA	P-Ch	-1.0	-1.5	-2.5	
Drain-Source ON Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =6A (Note 1)	N-Ch	-	28	40	m Ω
		V _{GS} =-10V, I _D =-4.9A (Note 1)	P-Ch	-	45	55	
		V _{GS} =4.5V, I _D =5.2A (Note 1)	N-Ch	-	40	50	
		V _{GS} =4.5V, I _D =-3.6A (Note 1)	P-Ch	-	75	85	
ON State Drain Current	I _{D(ON)}	V _{GS} =10V, V _{DS} =5V	N-Ch	15	-	-	A
		V _{GS} =-10V, V _{DS} =-5V	P-Ch	-12	-	-	
Forward Transconductance	g _{fs}	V _{DS} =10V, I _D =6A (Note 1)	N-Ch	6	-	-	S
		V _{DS} =-15V, I _D =-4.9A (Note 1)	P-Ch	4	-	-	
Source-Drain Diode Forward Voltage	V _{SD}	I _S =1.7A, V _{GS} =0V (Note 1)	N-Ch	-	0.77	1.2	V
		I _S =-1.7A, V _{GS} =0V (Note 1)	P-Ch	-	-0.82	-1.2	
Dynamic (Note 2)							
Total Gate Charge	Q _g	N-Ch : V _{DS} =10V, I _D =6A, V _{GS} =4.5V (Fig.1) P-Ch : V _{DS} =-15V, I _D =-4.9A, V _{GS} =-10V (Fig.3)	N-Ch	-	9.3	-	nC
Gate-Source Charge	Q _{gs}		P-Ch	-	15.6	-	
			N-Ch	-	2.5	-	
Gate-Drain Charge	Q _{gd}		P-Ch	-	2.4	-	
			N-Ch	-	3.2	-	
			P-Ch	-	3.3	-	
Turn-on Delay time	t _{d(on)}	N-Ch : V _{DD} =10V, I _D =1A, V _{GS} =4.5V, R _G =6 Ω R _L =10 Ω (Fig.2) P-Ch : V _{DD} =-15V, I _D =-1A, V _{GS} =-10V, R _L =15 Ω , R _G =6 Ω (Fig.4)	N-Ch	-	15.6	-	ns
Turn-on Rise time	t _r		P-Ch	-	13	-	
			N-Ch	-	9.7	-	
			P-Ch	-	4.7	-	
			N-Ch	-	26.3	-	
Turn-off Delay time	t _{d(off)}		P-Ch	-	47.1	-	
			N-Ch	-	26.9	-	
Turn-off Fall time	t _f		P-Ch	-	17	-	
Input Capacitance	C _{iss}	N-Ch : V _{DS} =8V, V _{GS} =0V, f=1.0MHz P-Ch : V _{DS} =-15V, V _{GS} =0V, f=1.0MHz	N-Ch	-	510	-	pF
Output Capacitance	C _{oss}		P-Ch	-	393	-	
			N-Ch	-	155	-	
Reverse transfer Capacitance	C _{rss}		P-Ch	-	116	-	
			N-Ch	-	127	-	
			P-Ch	-	45	-	

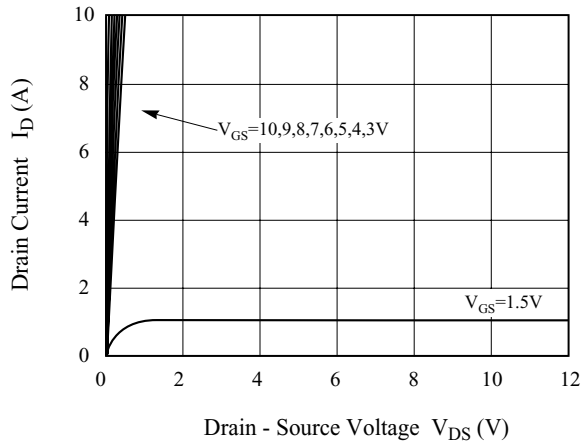
Note 1) Pulse test : Pulse width ≤300μs, Duty Cycle ≤2%.

Note 2) Guaranteed by design. Not subject to production testing.

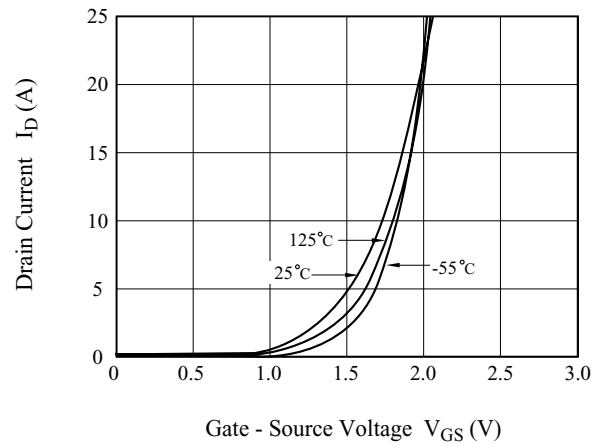
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N-Channel

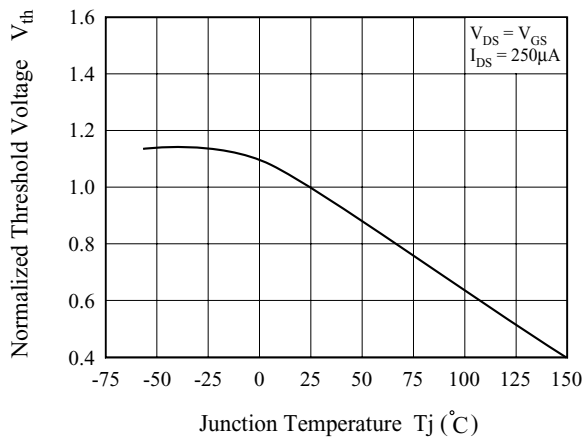
$I_D - V_{DS}$



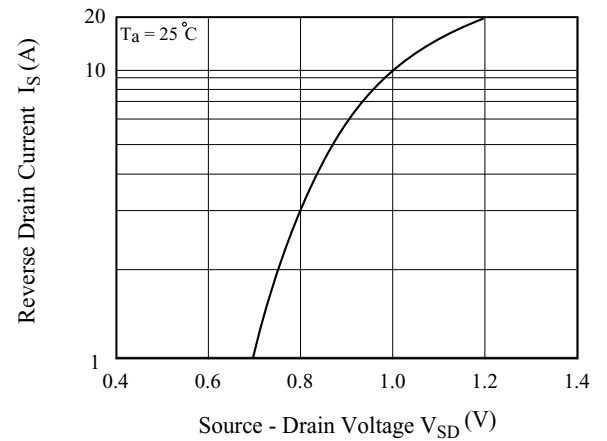
$I_D - V_{GS}$



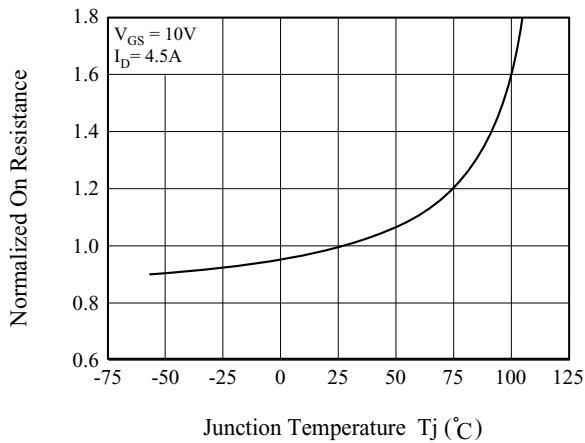
$V_{th} - T_j$



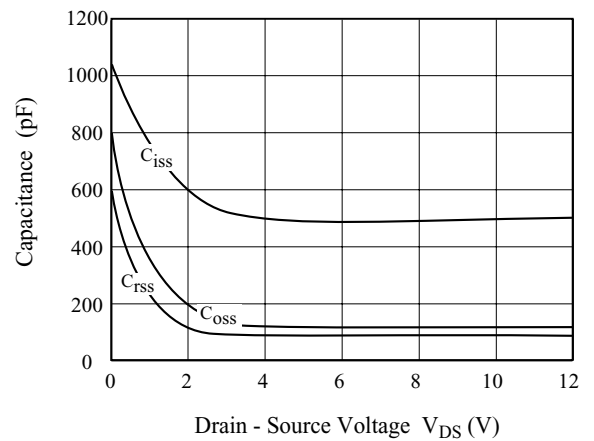
$I_S - V_{SD}$



$R_{DS(ON)} - T_j$

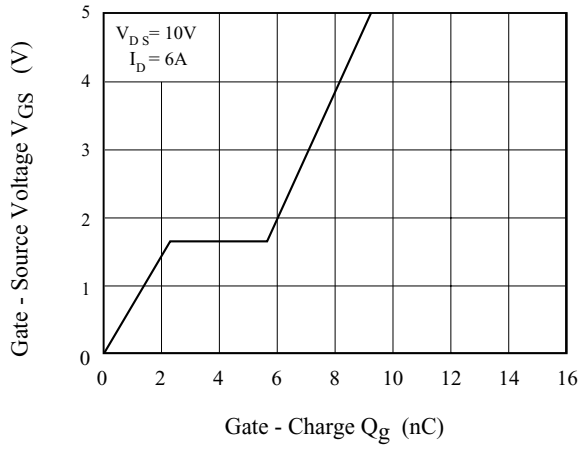


$C - V_{DS}$



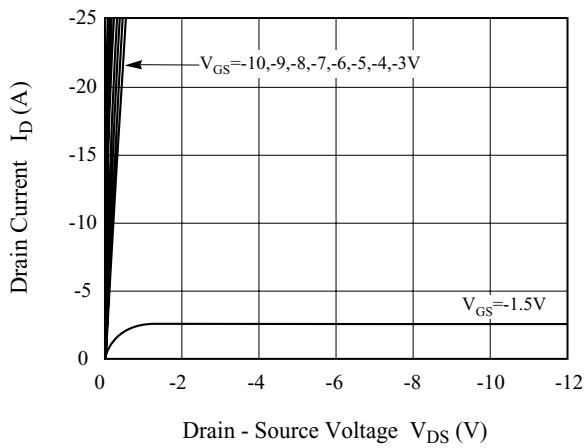
KMB5D5NP30Q

$Q_g - V_{GS}$

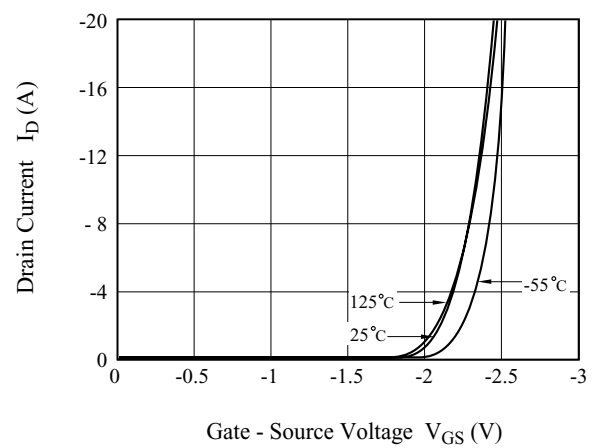


P-Channel

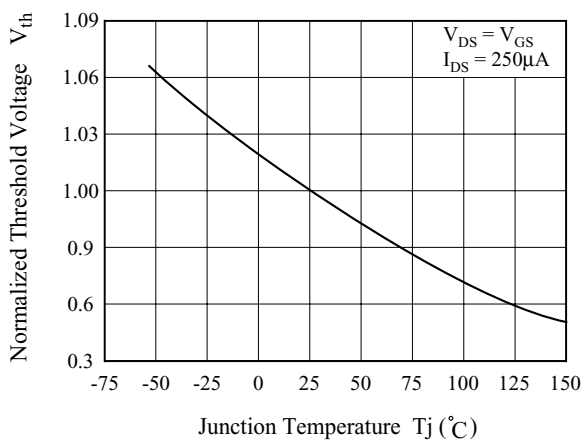
$I_D - V_{DS}$



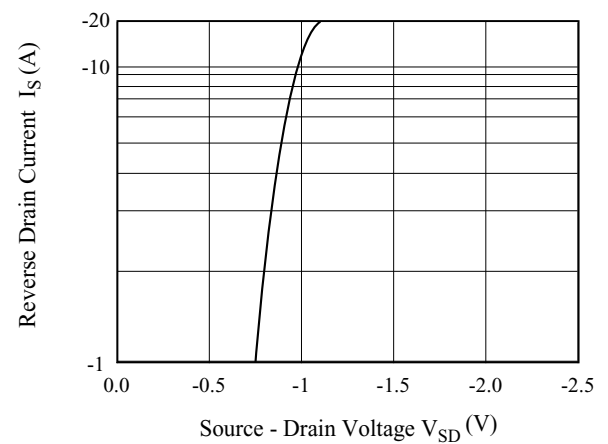
$I_D - V_{GS}$



$V_{th} - T_j$

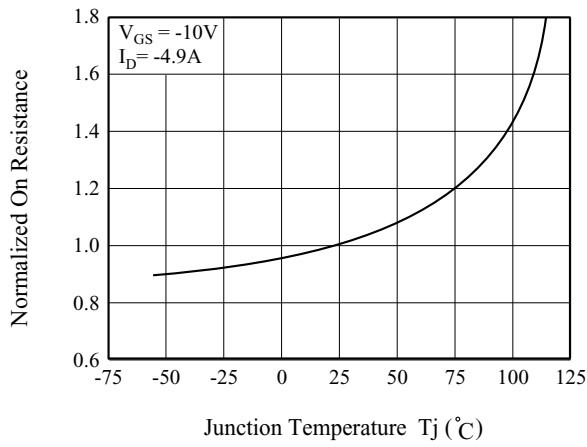


$I_S - V_{SD}$

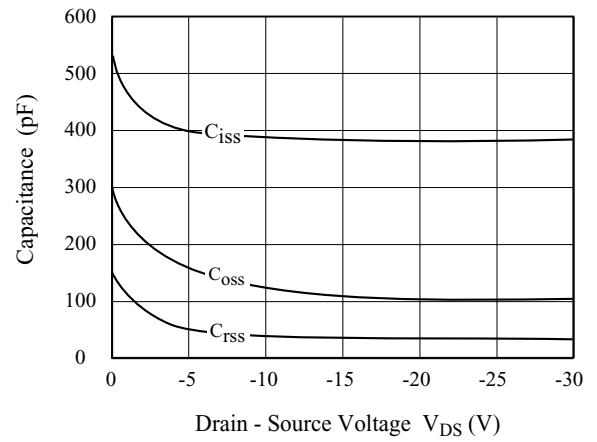


KMB5D5NP30Q

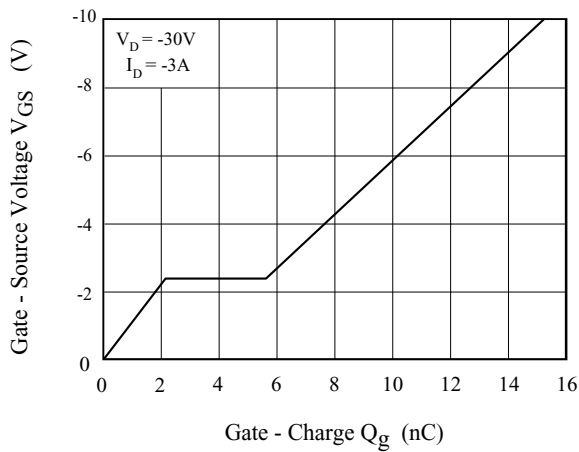
$R_{DS(ON)} - T_j$



$C - V_{DS}$



$Q_g - V_{GS}$



R_{th}

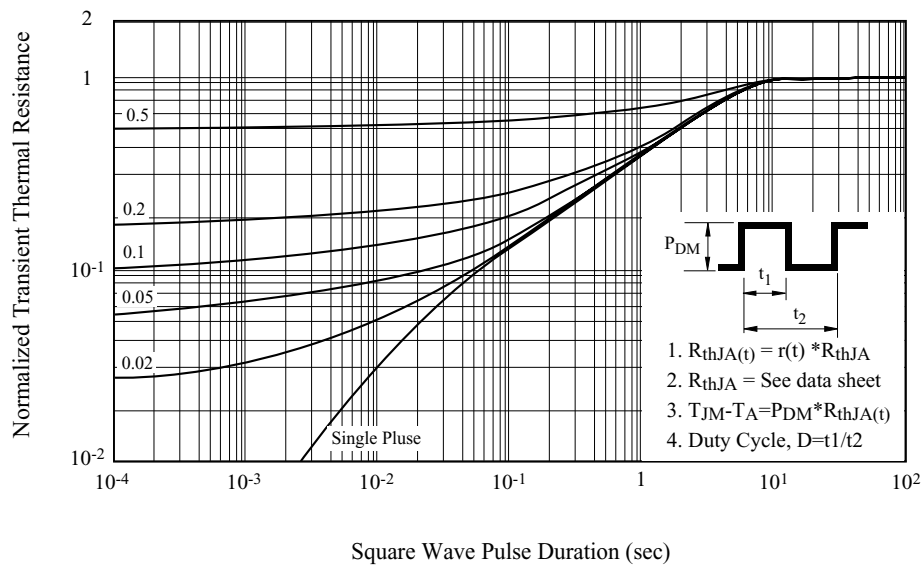


Fig. 1 Gate Charge

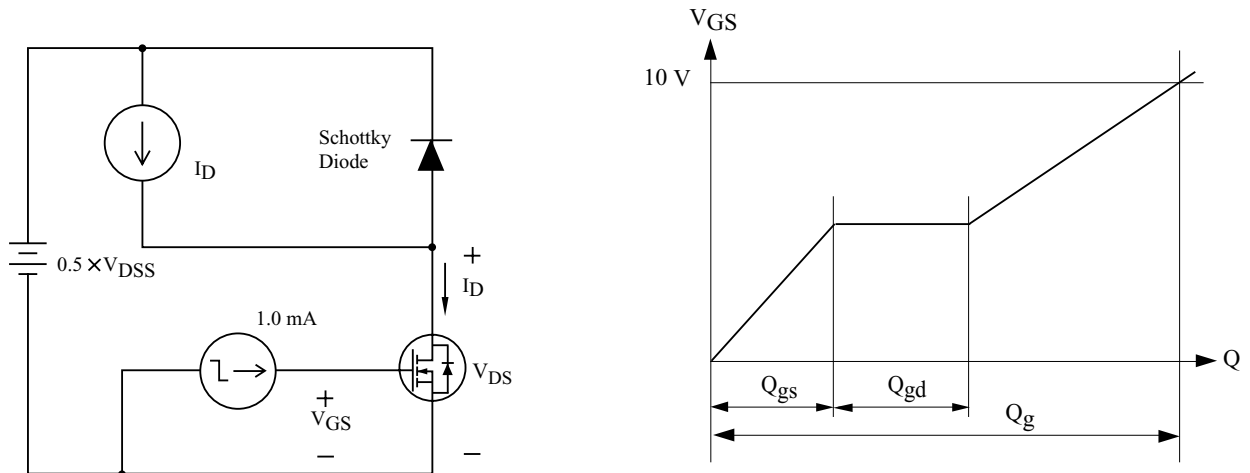


Fig. 2 Resistive Load Switching

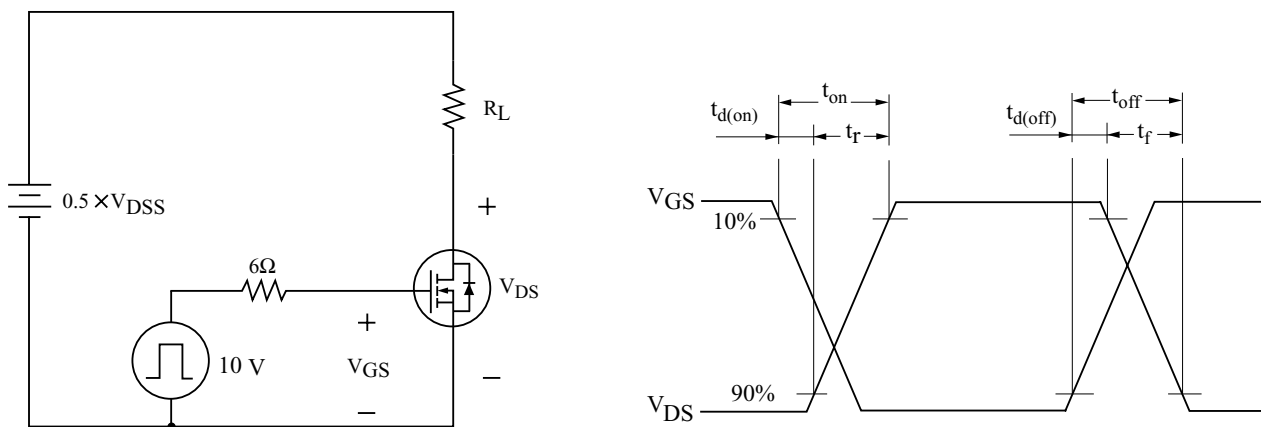


Fig. 3 Gate Charge

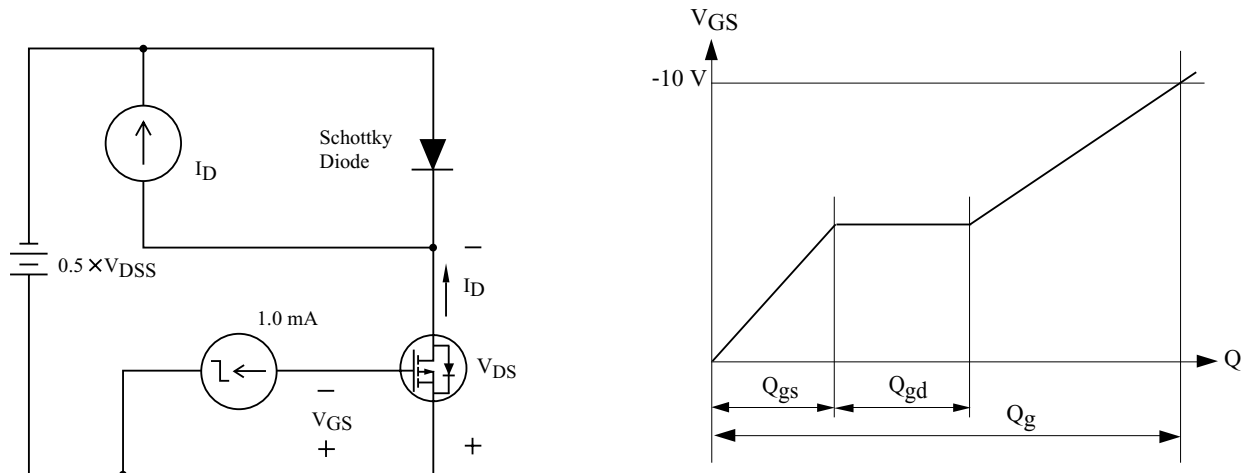


Fig. 4 Resistive Load Switching

