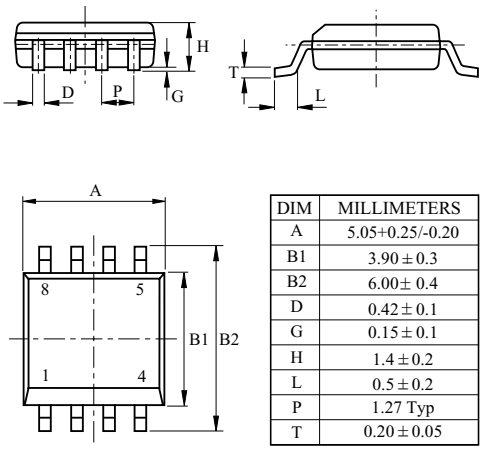
KMB5D0NP40Q

N and P-Ch Trench MOSFET

General Description

Switching regulator and DC-DC Converter applications.
It s mainly suitable for power management in PC,
portable equipment and battery powered systems.



DIM	MILLIMETERS
A	5.05+0.25/-0.20
B1	3.90 ± 0.3
B2	6.00± 0.4
D	0.42 ± 0.1
G	0.15 ± 0.1
H	1.4 ± 0.2
L	0.5 ± 0.2
P	1.27 Typ
T	0.20 ± 0.05

FLP-8

FEATURES

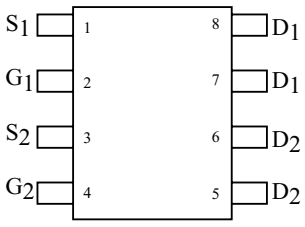
- N-Channel
  - : V_{DSS}=40V, I_D=5A.
  - : $R_{DS(ON)}$=35m Ω (Max.) @ V_{GS}=10V
  - : $R_{DS(ON)}$=62m Ω (Max.) @ V_{GS}=4.5V
- P-Channel
  - : V_{DSS}=-40V, I_D=-4A.
  - : $R_{DS(ON)}$=47m Ω (Max.) @ V_{GS}=-10V
  - : $R_{DS(ON)}$=65m Ω (Max.) @ V_{GS}=-4.5V
- Super High Dense Cell Design.
- Reliable and rugged.

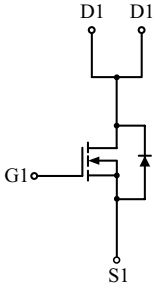
MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	40	-40	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D*	5	-4	A
	Pulsed (Note1)	I_{DP}*	20	-16	
Source-Drain Diode Current		I_S*	1.7	-1.7	A
Drain Power Dissipation		P_D*	2		W
Maximum Junction Temperature		T_j	150		℃
Storage Temperature Range		T_{stg}	-55 ~ 150		℃
Thermal Resistance, Junction to Ambient		R_{thJA}	62.5		℃/W

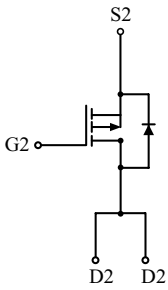
* : Surface Mounted on FR4 Board, t ≤ 10sec.

PIN CONNECTION (TOP VIEW)





N-Channel MOSFET



P-Channel MOSFET

ELECTRICAL CHARACTERISTICS (Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250㎂, V_{GS}=0V	N-Ch	40	-	-	V
		I_D=-250㎂, V_{GS}=0V	P-Ch	-40	-	-	
Drain Cut-off Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V	N-Ch	-	-	1	㎂
		V_{DS}=-32V, V_{GS}=0V	P-Ch	-	-	-1	
Gate Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	N-Ch	-	-	±100	nA
			P-Ch	-	-	±100	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D=250㎂	N-Ch	1.0	2.0	3.0	V
		V_{DS}=V_{GS}, I_D=-250㎂	P-Ch	-0.8	-1.5	-2.0	
Drain-Source ON Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.0A (Note 1)	N-Ch	-	25	35	mΩ
		V_{GS}=-10V, I_D=-4A (Note 1)	P-Ch	-	37	47	
		V_{GS}=4.5V, I_D=4A (Note 1)	N-Ch	-	45	62	
		V_{GS}=-4.5V, I_D=-3A (Note 1)	P-Ch	-	50	65	
ON State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	N-Ch	15	-	-	A
		V_{GS}=-10V, V_{DS}=-5V	P-Ch	-20	-	-	
Forward Transconductance	g_{fs}	V_{DS}=5V, I_D=5A (Note 1)	N-Ch	-	8.5	-	S
		V_{DS}=-5V, I_D=-4A (Note 1)	P-Ch	-	9.5	-	
Source-Drain Diode Forward Voltage	V_{SD}	I_S=1.7A, V_{GS}=0V (Note 1)	N-Ch	-	0.8	1.2	V
		I_S=-1.7A, V_{GS}=0V (Note 1)	P-Ch	-	-0.77	-1.2	

ELECTRICAL CHARACTERISTICS (Ta=25℃)

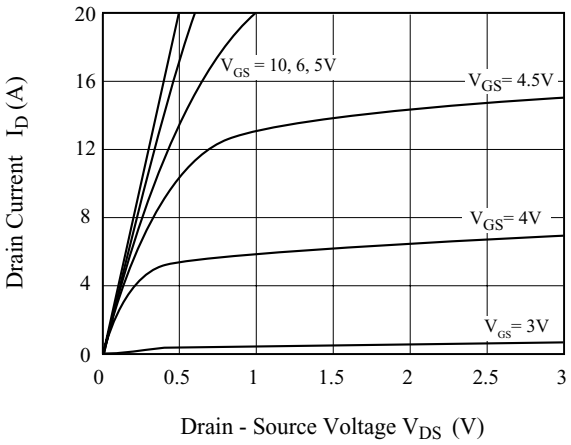
CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Dynamic (Note 2)							
Total Gate Charge	Q_g	**N-Ch** : V_{DS}=24V, I_D=5A, V_{GS}=10V (Fig.1) **P-Ch** : V_{DS}=-24V, I_D=-4A, V_{GS}=-10V (Fig.3)	N-Ch	-	15.8	18	nC
			P-Ch	-	19.9	23	
		N-Ch : V_{DS}=24V, I_D=5A, V_{GS}=4.5V (Fig.1) **P-Ch** : V_{DS}=-24V, I_D=-4A, V_{GS}=-4.5V (Fig.3)	N-Ch	-	7.7	9	
			P-Ch	-	9.8	11	
Gate-Source Charge	Q_{gs}	**N-Ch** : V_{DS}=24V, I_D=5A, V_{GS}=4.5V (Fig.1) **P-Ch** : V_{DS}=-24V, I_D=-4A, V_{GS}=-4.5V (Fig.3)	N-Ch	-	3	3.6	
			P-Ch	-	2.8	3.2	
Gate-Drain Charge	Q_{gd}		N-Ch	-	3.9	4.6	
			P-Ch	-	4.2	4.9	
Turn-on Delay time	$t_{d(on)}$	**N-Ch** : V_{DD}=15V, I_D=3A, V_{GS}=10V, R_G=4.7 Ω (Fig.2) **P-Ch** : V_{DD}=-15V, V_{GS}=-10V, R_G=4.7 Ω, I_D=-2.2A (Fig.4)	N-Ch	-	6.8	8	ns
			P-Ch	-	8.7	10	
Turn-on Rise time	t_r		N-Ch	-	8.4	9	
			P-Ch	-	19.8	23	
Turn-off Delay time	$t_{d(off)}$		N-Ch	-	16.6	18	
			P-Ch	-	63.7	75	
Turn-off Fall time	t_f		N-Ch	-	10.5	11	
			P-Ch	-	26	30	
Input Capacitance	C_{iss}	**N-Ch** : V_{DS}=10V, V_{GS}=0V, f=1.0MHz **P-Ch** : V_{DS}=-10V, V_{GS}=0V, f=1.0MHz	N-Ch	-	800	895	pF
			P-Ch	-	1090	1297	
Output Capacitance	C_{oss}		N-Ch	-	150	168	
			P-Ch	-	205	240	
Reverse transfer Capacitance	C_{rss}		N-Ch	-	98	110	
			P-Ch	-	125	145	

Note 1) Pulse test : Pulse width ≤300 μs, Duty Cycle ≤2%.

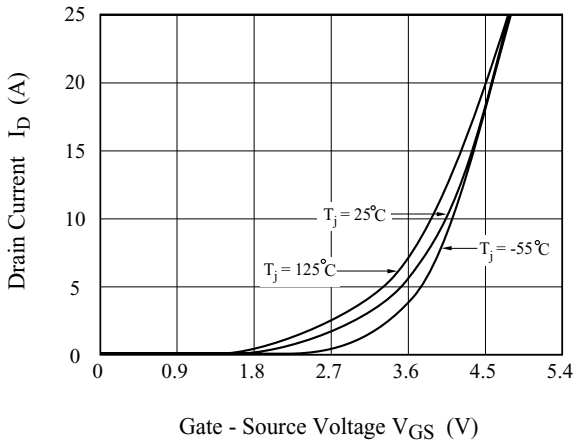
Note 2) Guaranteed by design. Not subject to production testing.

N-Channel

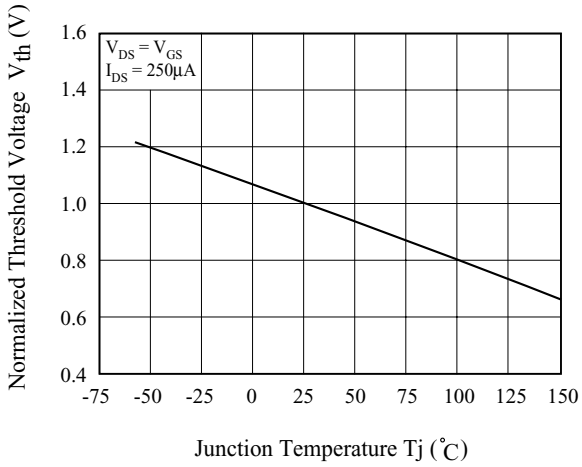
I_D - V_{DS}



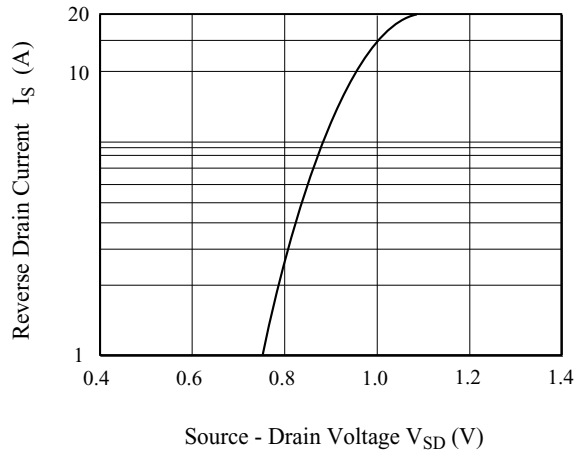
I_D - V_{GS}



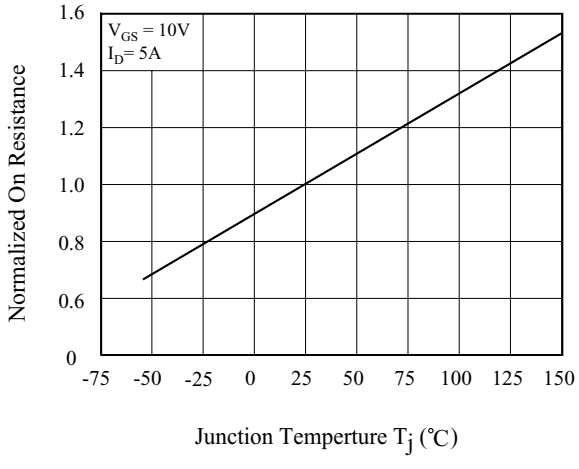
V_{th} - T_j



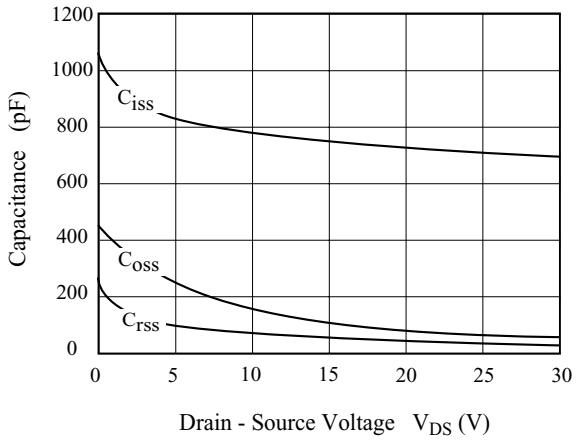
I_S - V_{SD}



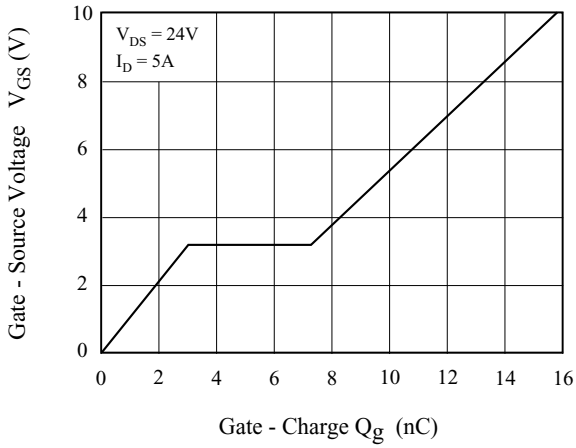
$R_{DS(ON)}$ - T_j



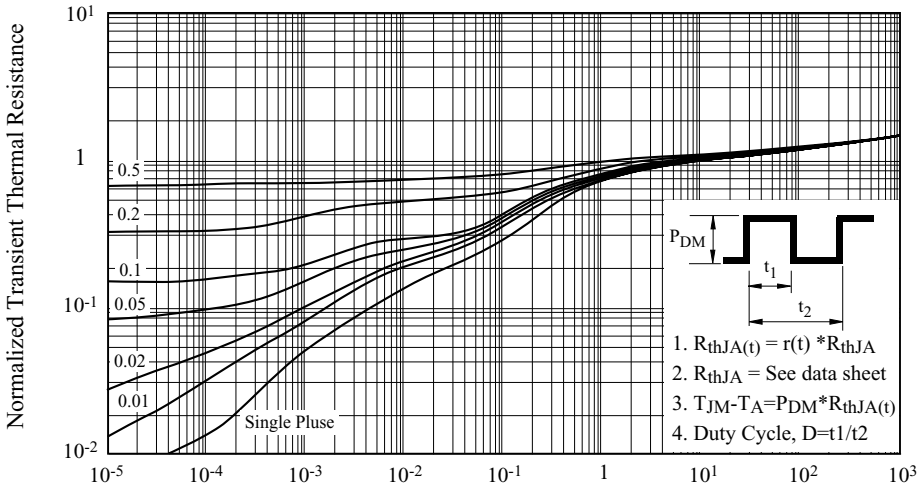
C - V_{DS}



Q_g- V_{GS}

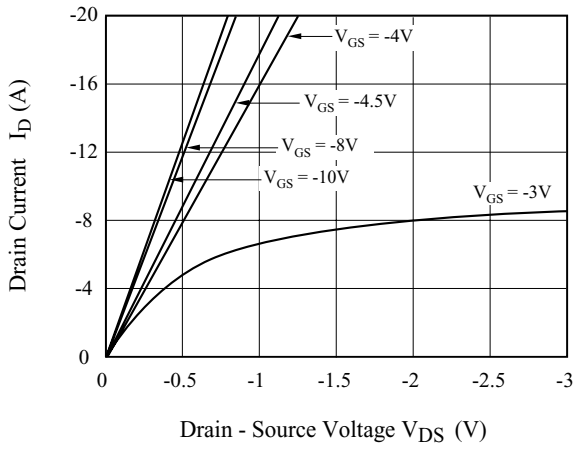

V_{DS} = 24V
I_D = 5A
Gate - Source Voltage V_{GS} (V)
Gate - Charge Q_g (nC)
0
2
4
6
8
10
12
14
16

R_{th}

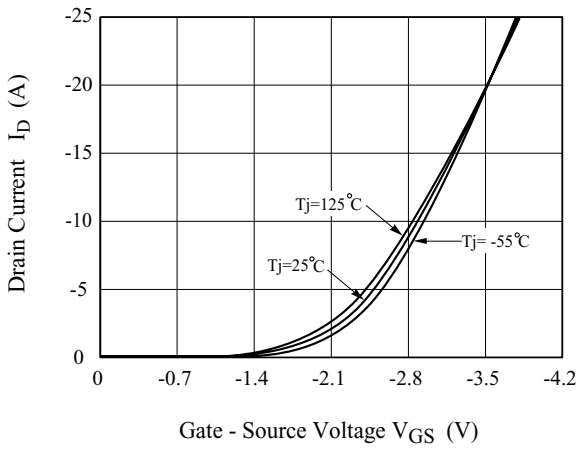

Normalized Transient Thermal Resistance
Square Wave Pulse Duration (sec)
0.5
0.2
0.1
0.05
0.02
0.01
Single Pluse
P_{DM}
t_1
t_2
1. $R_{thJA(t)}$ = r(t) *R_{thJA}
2. R_{thJA} = See data sheet
3. T_{JM}-T_A=P_{DM}*$R_{thJA(t)}$
4. Duty Cycle, D=t1/t2

P-Channel

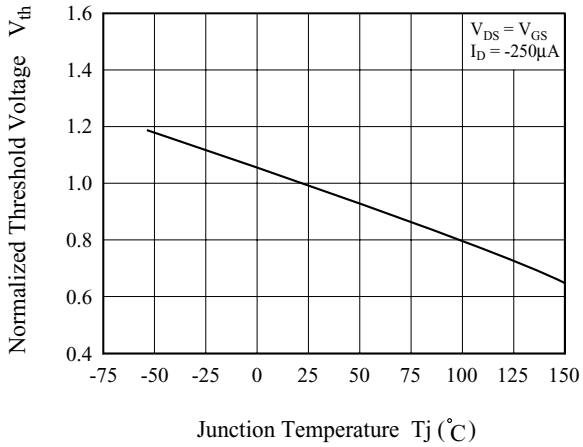
I_D - V_{DS}



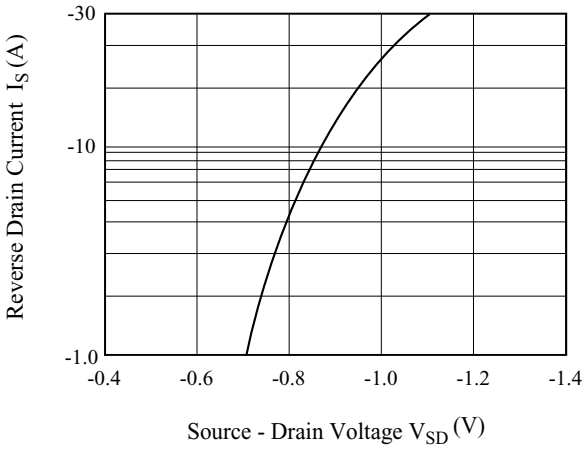
I_D - V_{GS}



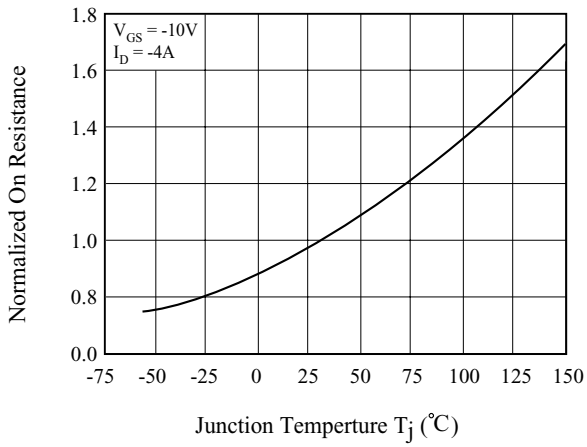
V_{th} - T_j



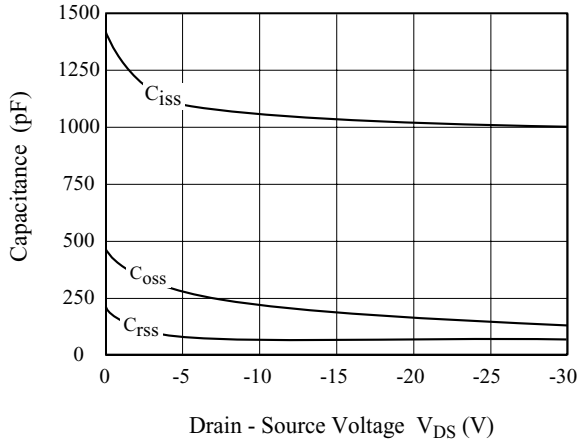
I_S - V_{SD}



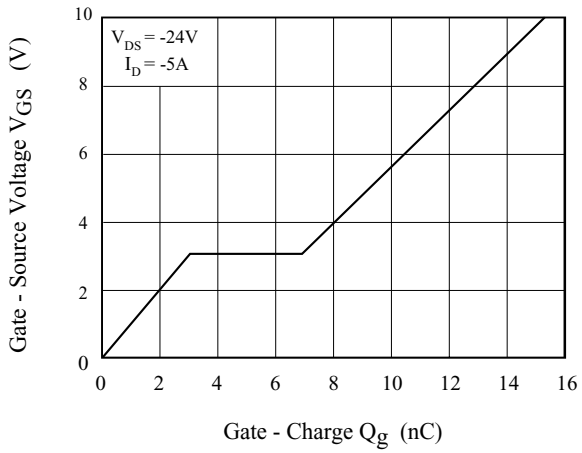
$R_{DS(ON)}$ - T_j



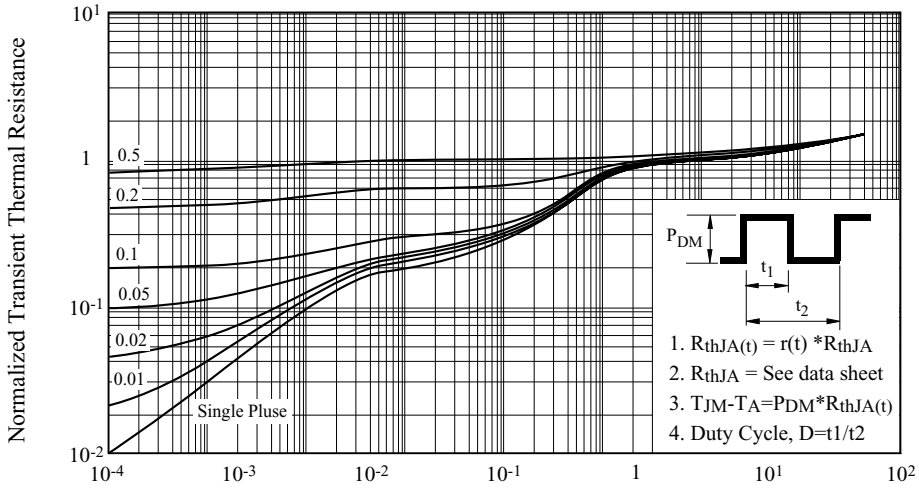
C - V_{DS}



Q_g - V_{GS}


V_{DS} = -24V
I_D = -5A
Gate - Source Voltage V_{GS} (V)
Gate - Charge Q_g (nC)
0
2
4
6
8
10
12
14
16

R_{th}


Normalized Transient Thermal Resistance
Square Wave Pulse Duration (sec)
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0.2
0.1
0.05
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0.01
Single Pluse
P_{DM}
t_1
t_2
1. $R_{thJA(t)}$ = r(t) *R_{thJA}
2. R_{thJA} = See data sheet
3. T_{JM}-T_A=P_{DM}*$R_{thJA(t)}$
4. Duty Cycle, D=t1/t2

Fig. 1 Gate Charge

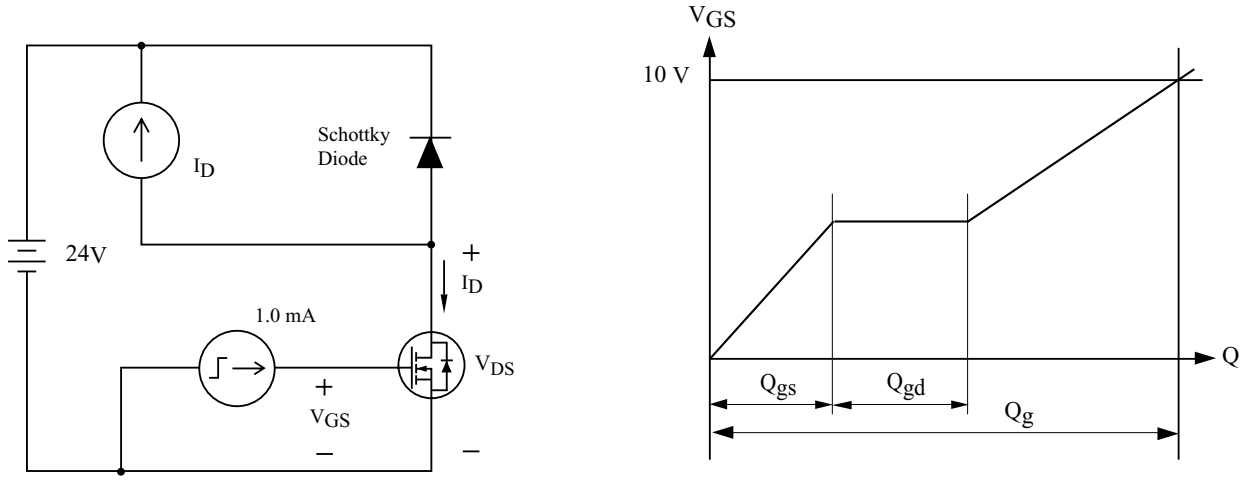
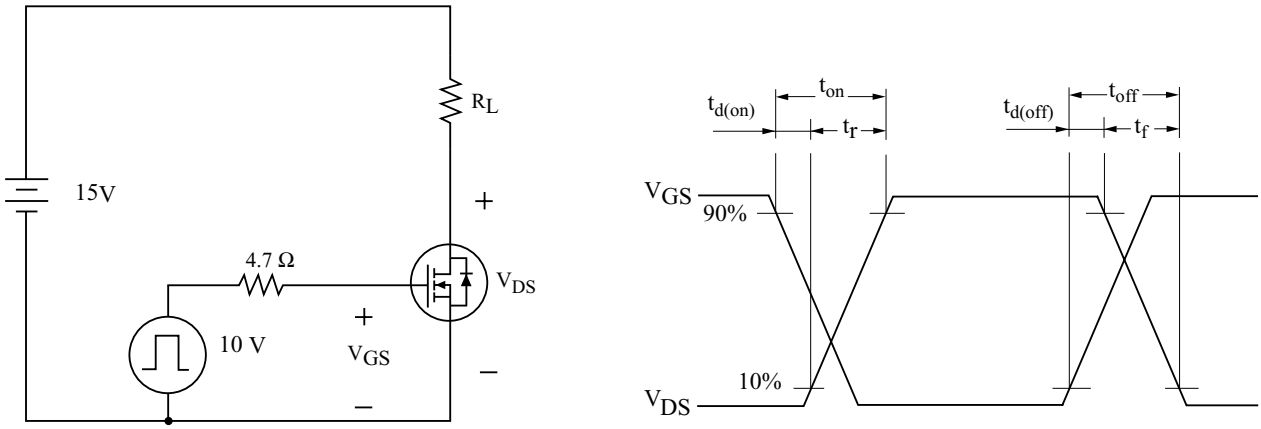
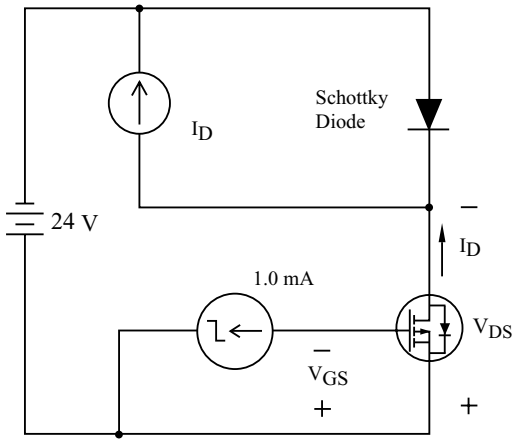


Fig. 2 Resistive Load Switching



P-Channel

Fig. 3 Gate Charge



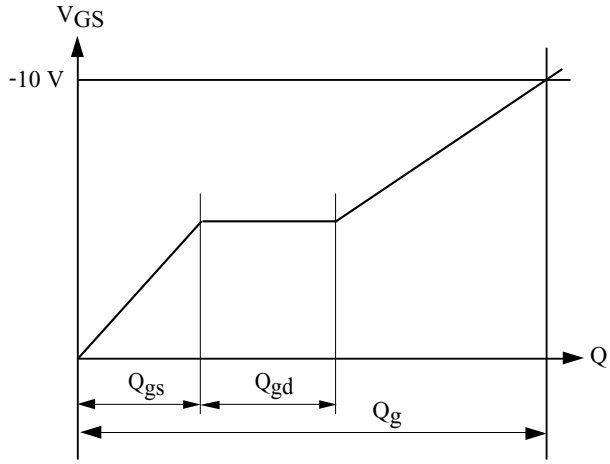


Fig. 4 Resistive Load Switching