Data Sheet | March 31, 2009 | FN6492.0

4-Channel And 6-Channel High Speed, Auto-direction Sensing Logic Level Translators

The ISL3034E, ISL3035E, ISL3036E 4- and 6-channel bi-directional, auto-direction sensing, level translators provide the required level shifting in multi-voltage systems at data transfer rates up to 100Mbps. The auto-direction sensing feature makes the ISL3034E, ISL3035E, ISL3036E ideally suited for memory-card level translation (or for generic four to six channel level translation) especially if bit-by-bit direction control is desired. The V_{CC} and V_L supply voltages set the logic levels on either side of the device. Logic signals present on the IC's V_L side appear as higher voltage logic signals on the IC's V_{CC} side and vice versa. The ISL3035E features a CLK_RET output that returns the same clock signal applied to the CLK_V_L input, but with timing that mimics the data returning from the I/OV_{CC} inputs.

The ISL3034E, ISL3035E, ISL3036E operate at full speed with external input drivers that source as little as 4mA output current. Each I/O channel is pulled up to V_{CC} or V_L by an internal 30µA current source, allowing the ISL3034E, ISL3035E, ISL3036E to be driven by either push-pull or open-drain drivers.

The ISL3034E and ISL3036E include an enable (EN) input that when driven low places the IC into a low-power shutdown mode, with all I/O lines tri-stated. All versions feature an automatic shutdown mode, that places the part in the same shutdown state when V_{CC} is less than V_L. The states of I/OV_{CC} and I/OV_L during shutdown are chosen by selecting the appropriate product (see Table 1).

The ISL3034E, ISL3035E, ISL3036E operate with V_{CC} voltages from +2.2V to +3.6V and V_L voltages from +1.35V to +3.2V, making them ideal for data transfer between low-voltage microcontrollers or ASICs and higher voltage components.

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	DATA RATE (Mbps)	NUMBER OF CHANNELS	EN PIN?	I/OV_L SHDN STATE	I/OV_{CC} SHDN STATE
ISL3034E	100	6	YES	16.5kΩ to V_L	16.5kΩ to V_{CC}
ISL3035E	100	6	NO	75kΩ to V_L	High Impedance
ISL3036E	100	4	YES	16.5kΩ to V_L	16.5kΩ to V_{CC}

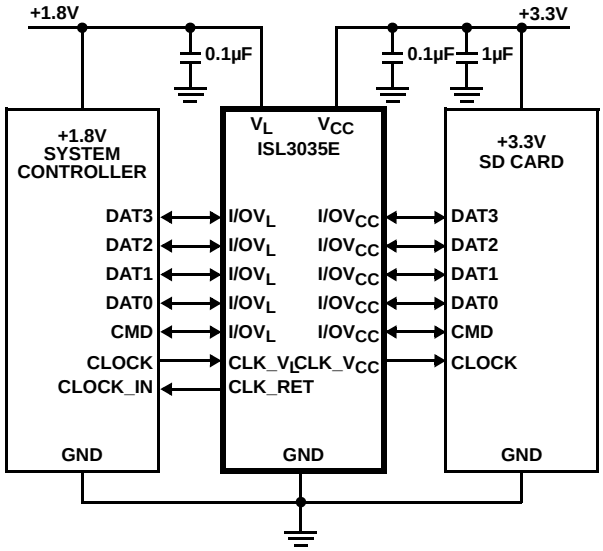
Features

- Best-In-Class ESD Protection: ±15kV IEC61000-4-2 ESD Protection on ALL Input, Output, and I/O Lines
- 100Mbps Guaranteed Data Rate
- Four (ISL3036) or Six (ISL3034, ISL3035) Bi-directional Channels
- Auto-direction Sensing Eliminates Direction Control Logic Pins
- Enable Input (ISL3034E, ISL3036E) for Logic Control of Low Power SHDN Mode
- Clock Return Output (ISL3035E)
- Compatible with 4mA Input Drivers or Larger
- +1.35V≤ V_L ≤ +3.2V and +2.2V ≤ V_{CC} ≤ +3.6V Supply Voltage Range
- Pb-Free (RoHS Compliant)
- 16Ld µTQFN (2.6mmx1.8mm),16 Ld TQFN (3mmx3mm), and 14 Ld QFN (3.5mmx3.5mm) Packages

Applications

- Simplifies the Interface Between Two Logic ICs Operating at Different Supply Voltages
- SD Card and MiniSD Card Level Translation
- MMC (Multi Media Card) Level Translation
- Memory Stick Card Level Translation

Typical Operating Circuit



Ordering Information

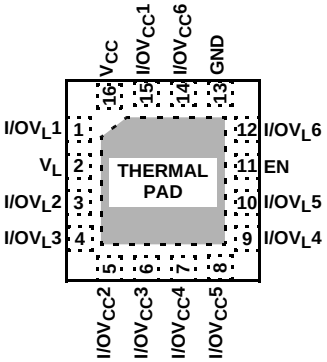
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL3034EIRTZ (Note 1)	34TZ	-40 to +85	16 Ld TQFN	L16.3x3A
ISL3034EIRTZ-T (Notes 1, 3)	34TZ	-40 to +85	16 Ld TQFN	L16.3x3A
ISL3034EIRUZ-T (Notes 2, 3)	GAE	-40 to +85	16 Ld µTQFN	L16.2.6x1.8A
ISL3035EIRTZ (Note 1)	35TZ	-40 to +85	16 Ld TQFN	L16.3x3A
ISL3035EIRTZ-T (Notes 1, 3)	35TZ	-40 to +85	16 Ld TQFN	L16.3x3A
ISL3035EIRUZ-T (Notes 2, 3)	GAF	-40 to +85	16 Ld µTQFN	L16.2.6x1.8A
ISL3036EIRZ-T (Notes 1, 3)	36EZ	-40 to +85	14 Ld QFN	L14.3.5x3.5
ISL3036EIRUZ-T (Notes 2, 3)	GAK	-40 to +85	16 Ld µTQFN	L16.2.6x1.8A

NOTES:

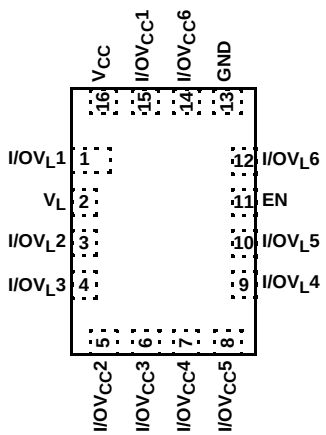
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. Please refer to TB347 for details on reel specifications.

Pinouts

ISL3034E
(16 LD TQFN)
TOP VIEW

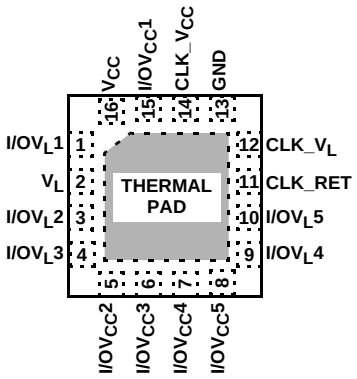


ISL3034E
(16 LD µTQFN)
TOP VIEW

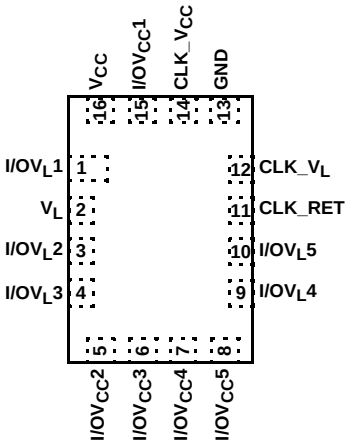


Pinouts (Continued)

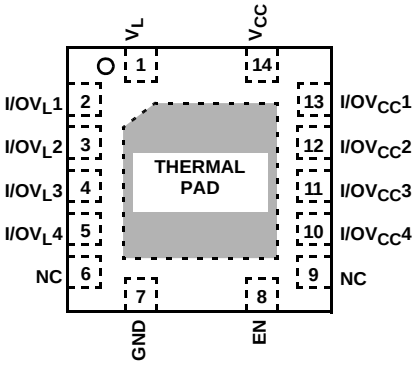
ISL3035E
(16 LD TQFN)
TOP VIEW



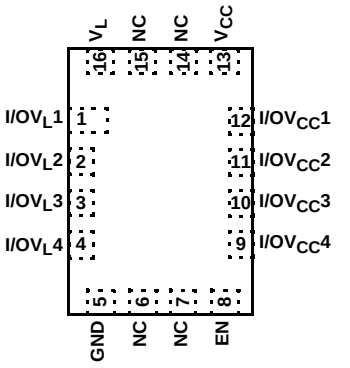
ISL3035E
(16 LD µTQFN)
TOP VIEW



ISL3036E
(14 LD QFN)
TOP VIEW



ISL3036E
(16 LD µTQFN)
TOP VIEW



Pin Descriptions

NAME	FUNCTION	NOTES
V_{CC}	V_{CC} power supply, +2.2V to +3.6V. Decouple V_{CC} to ground with a 0.1µF capacitor.	For normal operation, $V_{CC} > V_L$.
V_L	V_L logic supply, +1.35V to +3.2V. Decouple V_L to ground with a 0.1µF capacitor.	For normal operation, $V_{CC} > V_L$.
GND	Ground Pin	
EN	±15kV IEC61000 ESD Protected Enable Input. Logic “0” puts the device in shutdown. Logic “1” enables the device.	ISL3034E and ISL3036E only
$I/OV_{CC}x$	±15kV IEC61000 ESD Protected Input/Output channel referenced to V_{CC}.	
CLK_V_{CC}	±15kV IEC61000 ESD Protected Input/Output clock channel referenced to V_{CC}.	ISL3035E only
I/OV_Lx	±15kV IEC61000 ESD Protected Input/Output channel referenced to V_L.	
CLK_V_L	IEC61000 ESD Protected Input clock channel referenced to V_L.	ISL3035E only
CLK_RET	IEC61000 ESD Protected Output clock channel referenced to V_L.	ISL3035E only

Absolute Maximum Ratings

(All voltages referenced to GND.)

V_{CC}, V_L . . . . . -0.3V to +4V
$I/OV_{CC}\_$, CLK_V_{CC} . . . . . -0.3V to (V_{CC} + 0.3V)
$I/OV_L\_$, CLK_V_L, CLK_RET. . . . . -0.3V to (V_L + 0.3V)
EN . . . . . -0.3V to +4V
Short-Circuit Duration $I/OV_L\_$, $I/OV_{CC}\_$, CLK_V_{CC}, CLK_RET to GND. . . . . Continuous

Operating Conditions

Operating Temperature Range . . . . . -40℃ to +85℃

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (℃/W)	θ_{JC} (℃/W)
14 Ld QFN Package (Notes 4, 5).	46	6
16 Ld TQFN Package (Notes 4, 5). . . .	74	10
16 Ld µTQFN Package (Note 4)	93	44

Maximum Storage Temperature Range. . . . . -65℃ to +150℃
Maximum Junction Temperature . . . . . +150℃
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air, and with “direct attach” features for the QFN and TQFN. See Tech Brief TB379 for details.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{CC} = +2.2V to +3.6V, V_L = +1.35V to +3.2V, EN = V_L, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V and T_A = +25℃. (Note 6).

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (℃)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
POWER SUPPLIES							
V_L Supply Range	V_L	(Note 6)	Full	1.35	-	3.2	V
V_{CC} Supply Range	V_{CC}	(Note 6)	Full	2.2	-	3.6	V
V_{CC} Quiescent Supply Current	I_{CC}	I/OV_{CC} = V_{CC}, I/OV_L = V_L	Full	-	18	30	µA
V_L Quiescent Supply Current	I_{VL}	I/OV_{CC} = V_{CC}, I/OV_L = V_L	Full	-	12	18	µA
V_{CC} Shutdown Supply Current	I_{CCSD}	EN = GND or V_L > V_{CC} + 0.7V; ISL3034E and ISL3036E Only	Full	-	-	2.5	µA
		V_L > V_{CC} + 0.7V; ISL3035E Only	Full	-	-	2.5	µA
V_L Shutdown Supply Current	I_{LSD}	EN = GND or V_L > V_{CC} + 0.7V; ISL3034E and ISL3036E Only	Full	-	-	4	µA
		V_L > V_{CC} + 0.7V; ISL3035E Only	Full	-	-	4	µA
I/OV_{CC}, CLK_V_{CC} Tri-State Leakage Current	I_{LKG}	V_L > V_{CC} + 0.7V, V_O = 0V or V_{CC}, ISL3035E Only	Full	-	0.1	2	µA
EN Input Current	I_{IN_EN}	ISL3034E and ISL3036E Only	Full	-		1	µA
V_L - V_{CC} Shutdown Threshold High	V_{TH_H}	V_{CC} rising	Full	-0.2	0.05V_L	0.7	V
V_L - V_{CC} Shutdown Threshold Low	V_{TH_L}	V_{CC} falling	Full	-0.2	0.1V_L	0.7	V
I/OV_{CC}, I/OV_L Pull-up Resistance During Shutdown	R_{PU_SD1}	EN = GND; ISL3034E and ISL3036E Only	Full	10	16.5	23	kΩ
I/OV_L, CLK_V_L , CLK_RET Pull-up Resistance During Shutdown	R_{PU_SD2}	V_L > (V_{CC} + 0.7V); ISL3035E Only	Full	45	75	105	kΩ
$I/OV_L\_$, CLK_V_L, CLK_RET Pull-up Current	I_{VL_PU}	EN = V_L, I/OV_L = GND	Full	20	-	75	µA
$I/OV_{CC}\_$, CLK_V_{CC} Pull-up Current	I_{VCC_PU}	EN = V_L, I/OV_{CC} = GND	Full	20	-	75	µA
I/OV_L to I/OV_{CC} DC Resistance	R_{ON}		Full	-	3	-	kΩ

Electrical Specifications V_{CC} = +2.2V to +3.6V, V_L = +1.35V to +3.2V, EN = V_L, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V and T_A = +25°C. (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
ESD PROTECTION								
All Input and I/O Pins From Pin to GND		IEC61000-4-2 Air-Gap Discharge		25	-	±15	-	kV
		IEC61000-4-2 Contact Discharge		25	-	>±9	-	kV
		Human Body Model		25	-	±15	-	kV
All Pins		HBM, per JEDEC		25	-	>±12	-	kV
		Machine Model, per JEDEC		25	-	±1300	-	V
LOGIC-LEVEL THRESHOLDS								
I/OV_L, CLK_V_L Input Voltage High Threshold	V_{IHL}	(Note 7)		Full	-	-	V_L - 0.2	V
I/OV_L, CLK_V_L Input Voltage Low Threshold	V_{ILL}	(Note 7)		Full	0.15	-	-	V
I/OV_{CC}, CLK_V_{CC} Input Voltage High Threshold	V_{IHC}	(Note 7)		Full	-	-	V_{CC} - 0.4	V
I/OV_{CC}, CLK_V_{CC} Input Voltage Low Threshold	V_{ILC}	(Note 7)		Full	0.2	-	-	V
EN Input Voltage High Threshold	V_{IH}			Full	-	-	V_L - 0.4	V
EN Input Voltage Low Threshold	V_{IL}			Full	0.4	-	-	V
I/OV_L, CLK_RET Output Voltage High	V_{OHL}	I_{OH} = 20µA, $I/OV_{CC} \geq V_{CC}$ - 0.4V		Full	2/3 V_L	-	-	V
I/OV_L, CLK_RET Output Voltage Low	V_{OLL}	I_{OL} = 20µA, $I/OV_{CC} \leq$ 0.2V		Full	-	-	1/3 V_L	V
I/OV_{CC}, CLK_V_{CC} Output Voltage High	V_{OHC}	I_{OH} = 20µA, $I/OV_L \geq V_L$ - 0.2V		Full	2/3 V_{CC}	-	-	V
I/OV_{CC}, CLK_V_{CC} Output Voltage Low	V_{OLC}	I_{OL} = 20µA, $I/OV_L \leq$ 0.15V		Full	-	-	1/3 V_{CC}	V
RISE/FALL TIME ACCELERATOR STAGE								
Accelerator Pulse Duration		On falling edge		25	-	3	-	ns
		On rising edge		25	-	3	-	ns
I/OV_L, CLK_RET Output Accelerator Source Impedance		V_L = 1.62V		25	-	11	-	Ω
		V_L = 3.2V		25	-	6	-	Ω
I/OV_{CC}, CLK_V_{CC} Output Accelerator Source Impedance		V_{CC} = 2.2V		25	-	9	-	Ω
		V_{CC} = 3.6V		25	-	8	-	Ω
I/OV_L, CLK_RET Output Accelerator Sink Impedance		V_L = 1.62V		25	-	9	-	Ω
		V_L = 3.2V		25	-	8	-	Ω
I/OV_{CC}, $CLKV_{CC}$ Output Accelerator Sink Impedance		V_{CC} = 2.2V		25	-	10	-	Ω
		V_{CC} = 3.6V		25	-	9	-	Ω
TIMING CHARACTERISTICS (R_{SOURCE} = 150Ω, Input rise/fall time ≤ 1ns)								
I/OV_{CC}, CLK_V_{CC} Rise Time	t_{RVCC}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF, push-pull drivers		Full	-	-	3.2	ns
I/OV_{CC}, CLK_V_{CC} Fall Time	t_{FVCC}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF		Full	-	-	3.2	ns
I/OV_L, CLK_RET Rise Time	t_{RVL}	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_RET} = 15pF, push-pull drivers	$V_L \geq$ 1.35V	Full	-	-	4	ns
			$V_L \geq$ 1.62V	Full	-	-	3.5	ns

Electrical Specifications V_{CC} = +2.2V to +3.6V, V_L = +1.35V to +3.2V, EN = V_L, unless otherwise noted. Typical values are at V_{CC} = +3.3V, V_L = +1.8V and T_A = +25°C. (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
I/OV_L, CLK_RET Fall Time	t_{FVL}	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_RET} = 15pF	$V_L \geq 1.35V$	Full	-	-	4	ns
			$V_L \geq 1.62V$	Full	-	-	3.5	ns
I/OV_{CC}, CLK_V_{CC} Propagation Delay (Driving I/OV_L, CLK_V_L)	t_{PDVCC}	R_S = 150Ω, $C_{I/OVCC}$ = 10pF, C_{CLK_VCC} = 10pF, push-pull drivers	$V_L \geq 1.35V$	Full	-	-	7.5	ns
			$V_L \geq 1.62V$	Full	-	-	6.5	ns
t_{PDVCC} Channel-to-Channel Skew (Note 9)	t_{SKEWC}		$V_L \geq 1.35V$	Full	-	-	1.3	ns
			$V_L \geq 1.62V$	Full	-	-	1	ns
I/OV_L, CLK_RET Propagation Delay (Driving I/OV_{CC}, CLK_V_{CC})	t_{PDVL}	R_S = 150Ω, $C_{I/OVL}$ = 15pF, C_{CLK_RET} = 15pF, push-pull drivers		Full	-	-	6.5	ns
t_{PDVL} Channel-to-Channel Skew (Note 9)	t_{SKEWL}		$V_L \geq 1.35V$	Full	-	-	1.3	ns
			$V_L \geq 1.62V$	Full	-	-	0.8	ns
Delay from EN High to I/OV_{CC} Active	t_{EN-VCC}	R_{LOAD} = 1MΩ, $C_{I/OVCC}$ = 10pF (ISL3034E and ISL3036E)		25	-	1.5	-	µs
Delay from EN High to I/OV_L Active	t_{EN-VL}	R_{LOAD} = 1MΩ, $C_{I/OVL}$ = 15pF (ISL3034E and ISL3036E)		25	-	1.5	-	µs
Maximum Data Rate	$D.R._{1.35}$	Push-pull operation, R_{SOURCE} = 150Ω, $C_{I/OVCC}$ = 10pF, $C_{I/OVL}$ = 15pF, C_{CLK_VCC} = 10pF, C_{CLK_RET} = 15pF	$V_L \geq 1.35V$	Full	85	-	-	Mbps
	$D.R._{1.6}$		$V_L \geq 1.62V$	Full	100	-	-	Mbps

NOTES:

6. V_L must be less than or equal to V_{CC} - 0.2V during normal operation. However, V_L can be greater than V_{CC} during start-up and shutdown conditions and the part will not latch-up nor be damaged.
7. Input thresholds are referenced to the boost circuit.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. Delta between all I/OV_L channel prop delays, or delta between all I/OV_{CC} channel prop delays, all channels tested at the same test conditions.

Test Circuits and Waveforms

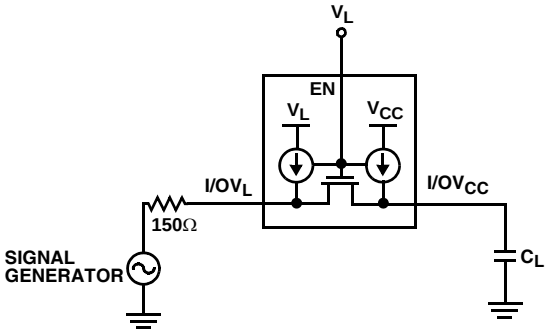


FIGURE 1A. TEST CIRCUIT

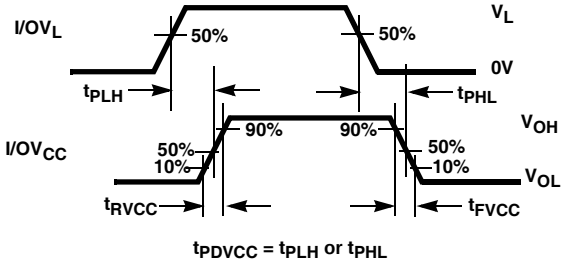


FIGURE 1B. MEASUREMENT POINTS

FIGURE 1. I/OV_{CC} OUTPUT PROPAGATION DELAY AND TRANSITION TIMES (PUSH - PULL)

Test Circuits and Waveforms (Continued)

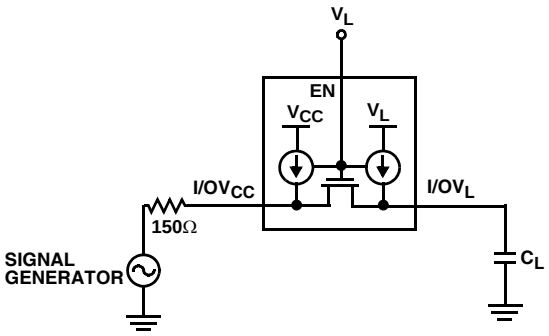


FIGURE 2A. TEST CIRCUIT

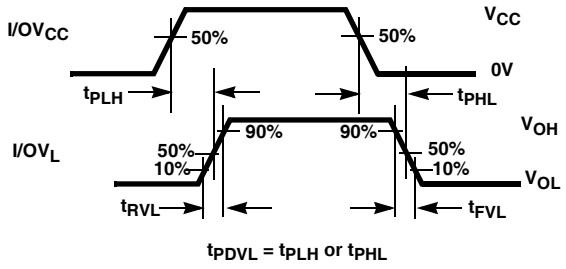
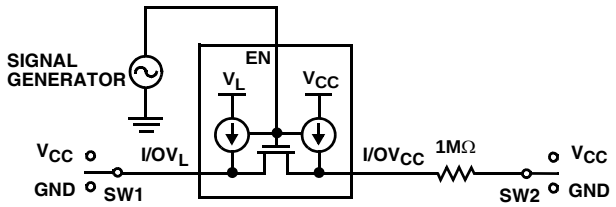


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. I/OV_L OUTPUT PROPAGATION DELAY AND TRANSITION TIMES (PUSH - PULL)



PARAMETER	SW1	SW2
t_{ENL}	GND	V_{CC}
t_{ENH}	V_{CC}	GND

FIGURE 3A. TEST CIRCUIT

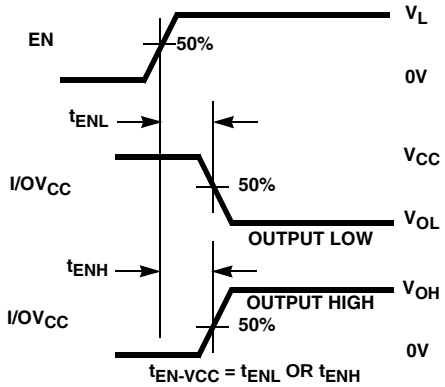
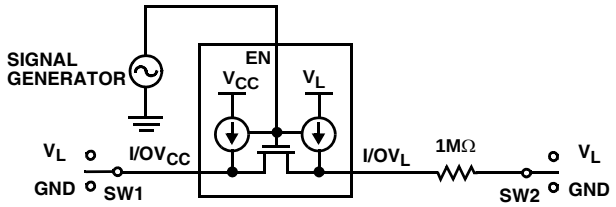


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. I/OV_{CC} OUTPUT ENABLE TIMES



PARAMETER	SW1	SW2
t_{ENL}	GND	V_L
t_{ENH}	V_L	GND

FIGURE 4A. TEST CIRCUIT

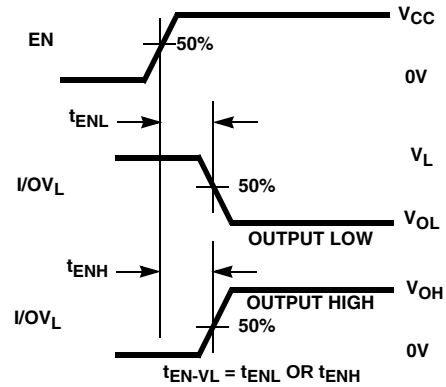


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. I/OV_L OUTPUT ENABLE TIMES

Application Information

Overview

The ISL3034E, ISL3035E, ISL3036E are 100Mbps, bi-directional voltage level translating ICs for multi-supply voltage systems. These products shift lower voltage levels on one interface side (supplied by V_L) to a higher voltage level on the other interface side (supplied by V_{CC}), or vice versa. V_{OH} of the I/OV_L pins tracks the V_L supply, while V_{OH} of the I/OV_{CC} pins tracks the V_{CC} supply.

These ICs feature bit-by-bit auto-direction sensing to increase flexibility, and to eliminate the need for direction control pins. On chip pull-up current sources in the active mode, and pull-up resistors in SHDN mode, eliminate the need for most external bus resistors. Drivers interfacing with these level translators may be open-drain or push-pull types, and all three versions may also be used for unidirectional level shifting.

The three versions share the same architecture, but the ISL3034E is a general purpose 6-Channel version, while the 6-Channel ISL3035E specifically targets SD Card and other memory card applications. The 4-channel ISL3036 targets nibble and byte based applications, as well as 4-wire SPI interfaces. Power supply ranges allow level shifting between 1.5V, 1.8V, and 2.5V powered devices on the V_L side to 2.5V, and 3.3V devices on the V_{CC} side.

Principles of Operation

When enabled, these level shifters detect transitions on an I/O pin, and drive the appropriate logic level on the corresponding I/O pin on the other “side”. If the transition was low-to-high, the channel shifts the voltage up to V_{CC} (for transitions on an I/OV_L pin) or down to V_L (for transitions on an I/OV_{CC} pin), and then drives the shifted level on the other side. The ISL3035E enables whenever $V_{CC} > V_L + 200mV$, while the ISL3034E and ISL3036E enable if EN = 1 AND $V_{CC} > V_L + 200mV$.

Upon detecting a transition on either I/O pin, that channel’s accelerator circuitry actively drives the opposite side’s (output) pin to GND or the output’s supply rail, and then turns off. Weak hold circuitry then maintains the logic state until the input is 3-stated, or until another active transition occurs on either I/O pin for that channel. Figure 5 shows the simplified block diagram of one level shifting channel. The accelerator circuitry comprises high and low threshold detectors, one shots with level shifters and large output drivers. A transition on one of the I/OV_L or I/OV_{CC} pins momentarily defines that pin as an input. When the high or low threshold is crossed, a one-shot fires either the PMOS or NMOS driver, respectively, on the opposite side (effectively the output). These drivers are large enough to quickly drive the output node to its respective supply or to GND. Note that this transition on the “output” trips the transition detector on that pin, firing its accelerator, which feeds back to the “input” to help reinforce slow transitions, such as those from an

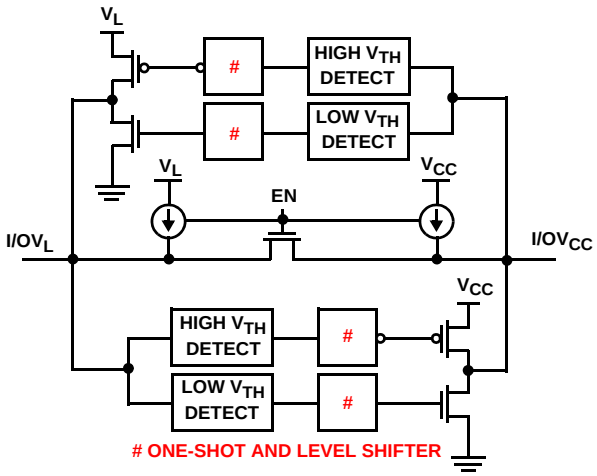


FIGURE 5. ONE CHANNEL SIMPLIFIED SCHEMATIC

open-drain type driver. Once the one-shot - and thus the accelerator - times out (approximately 3ns to 4ns), the large output drivers tri-state and the pins are weakly held in the last state by the small NMOS transistor between I/OV_L and I/OV_{CC} (for a low) or by the small current sources (for a high). In this static state, the I/O pins are easily overdriven by the next transition from an external driver. Having large pull-up and pull-down devices in the accelerator (vs just an active pull-up) nearly eliminates the concern about the external driver’s output impedance, and that impedance’s effect on V_{OL}, fall times and data rate.

The weak pull-up current sources on each I/O pin and the NMOS pass transistors, remain ON whenever the IC is enabled. If a channel’s external driver tri-states, the weak pull-up currents either keep the I/O pins high, or if the last state was a low the current sources pull the I/O pins high. In the latter case, each channel’s accelerators will once again fire when either the I/OV_L or the I/OV_{CC} voltage crosses the accelerator’s high threshold level.

Auto Direction Sensing

Each level translator channel independently and automatically determines the direction of data transfer without any external control signals. As described earlier, a transition on either of the channel’s I/O pins momentarily defines that pin as an input, which then translates and drives that input signal to the channel’s corresponding pin on the other port (now the output). After a brief period of active driving, both I/O pins return to their weak “hold” mode, where the next transition on either I/O pin determines the direction for the next transfer.

Auto sensing saves valuable processor GPIO pins (three [CLK, CMD, DAT] for SD Card applications, or six for the general purpose hex case), and simplifies the software associated with the peripheral interface.

Using Open Drain Drivers

These level translators’ accelerator based architecture works equally well when driven by push-pull or open drain type drivers (e.g., for the CMD line initialization in MMC

applications). The low static pull-up current is easily overdriven by an active pull-down, and the feedback nature of the accelerators (i.e., the accelerator firing in one direction also triggers the accelerator in the opposite direction) aids the passive pull-up once the input signal passes the accelerator's high threshold. The pull-up current and load capacitance set the input signal rise time, and thus the maximum data rate. For slow data rates the internal pull-up current may suffice, but higher data rates - or more heavily loaded signal lines - may require an external pull-up resistor.

Using External Bus Resistors

As mentioned earlier, these level translators incorporate I/O pin pull-up current sources when enabled, and I/O pin pull-up resistors in SHDN (except for the ISL3035E's I/OV_{CC} pins). Therefore, external pull-up or pull-down resistors shouldn't be necessary, and aren't recommended, unless using high-speed open drain signaling.

Power Supplies

WIDE SUPPLY RANGE

These ICs operate from a wide range of supply voltages. V_L is designed to connect to the supply of 1.5V, 1.8V, and 2.5V powered devices, while V_{CC} is targeted for 2.5V, and 3.3V components. Remember that V_{CC} must be greater than V_L for proper operation.

POWER SUPPLY SEQUENCING

Either V_{CC} or V_L may be powered up first, but the IC remains in SHDN until V_{CC} exceeds V_L by as much as 200mV. V_L may exceed V_{CC} by as much as 4V without causing any damage.

I/O PIN INPUT THRESHOLDS VS SUPPLY VOLTAGE

Even though the "Electrical Specification" table on page 4 shows the I/O pin input thresholds (V_{IH}, V_{IL}) with a fixed delta from the supplies or GND, the thresholds are better represented as a percentage of the supplies. The typical I/OV_{CC} and CLK_V_{CC} V_{IH} runs about 55% to 60% of V_{CC}, while the corresponding V_{IL} runs about 33% of V_{CC}. The typical I/OV_L and CLK_V_L V_{IH} runs about 60% to 70% of V_L, while the corresponding V_{IL} runs about 25% to 35% of V_L.

Low Power SHDN Mode

This family of level translators features a low power SHDN mode that tri-states all the I/O and output pins, considerably reduces current consumption, and enables any pull-up resistors on a port's I/O pins (see Table 1). The ISL3034E and ISL3036E enter the SHDN mode when the EN input switches low, or automatically when the V_{CC} voltage drops below the V_L voltage. The ISL3035 has no enable pin, so it enters SHDN only if V_{CC} drops below V_L. The V_L supply powers the EN circuitry.

ISL3034E and ISL3036E

The ISL3034E and ISL3036E are general purpose level translators featuring an enable pin, and six or four channels, respectively. Both products include SHDN mode 16.5kΩ pull-ups on the I/OV_{CC} and I/OV_L pins.

ISL3035E

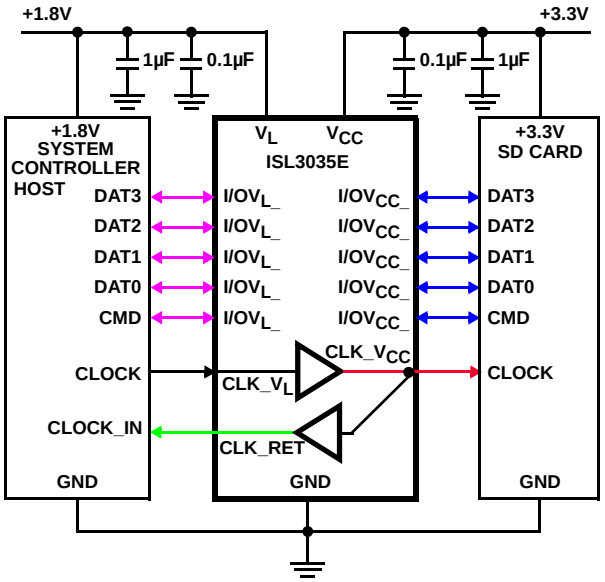


FIGURE 6. ISL3035E IN AN SD CARD APPLICATION

The ISL3035E specifically targets memory card applications, and Figure 6 illustrates its use in an SD Card application. Instead of six general purpose channels, the ISL3035E features five general purpose channels and one dedicated CLK channel. In memory card applications, the CLK channel is a unidirectional signal driven by the host controller and used by the memory card to synchronize data reads and writes. The ISL3035E's CLK channel is unique in that the host CLK applied to the CLK_V_L pin routes to the memory card via the CLK_V_{CC} pin, but it also loops back to the host on the CLK_RET pin. This CLK_RET signal better mimics the timing of "read" data returned from the memory card (see Figure 21 for signal timing), so using CLK_RET as the host's input CLK improves the CLK to data timing relationship.

CLK_RET is strictly an output, and CLK_V_L is strictly an input. If an ISL3035E application needs a sixth I/O channel then the user needs to connect CLK_V_L and CLK_RET together. Connected this way, the combination channel has the same architecture as the other I/O channels. Both CLK_RET and CLK_V_L have equivalent pull-up current sources and SHDN pull-up resistors, so connecting these two pins together doubles the pull-up current in either mode.

The bit-by-bit auto direction control eliminates the need for GPIO signals to control the flow of data on the CMD and DAT lines.

The ISL3035E has no enable pin, so it only enters the low power SHDN mode when V_{CC} drops below V_L. There are no SHDN pull-up resistors on the I/OV_{CC} and CLK_V_{CC} pins, but there are 75kΩ pull-ups on the I/OV_L, CLK_V_L, and CLK_RET pins.

Best-in-Class ESD Protection

All pins on these devices include class 3 (>12kV) Human Body Model (HBM) ESD protection structures, but the input and I/O pins incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM and ±15kV to IEC61000-4-2. The I/OV_{CC} pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a memory card, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up and without degrading the level shifting performance. This built-in ESD protection eliminates the need for board level protection structures (e.g., transient suppression diodes) and the associated, undesirable capacitive load they present. To ensure the full benefit of the built-in ESD protection, connect the IC's GND pin directly to a low impedance GND plane.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (typically I/OV_{CC} pins in memory card applications) but the ISL3034E, ISL3035E, and ISL3036E feature IEC61000 ESD protection on all logic and I/O pins (both I/OV_L and I/OV_{CC}, as well as CLK pins). Unlike HBM and MM methods which only test each pin-to-pin combination without applying power, IEC61000 testing is also performed with the IC in its typical application configuration (power applied). The IEC61000 standard's lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into these devices' pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. All the EN, CLK, and I/O pins withstand ±15kV air-gap discharges, relative to GND.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. Devices in this family survive ±9kV contact discharges (relative to the GND pin) on the EN, CLK, and I/O pins.

Layout and Decoupling Considerations

These level translators' high data rates and fast signal transitions require that the accelerators have high transient currents. Thus, short, low inductance supply traces and decoupling within 1/8th inch of the IC are imperative with very low impedance GND return paths.

Typical Performance Curves

V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, Data Rate = 100Mbps, push-pull driver, T_A = +25°C; Unless Otherwise Specified.

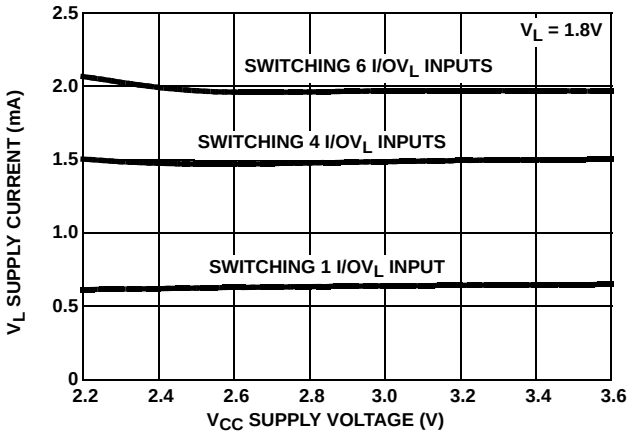


FIGURE 7. V_L SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

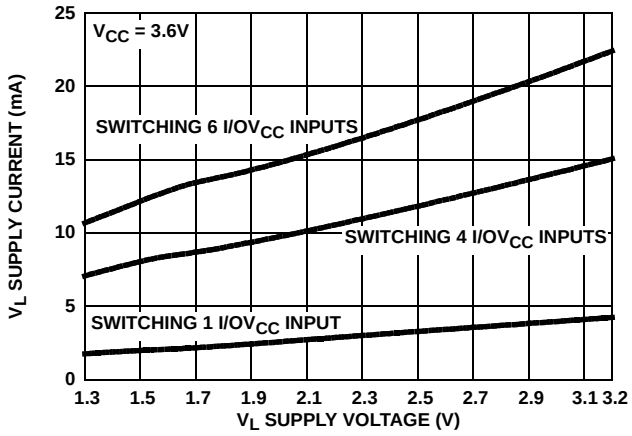


FIGURE 8. V_L SUPPLY CURRENT vs V_L SUPPLY VOLTAGE

Typical Performance Curves

V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, Data Rate = 100Mbps, push-pull driver, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

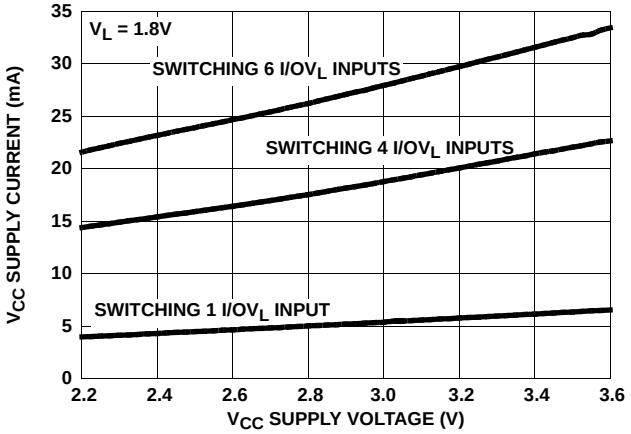


FIGURE 9. V_{CC} SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

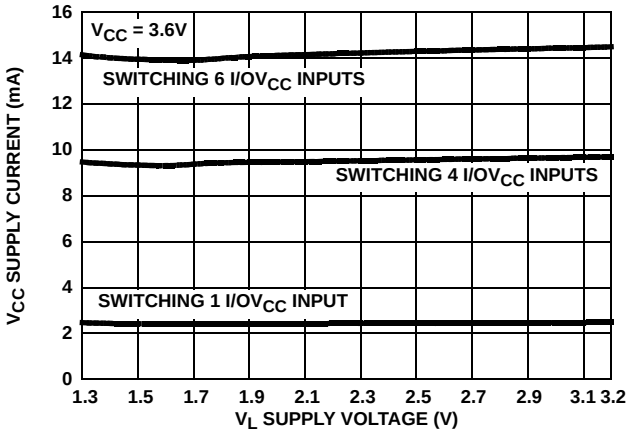


FIGURE 10. V_{CC} SUPPLY CURRENT vs V_L SUPPLY VOLTAGE

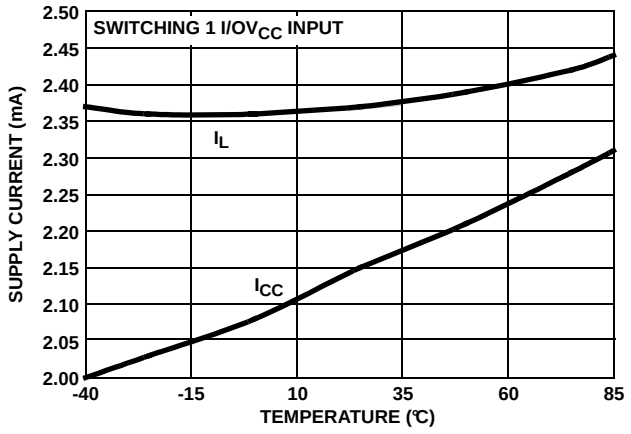


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

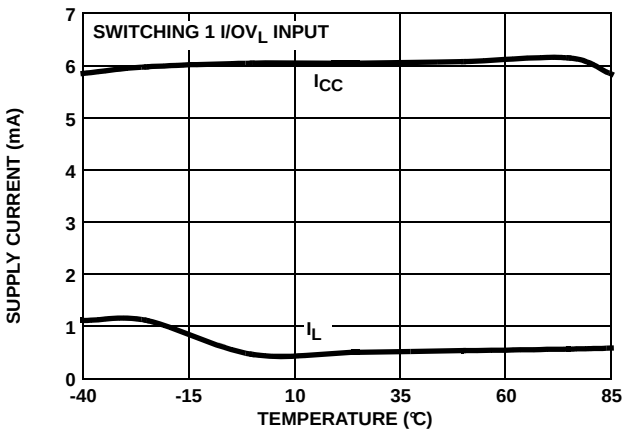


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

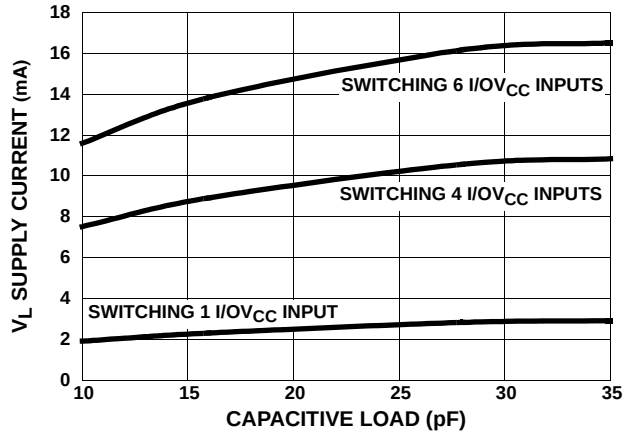


FIGURE 13. V_L SUPPLY CURRENT vs I/OV_L CAPACITIVE LOAD

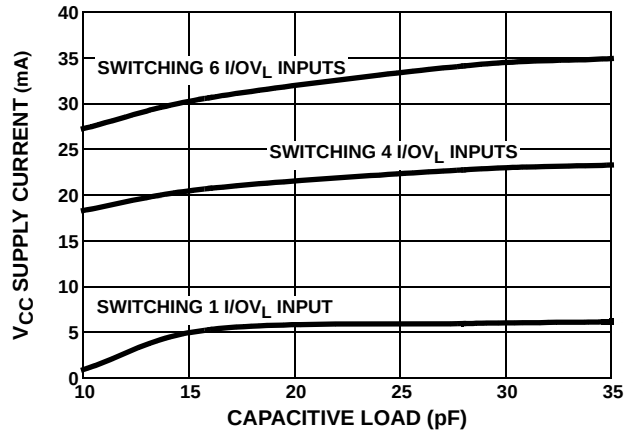


FIGURE 14. V_{CC} SUPPLY CURRENT vs I/OV_{CC} CAPACITIVE LOAD

Typical Performance Curves

V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, Data Rate = 100Mbps, push-pull driver, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

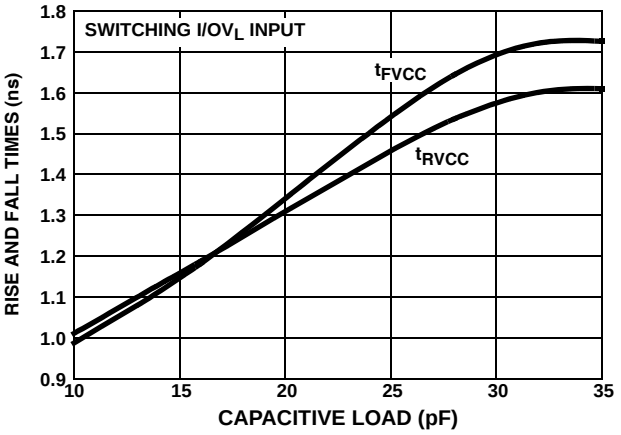


FIGURE 15. RISE/FALL TIME vs I/OV_{CC} CAPACITIVE LOAD

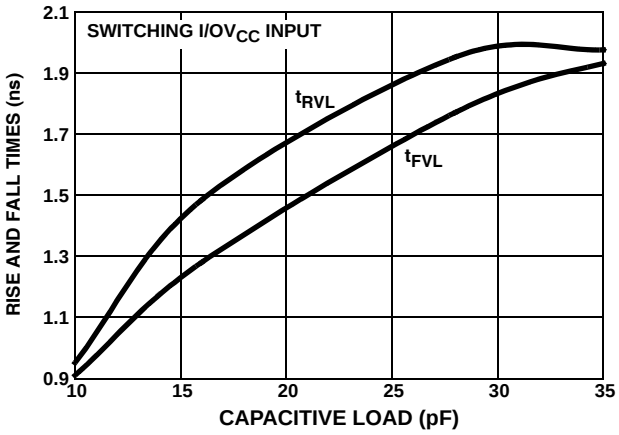


FIGURE 16. RISE/FALL TIME vs I/OV_L CAPACITIVE LOAD

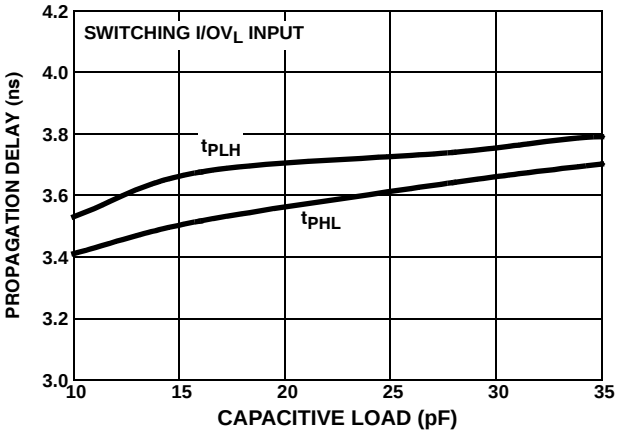


FIGURE 17. PROPAGATION DELAY vs I/OV_{CC} CAPACITIVE LOAD

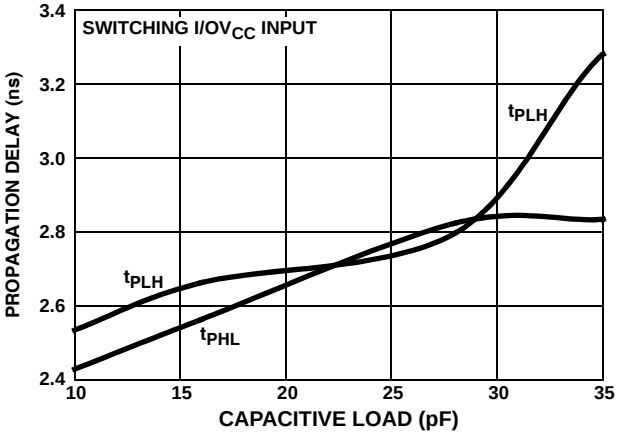


FIGURE 18. PROPAGATION DELAY vs I/OV_L CAPACITIVE LOAD

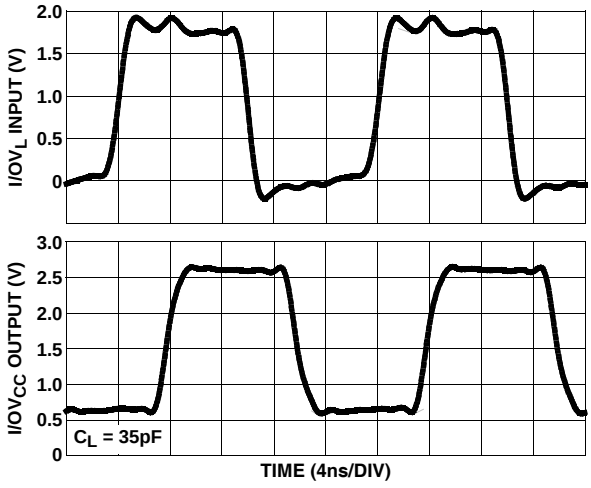


FIGURE 19. I/OV_{CC} OUTPUT WAVEFORMS (100Mbps)

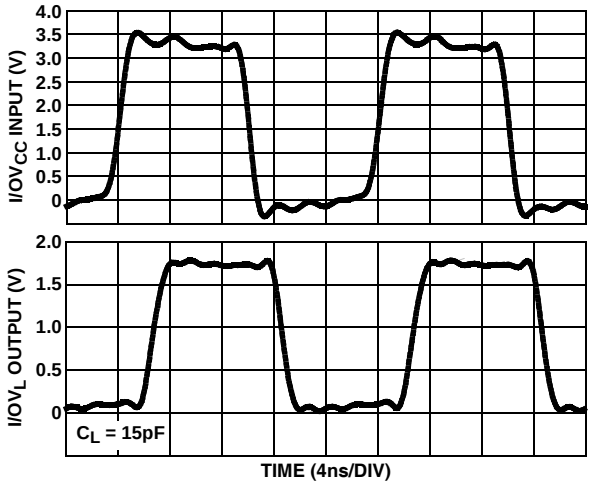


FIGURE 20. I/OV_L OUTPUT WAVEFORMS (100Mbps)

Typical Performance Curves

V_{CC} = 3.3V, V_L = 1.8V, C_L = 15pF, R_{SOURCE} = 150Ω, Data Rate = 100Mbps, push-pull driver, T_A = +25°C; Unless Otherwise Specified. **(Continued)**

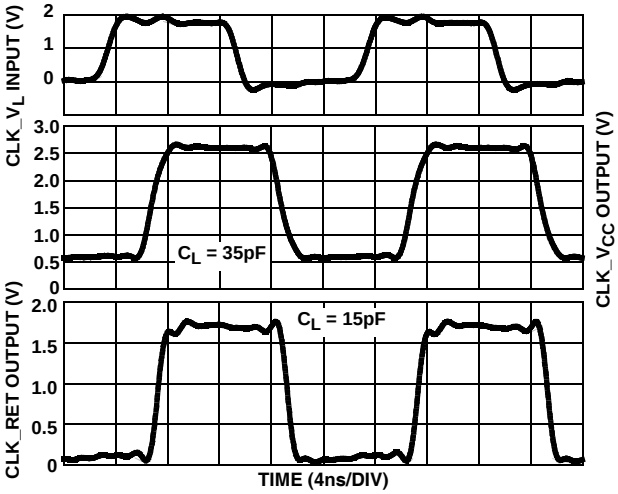


FIGURE 21. ISL3035E CLOCK WAVEFORMS (100Mbps)

Die Characteristics

SUBSTRATE AND TQFN/QFN THERMAL PAD POTENTIAL (POWERED UP):

GND

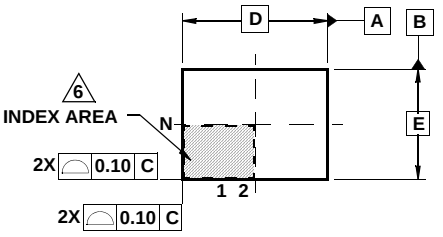
TRANSISTOR COUNT:

ISL3034E, ISL3035E - 2600
ISL3036E - 2000

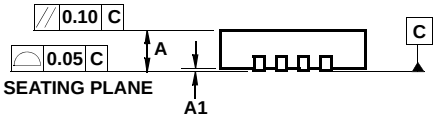
PROCESS:

Si Gate BiCMOS

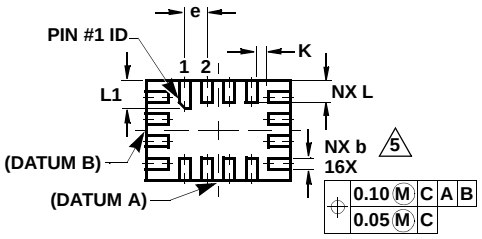
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



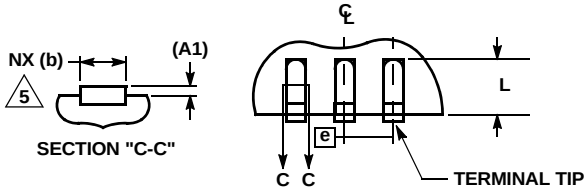
TOP VIEW

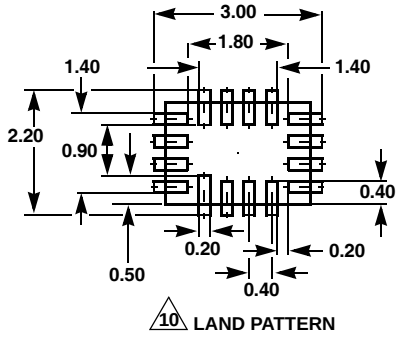


SIDE VIEW



BOTTOM VIEW





L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e		0.40 BSC		-
K	0.15	-	-	-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		16		2
Nd		4		3
Ne		4		3
θ	0	-	12	4

Rev. 5 2/09

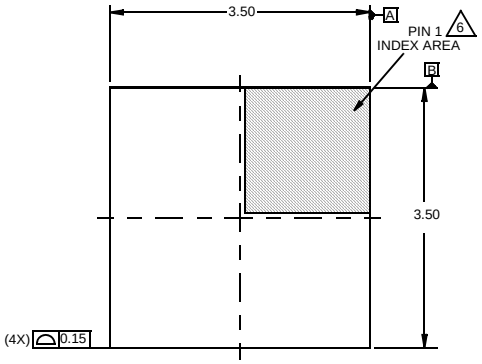
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.

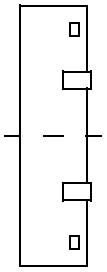
Package Outline Drawing

L14.3.5x3.5

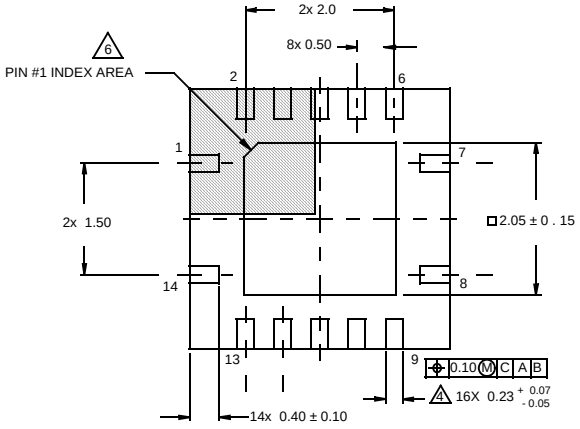
14 LEAD QUAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (QFN)
Rev 0, 2/08



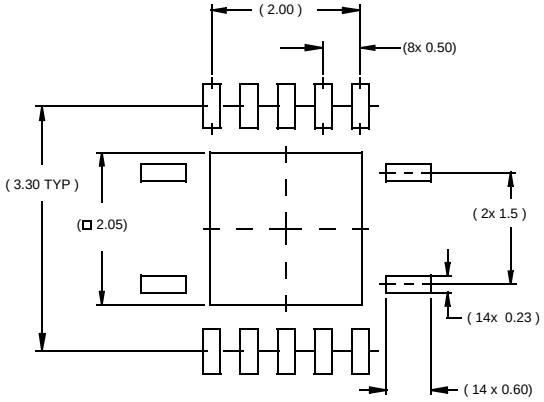
TOP VIEW



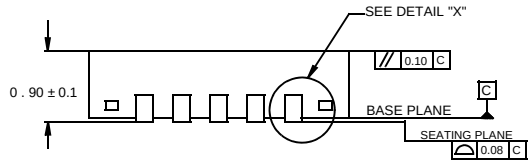
VIEW “A-A”



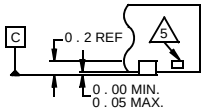
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

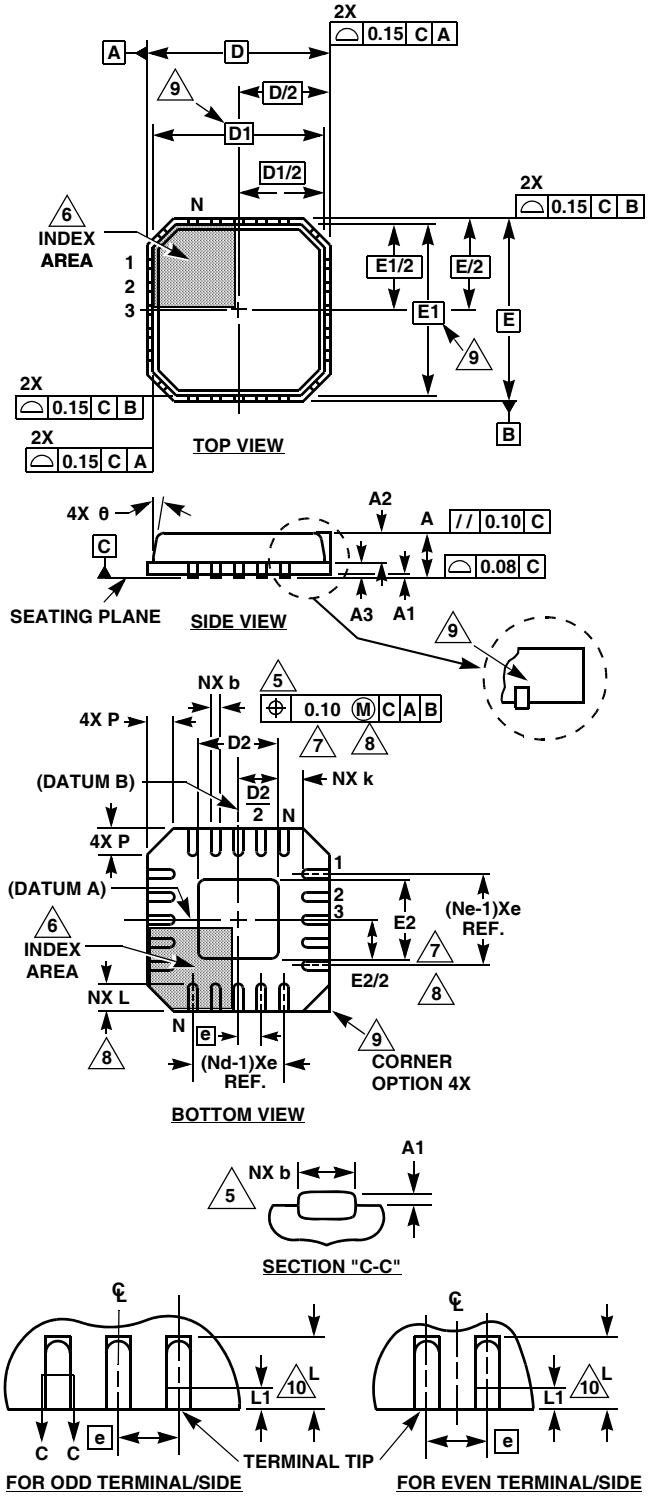


DETAIL “X”

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Lead width dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)



L16.3x3A

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A2	-	-	0.80	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		3.00 BSC		-
D1		2.75 BSC		9
D2	1.35	1.50	1.65	7, 8, 10
E		3.00 BSC		-
E1		2.75 BSC		9
E2	1.35	1.50	1.65	7, 8, 10
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220WEED-2 Issue C, except for the E2 and D2 MAX dimension.