Data Sheet | March 9, 2006 | FN9265.0

CCFL Brightness Controller

ISL6884 controls Pulse Width Modulated Dimming for up to 8 inverters to supply power to up to 40 Cold Cathode Fluorescent Lamps (CCFL) for back lighting in large LCD displays.

The ISL6884 brightness controller provides an I^2C interface for dimming control, enable, status, and brightness balance. The duty cycle of all 8 DPWM outputs is adjusted with a Master Brightness Control register. The duty cycle of each of the 8 DPWM outputs can be offset from the master brightness to adjust for uniform brightness.

The PWM dimming frequency can be set by an internal, adjustable oscillator or synchronized to an external source to minimize interference with video.

ISL6884's slave address is:

- 1101_1111 for reading
- 1101_1110 for writing

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. DWG. #
ISL6884IAZ (See Note)	-40 to 85	20 Ld SSOP (Pb-free)	M20.15
ISL6884IAZ-T (See Note)	-40 to 85	20 Ld SSOP Tape and Reel (Pb-free)	M20.15

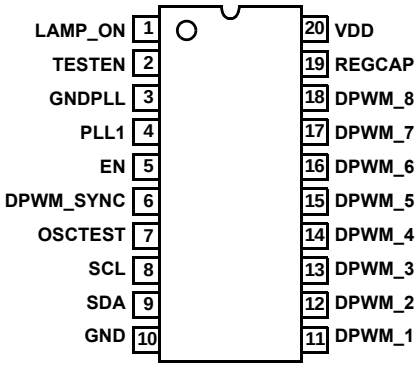
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

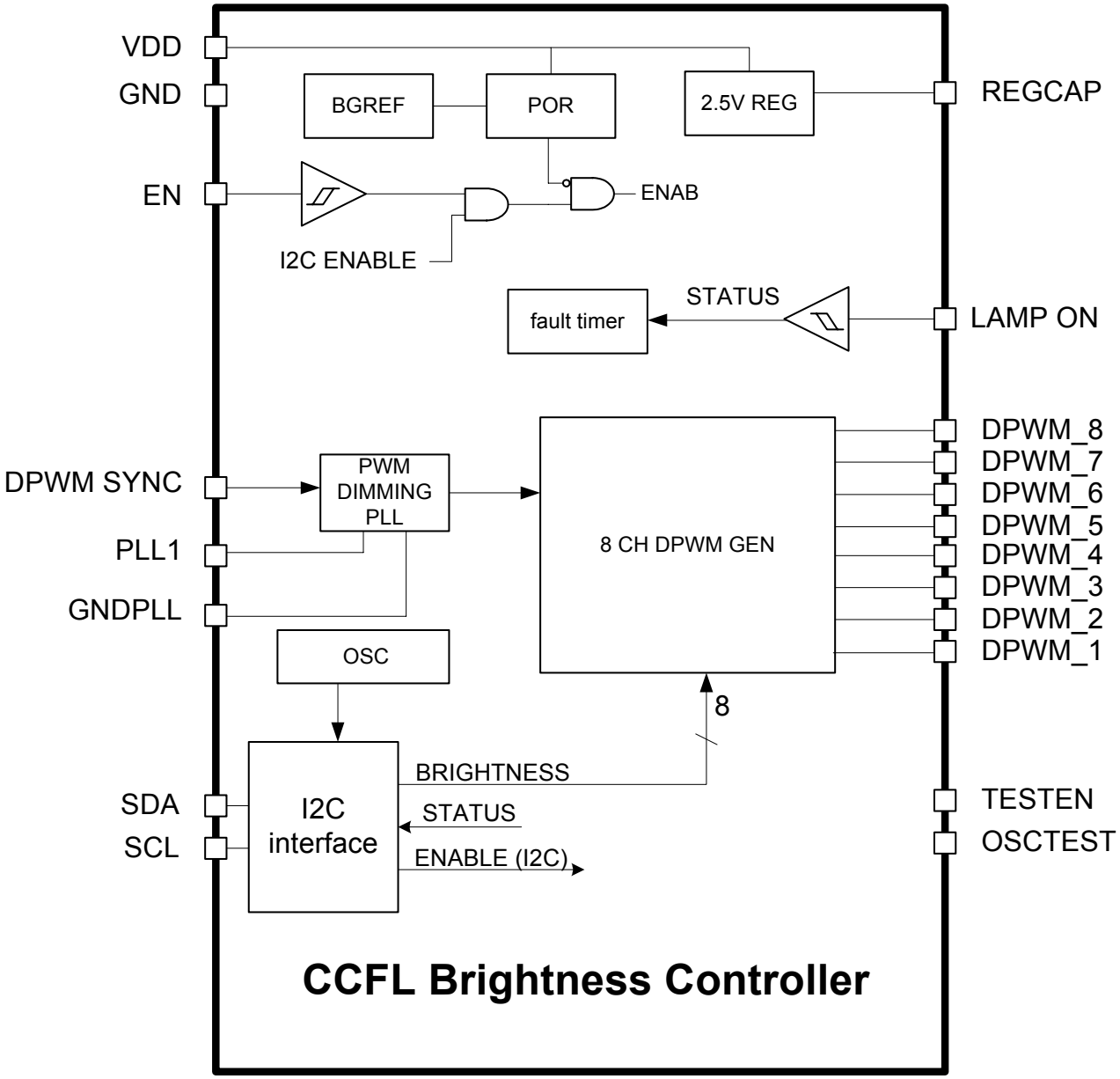
- Wide Supply Voltage Range of 3.0V to 5.5V
- Dimming
  - I^2C dimming control input
  - PWM dimming can be synchronized to an external source or set by an internal, adjustable oscillator.
  - 8 channel dimming allows the user to balance the brightness of the CCFL lamps via I^2C control
  - User programmable fault time out
- User Programmable Fault Time Out
- I^2C Status Output
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

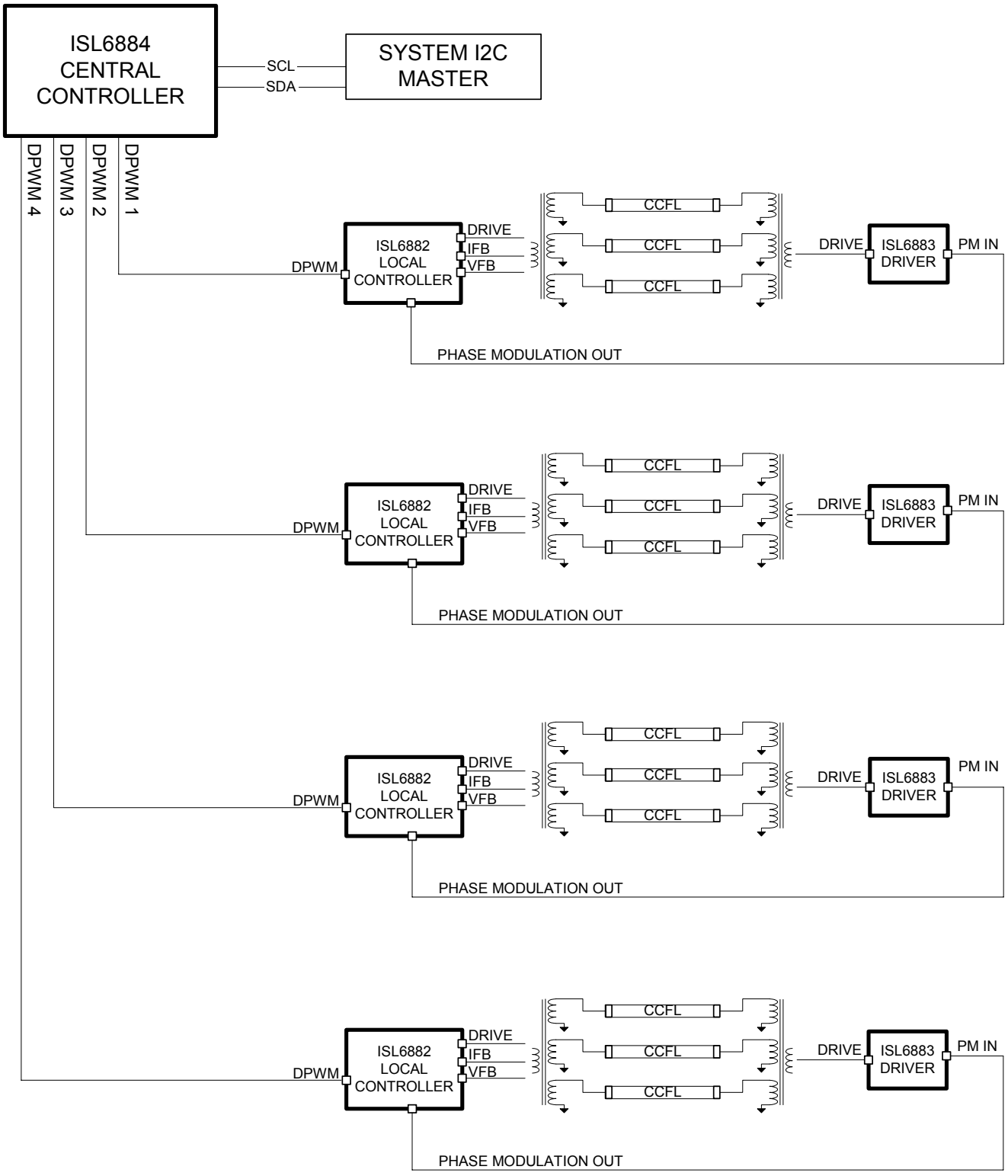
ISL6884
(20 LD SSOP)
TOP VIEW



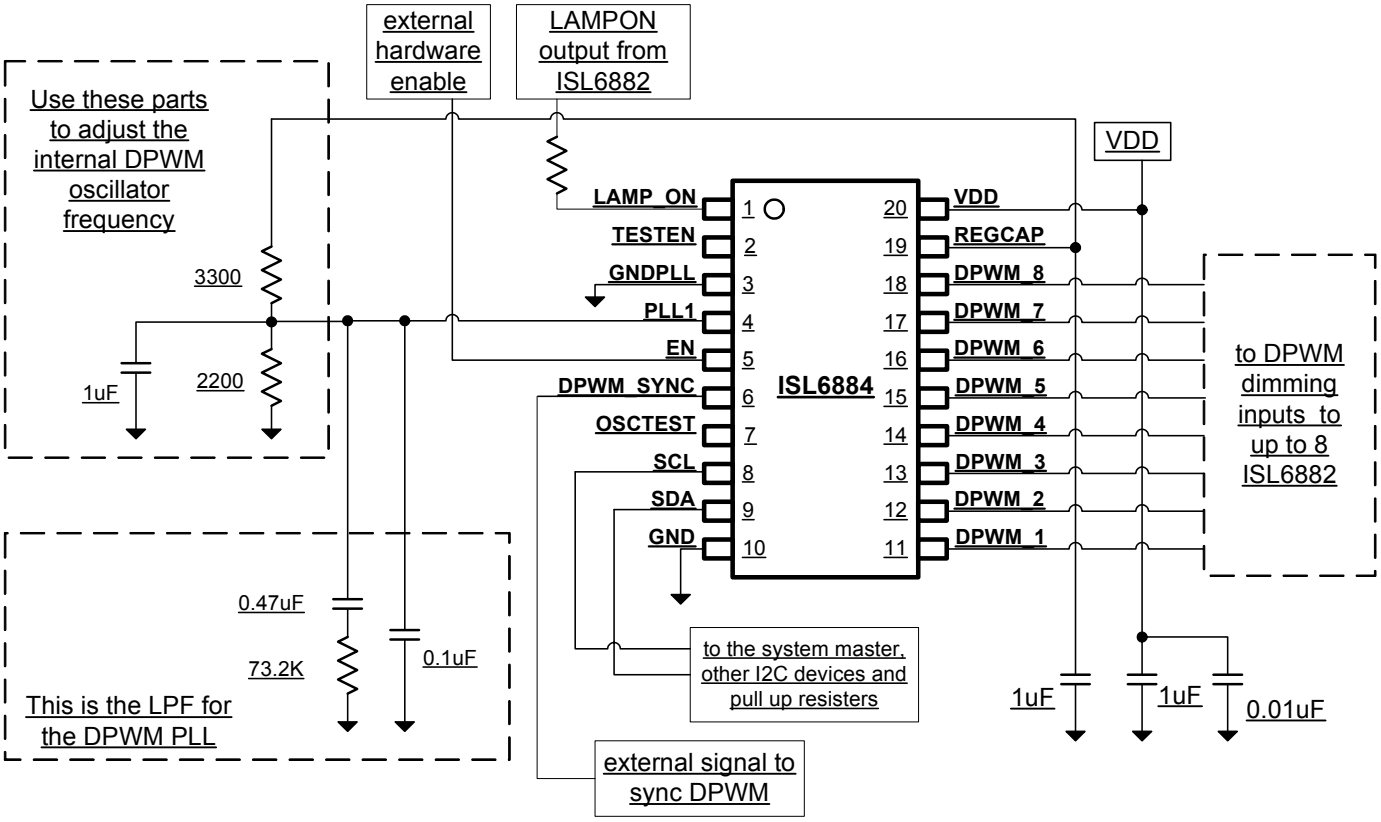
Block Diagram



Simplified System Diagram - Central Controller and Multiple Local Controllers



ISL6884 Application Schematic



Absolute Maximum Ratings

Supply Voltage (VDD) . . . . . -0.3V to 6.0V
Input/Output Voltage . . . . . -0.3V to VDD + 0.3V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to 85°C
Maximum Operating Junction Temperature . . . . . 125°C
Supply Voltage, VDD . . . . . 5V ±10%

Thermal Information

Thermal Resistance (Typical, Notes 1)	θ_{JA} (°C/W)
20 Ld SSOP	110

Thermal Information

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER ON RESET						
VDD Rising	POR_{rising}		2.4	2.7	3.0	V
VDD Falling	$POR_{falling}$		2.2	2.5	2.7	V
POR Hysteresis	POR_{hyst}		-	200	-	mV
VOLTAGE REGULATOR						
Regulated Voltage	V_{reg}	External Capacitor = 1µF, ESR<1Ω	2.3	2.5	2.7	V
LOGIC LEVEL INPUTS (EN, DPWM_SYNC, LAMPON)						
V In High	VIH_{LOGIC}		2.6	-	-	V
V In Low	VIL_{LOGIC}		-	-	0.8	V
Hysteresis	Vhyst		-	140	-	mV
Input Current	$I_{\_IN}$	V_{in} = VDD	-	10	-	nA
		V_{in} = 0V	-	-10	-	nA
I^2C						
V In Low	V_{IL}		-	-	0.3*VDD	V
V In High	V_{IH}		0.7*VDD	-	-	V
Schmitt Trigger Input Hysteresis	V_{hys}		-	0.05*VDD	-	V
V Out Low	V_{OL}	I in low = 3mA	-	-	0.4	V
SDA, SCL Rise Time	T_{rise_I2C}	Cload = 200pF Rpullup = 1700, 30%-70%	-	300	-	ns
SDA, SCL Fall Time	T_{fall_I2C}	Cload = 200pF Rpullup = 1700, 30%-70%	-	-	300	ns

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DPWM						
DPWM PLL Free Run Frequency	$f_{freerun}$		-	160	-	Hz
DPWM PLL Lock Frequency	f_{lock}		120	160	200	Hz
Lock Time	T_{lock}		-	150	-	ms
DPWM Duty Cycle	$DPWM_{DCmin}$	BRT_M = 00hex (Note 3)	3	4	5	%
DPWM Duty Cycle	$DPWM_{DCmid}$	BRT_M = 7Fhex (Note 3)	49	50	51	%
DPWM Duty Cycle	$DPWM_{DCmax}$	BRT_M = FFhex (Note 3)	98	-	100	%
DPWM Output High	V_{OH}	I_{OH} = 2mA	0.7*VDD	-	-	V
DPWM Output Low	V_{OL}	I_{OL} = 2mA	-	-	0.3*VDD	V
DPWM Rise Time	T_{rise_DPWM}	Cload = 200pF	-	-	500	ns
DPWM Fall Time	T_{fall_DPWM}	Cload = 200pF	-	-	500	ns

NOTE:

2. Master enable (0X2B) = 01, channel enable (0X2C) = FF, all other registers in default mode

Pin Description

VDD - Power input for digital systems. All functions are disabled unless this pin exceeds 3V (see Power On Reset specs). A 0.01µF decoupling cap should be placed between VDD and GND with the shortest possible traces.

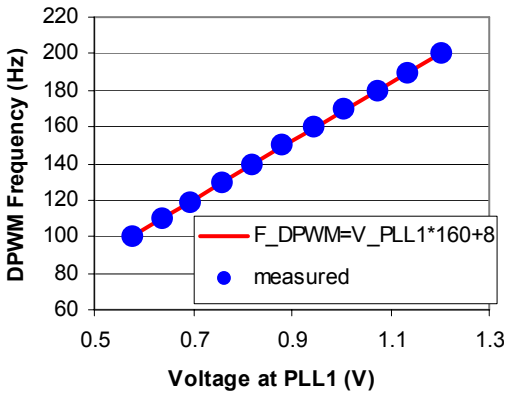
GND - Ground for digital systems.

REGCAP - An external 1µF capacitor to decouple the internal 2.5V regulator.

EN - Logic level input signal. Voltage at this pin above a threshold ENables circuit operation.

DPWM SYNC - A logic level input signal. The dimming PWM frequency oscillator will synchronize to this signal (if present). If no signal is present at this pin, the internal DPWM oscillator will free run at approximately 160Hz.

PLL1 - Analog input. An RC network on these pins sets the loop response of the DPWM Phase Locked Loop. A voltage source or resister divider at this pin will set the DPWM frequency. See the graph below for approximate frequency vs voltage at PLL1.



GNDPLL - A separate ground terminal for the PLL. Filter and bias components on PLL1 should be connected to this ground with the shortest possible traces. This pin is also connected to the system ground with a trace that is not critical.

DPWM 1:8 - Logic level outputs that control the analog and PWM dimming of each of 8 ISL6882s. The duty cycle of the DPWM signals range from 4% (minimum brightness) to 100% (maximum brightness). A low pass filter in the inverter Controller converts the DPWM duty cycle to a DC voltage that performs 3:1 analog dimming. The combined dimming range is 100:1. The dimming value is set by I^2C registers.

LAMP_ON - A logic level input signal. A high level on the pin indicates that all lamps are ON and operating normally. A low level at this pin indicates that at least one of the lamps is either not ignited or out of the circuit. When this pin is low, the fault timer runs. When this pin is high, the fault timer is reset. Because this is a high impedance line that may be routed near sources of EMI, it is recommended that a 10K resister is placed in series between the LAMP_ON pin and all other circuits.

SDA, SCL - Logic level input/output signals. SDA is the I^2C data line and SCL is the I^2C clock line. The ISL6884 receives data via I^2C to enable or disable the inverters, set dimming for each channel, and set the number of channels. System status can be read via I^2C.

TESTEN and OSCTEST - These pins are used for internal tests. They should be left unconnected in normal operation.

I^2C Register Description

Register addresses and default values are given in the following Register Description Table.

I^2C Slave Address - ISL6884's slave address is:

- 1101_1111 for reading
- 1101_1110 for writing

BRT_M - Master Brightness Control input. This register controls the duty cycle of al 8 DPWM outputs.

BRT_OS[1..8] - Brightness offset. These registers allow the system designer to increase or decrease the duty cycle of individual channel to equalize the brightness of all lamps in a system. Note: Value is stored as 2's complement number.

MSTR_EN - Master Enable, This signal is AND'ed with the EN pin to create the enable for the PWM dimming output. If this bit OR the EN pin is low the DPWM outputs are held low.

CH_EN - Individual Channel Enables for each DPWM output. If only DPWM 1, 3, 5 and 7 are to be used, CH_EN bits 1, 3, 5, and 7 should be set to 1 and bits 2, 4, 6, and 8 should be set to 0.

FLT_TOUT - Fault Timer Time Out Setting. This register controls the response of the ISL6884 to a logic low input on the LAMPON pin (indicating that one or more lamps is NOT ON). A value between 0X01 and 0XFF in the FLT_TOUT register will set the time that ISL6884 will operate with a low signal at the LAMPON pin (fault time out). The adjustment range is from less than 0.1 second to approximately 2 seconds. The power on reset default time out is 1 second. After a fault time out, all DPWM outputs are latched low until power is cycled. If FLT_TOUT is set to 0X00, ISL6884 will not time out and will continue to operate even with a low signal at the LAMPON pin.

STATUS - indicates the status of the Time out Fault, LAMPON input signal and ENABLE (MSTR_EN AND EN pin).

Register Description Table

Register Descriptions:

NOTES:

1. sb denotes sign bit for 2's compliment numbers.
2. The second row shows the register's default value loaded at Power On Reset.

TABLE 1. REGISTER DESCRIPTION TABLE (READ/WRITE REGISTERS)

WORD NAME	DESCRIPTION							
BYTE ADDRESS	MSB LABEL	BIT 6 LABEL	BIT 5 LABEL	BIT 4 LABEL	BIT 3 LABEL	BIT 2 LABEL	BIT 1 LABEL	LSB LABEL
POR	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE
BRT_M	Brightness Magnitude Setting							
0x00	b7	b6	b5	b4	b3	b2	b1	b0
POR	0	0	1	1	1	1	1	1
brt_os1	Brightness Offset for Light Sensor 1. Note: Value is stored as 2's complement number							
0x01			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os2	Brightness Offset for Light Sensor 2. Note: Value is stored as 2's complement number.							
0x02			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os3	Brightness Offset for Light Sensor 3. Note: Value is stored as 2's complement number							
0x03			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os4	Brightness Offset for Light Sensor 4. Note: Value is stored as 2's complement number.							
0x04			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os5	Brightness Offset for Light Sensor 5. Note: Value is stored as 2's complement number							
0x05			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os6	Brightness Offset for Light Sensor 6. Note: Value is stored as 2's complement number.							
0x06			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os7	Brightness Offset for Light Sensor 7. Note: Value is stored as 2's complement number.							
0x07			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
brt_os8	Brightness Offset for Light Sensor 8. Note: Value is stored as 2's complement number.							
0x08			sb	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
mstr_en	Master Enable, This signal is AND'ed with the en pin to create the enable for the PWM dimming output.							
0x2a								mstr_en
POR	0	0	0	0	0	0	0	0
ch_en	Individual Channel Enables for each DPWM output.							
0x2b	b7	b6	b5	b4	b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0
flt_tout	Fault Timer Time Out Setting.							

TABLE 1. REGISTER DESCRIPTION TABLE (READ/WRITE REGISTERS) (Continued)

WORD NAME	DESCRIPTION							
BYTE ADDRESS	MSB LABEL	BIT 6 LABEL	BIT 5 LABEL	BIT 4 LABEL	BIT 3 LABEL	BIT 2 LABEL	BIT 1 LABEL	LSB LABEL
POR	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE
0x2c	b7	b6	b5	b4	b3	b2	b1	b0
POR	1	0	0	0	0	0	0	0
CM	Maximum Fails Setting. This value determines how many consecutive I^2C fails can occur before channel is faulted.							
0x2d							b1	b0
POR	0	0	0	0	0	0	0	1
i^2c_suh _pres	I^2C Setup/Hold Preset Value. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x2E			b5	b4	b3	b2	b1	b0
POR	0	0	0	0	0	1	1	0
i^2c_scl _hpres	I^2C SCL High Time Preset Value. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x2f			b5	b4	b3	b2	b1	b0
POR	0	0	0	0	0	1	0	0
i^2c_scl_ lpres	I^2C SCL Low Time Preset Value. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x30			b5	b4	b3	b2	b1	b0
POR	0	0	0	1	0	0	1	0
i^2c_bfree	I^2C Bus Free Time Value. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x31			b5	b4	b3	b2	b1	b0
POR	0	0	0	0	1	0	1	1
i^2c _stretch	I^2C Stretch Value. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x32								i2c_stretch
POR	0	0	0	0	0	0	0	0
toc_spd _ctrl	Time Out Counter Speed Control. See I^2C Document for description **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x33						b18	b17	b16
POR	0	0	0	0	0	0	0	0
toc_spd _ctrl	Time Out Counter Speed Control. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x34	b15	b14	b13	b12	b11	b10	b9	b8
POR	1	1	1	0	0	1	1	1
toc_spd _ctrl	Time Out Counter Speed Control. See I^2C Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x35	b7	b6	b5	b4	b3	b2	b1	b0
POR	0	0	1	1	1	0	0	0
dc_max	Duty Cycle Maximum Setting. See DPWM Document for description **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x36	b7	b6	b5	b4	b3	b2	b1	b0
POR	1	1	1	1	1	1	1	1
dc_min	Duty Cycle Minimum Setting. See DPWM Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							

TABLE 1. REGISTER DESCRIPTION TABLE (READ/WRITE REGISTERS) (Continued)

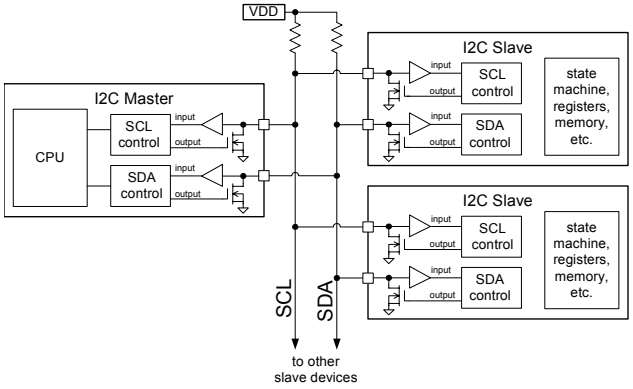
WORD NAME	DESCRIPTION							
BYTE ADDRESS	MSB LABEL	BIT 6 LABEL	BIT 5 LABEL	BIT 4 LABEL	BIT 3 LABEL	BIT 2 LABEL	BIT 1 LABEL	LSB LABEL
POR	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE	POR VALUE
0x37	b7	b6	b5	b4	b3	b2	b1	b0
POR	0	0	0	0	1	0	0	1
pwm_ sync_sel	PWM Sync Mode Select. PWM_SYNC_SEL = xxxxxx00: INTERNAL ONLY. DPWM frequency set by an internal oscillator. External DPWM_SYNC is ignored. PWM_SYNC_SEL = xxxxxx01: AUTOMATIC SYNC SELECT. DPWM frequency set by an external DPWM_SYNC signal if it is present or by the internal oscillator if no external signal is present. PWM_SYNC_SEL = xxxxxx10: EXTERNAL ONLY. DPWM frequency set by an external signal at DPWM_SYNC. No signal at DPWM_SYNC results in no DPWM output switching.							
0x38							pwm_sync _sel2	pwm_sync _sel1
POR	0	0	0	0	0	0	0	1
pll_bypass pmp1 pmp0	Bypass PLL bit = 1 forces DPWM frequency to an internal oscillator. Charge Pump Bit1. See Plan 9 CDR Document for description. Charge Pump Bit0. See Plan 9 CDR Document for description. **Caution! Changing this register from its default value may result in unpredictable behavior**							
0x39						pll_bypass	pmp1	pmp0
POR	0	0	0	0	0	0	0	0
Mux Selection for test mode mux. If the part is in test mode, the decode of this value changes the following pins:mx_sel = 0: dpwm6, dpwm7, dpwm8 in functional mode. mx_sel = 1: dpwm6 = vco_out, dpwm7 = div512_out, dpwm8 = div64_clk. mx_sel = 2: dpwm6 in functional mode, dpwm7 = clk_d4, dpwm8 = dpwm_clk. **Caution! Changing this register from its default value may result in unpredictable behavior**								
0x3A					mx_sel b3	b2	b1	b0
POR	0	0	0	0	0	0	0	0

I²C Bus General Description

Introduction

(Refer to Philips I²C Specification, Rev. 2.1)

The I²C bus is a 2 wire communication bus for integrated circuits. I²C, I2C or IIC are commonly used instead of the formal name ***I***nter-***I***ntegrated-***C***ircuit bus. The 2 wires are the SCL (***S***erial ***CL***ock) and SDA (***S***erial ***DA***ta). All ICs on the bus are connected to the SCL and SDA lines. SCL and SDA pins on each device are bidirectional and can act as either inputs or open drain outputs. Which device is transmitting and receiving is determined by the bus protocol which will be described below.



A typical I²C bus system is made of a ‘master’ that initiates communication (usually a microprocessor) and one or more ‘slaves’ that respond to commands from the master. Each slave has a device address. In a typical communication sequence, the master will initiate communication with a ‘start condition’ followed by the address of one of the slave devices. The slave device must acknowledge that it recognizes its address. After receiving the acknowledge, the master will transmit one or more bytes of commands and data. If the slave device is an EEPROM the command is the address within the EEPROM that is to be read or written. If data is to be written to the EEPROM the master transmits it after the command.

START and STOP Conditions

As shown in Figure 1, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

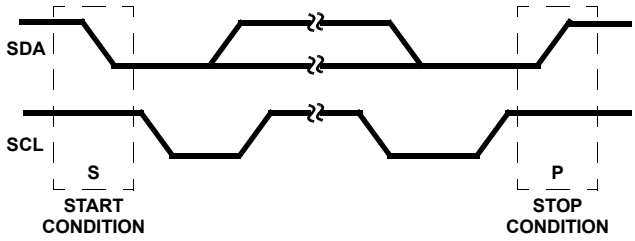


FIGURE 1. START AND STOP WAVEFORMS

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 2.

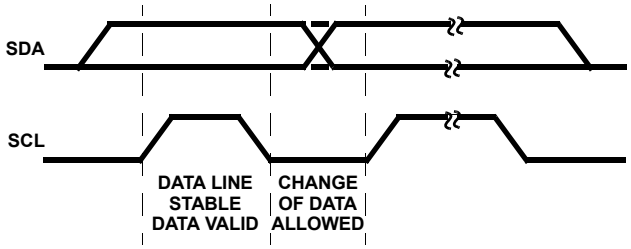


FIGURE 2. DATA VALIDITY

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (Figure 3). The peripheral that acknowledges has to pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Of course, set-up and hold times must also be taken into account.)

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

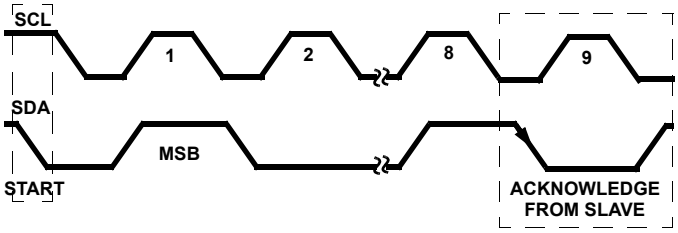
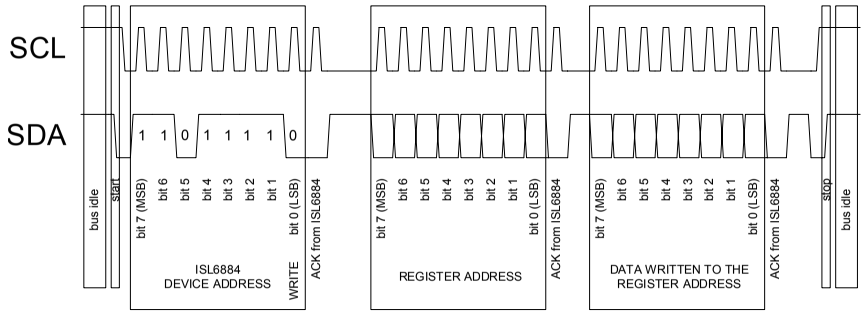


FIGURE 3. ACKNOWLEDGE ON THE I²C BUS

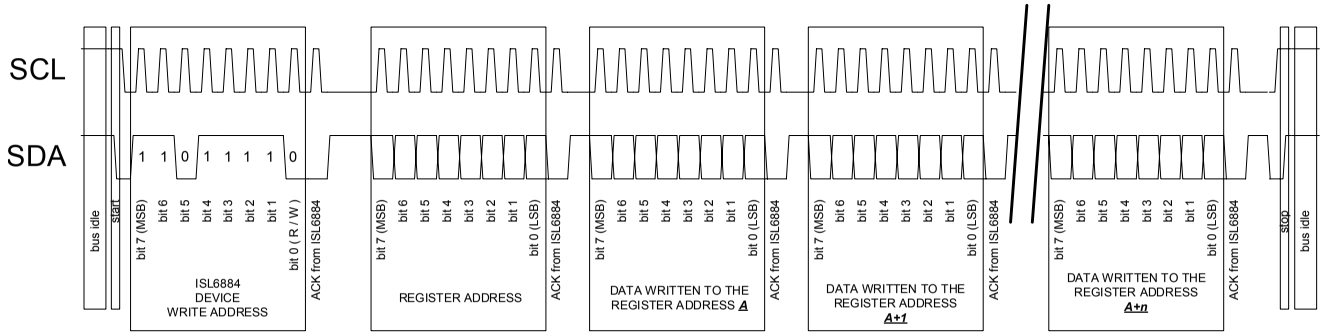
I^2C Transactions Between the System Master and the ISL6884

Below are typical transactions between the system master and the ISL6884.

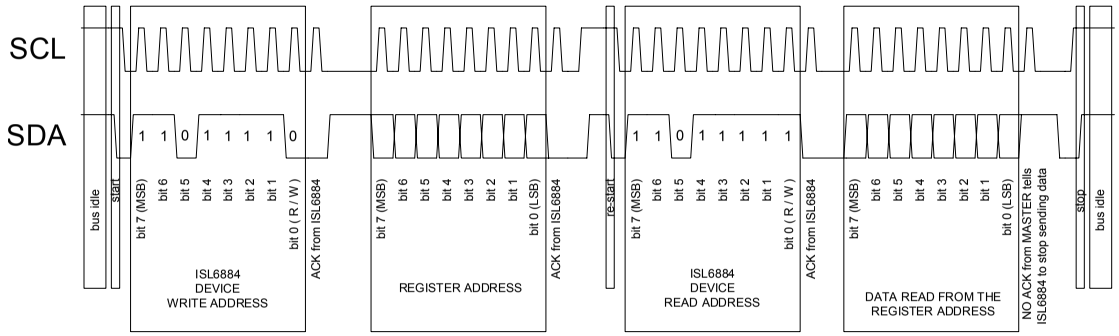
WRITING TO ONE REGISTER IN ISL6884



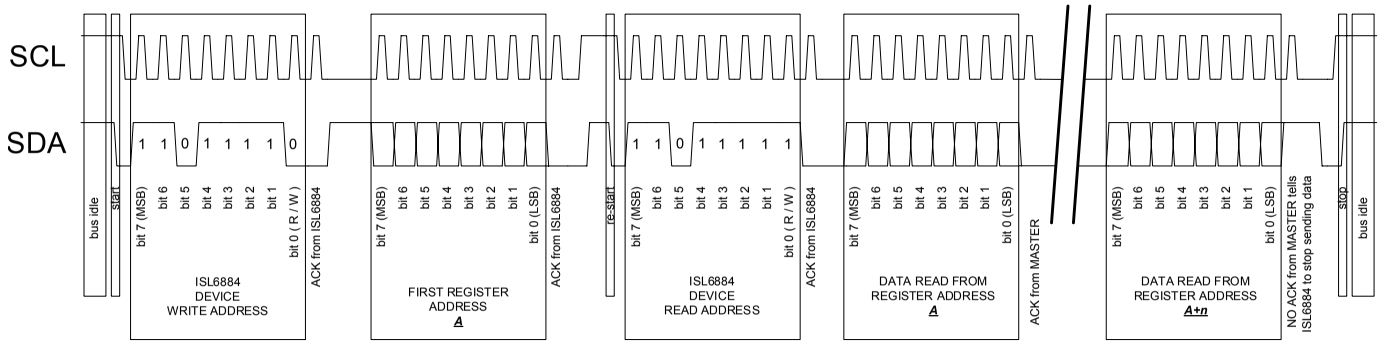
WRITING N CONSECUTIVE REGISTERS TO ISL6884



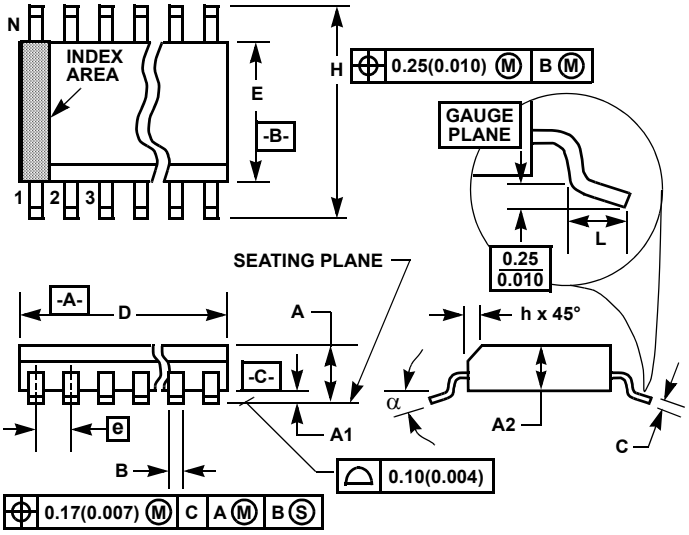
READING ONE REGISTER IN ISL6884



READING CONSECUTIVE REGISTER FROM ISL6884



Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M20.15

20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.337	0.344	8.56	8.74	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

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