Single Event and Total Dose Hardened, High-Speed, Dual Output PWMs

IS-1825ASRH, IS-1825ASEH, ISL71823ASRH

The single event and total dose hardened IS-1825ASRH, IS-1825ASEH and ISL71823ASRH pulse width modulators are designed to be used in high frequency, switching power supplies in either voltage or current-mode configurations. Both designs include a precision voltage reference, a low power start-up circuit, a high frequency oscillator, a wide-band error amplifier and a fast current-limit comparator.

The IS-1825ASRH, IS-1825ASEH features dual, alternating outputs operating from zero to less than 50% duty-cycle, while the ISL71823ASRH features dual, in-phase outputs operating from zero to less than 100% duty cycle.

Constructed with the Intersil Rad-hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide a high level of immunity to single event transients. All specified parameters are guaranteed and tested for 300krad(Si) total dose performance.

Detailed Electrical Specifications for these devices are contained in SMD 5962-02511. A "hot-link" is provided on our website for downloading the SMD.

Features

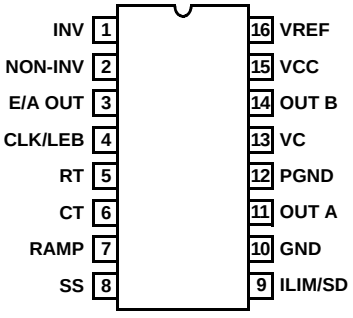
- Electrically Screened to DLA SMD # 5962-02511
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - Total Dose . . . . . 300krad(Si) (max)
  - Latch-up Immune. . . . . Dielectrically Isolated
  - SEU immune. . . . . LET = 35MeV/mg/cm^2(max)
- Oscillator Frequency . . . . . 1MHz(max)
- High Output Drive Current. . . . . 1A peak(typ)
- Low Start-up Current . . . . . 300µA(max)
- Undervoltage Lockout
  - Start Threshold. . . . . 8.8V(max)
  - Stop Threshold . . . . . 7.6V(min)
  - Hysteresis . . . . . 300mV(min)
- Improved Soft-Start Function Compared with Commercial 1825A/1823A Types
- Pulse-by-Pulse Current Limiting
- Latched Overcurrent Comparator with Full Cycle Restart
- Programmable Leading Edge Blanking

Applications

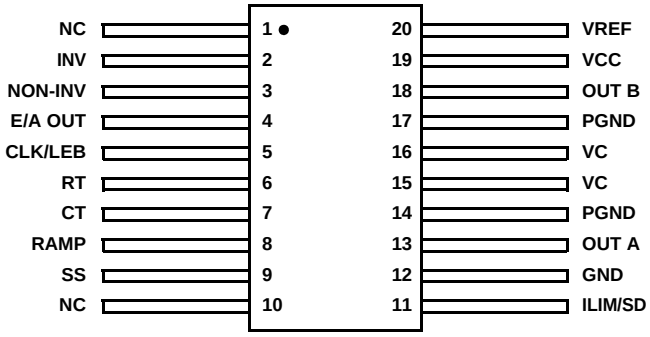
- Voltage or Current-Mode Switching Power Supplies
- Control of High Current MOSFET Drivers
- Motor Speed and Direction Control

Pin Configurations

IS1-1825ASRH, IS1-1825ASEH, ISL71823ASRHQD
(CDIP2-T16 SBDIP)
TOP VIEW



IS9-1825ASRH, IS9-1825ASEH, ISL71823ASRHQF
(CDFP4-F20 FLATPACK)
TOP VIEW



Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG DWG. #
IS0-1825ASRH/SAMPLE	IS0-1825ASRH/SAMPLE	-50 to +125		
5962F0251101V9A	IS0-1825ASRH-Q	-50 to +125		
5962F0251102V9A	IS0-1825ASEH-Q	-50 to +125		
5962F0251101QEC	IS1-1825ASRH-8	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101QXC	IS9-1825ASRH-8	-50 to +125	20 Ld Flatpack	K20.A
5962F0251101VEC	IS1-1825ASRH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102VEC	IS1-1825ASEH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101VXC	IS9-1825ASRH-Q	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102VXC	IS9-1825ASEH-Q	-50 to +125	20 Ld Flatpack	K20.A
IS1-1825ASRH/Proto	IS1-1825ASRH/Proto	-50 to +125	16 Ld SBDIP	D16.3
IS9-1825ASRH/Proto	IS9-1825ASRH/Proto	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102QEC	ISL71823ASRHQD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102QXC	ISL71823ASRHQF	-50 to +125	20 Ld Flatpack	K20.A
5962F0251102VEC	ISL71823ASRHVD	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102VXC	ISL71823ASRHVF	-50 to +125	20 Ld Flatpack	K20.A
ISL71823ASRHD/Proto	ISL71823ASRHD/Proto	-50 to +125	16 Ld SBDIP	D16.3
ISL71823ASRHF/Proto	ISL71823ASRHF/Proto	-50 to +125	20 Ld Flatpack	K20.A

NOTE:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Typical Performance Curves

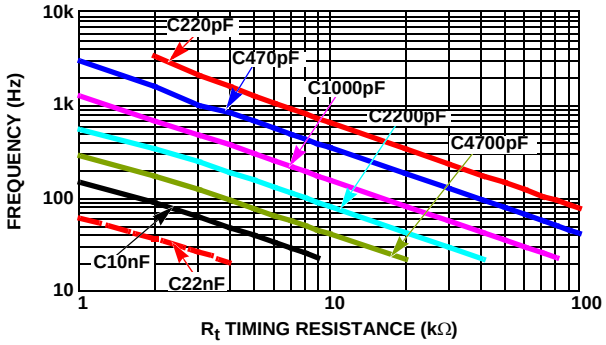


FIGURE 1. OSCILLATOR FREQUENCY vs R_t and C_t

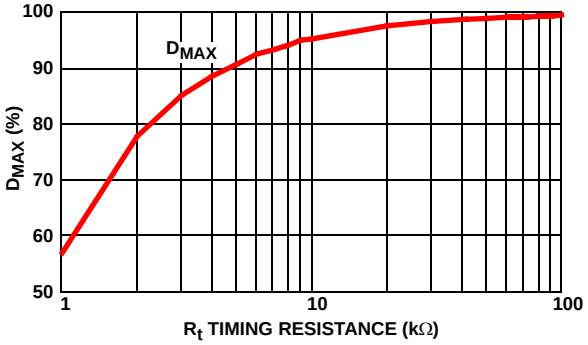


FIGURE 2. MAXIMUM DUTY CYCLE vs R_t

Die Characteristics

DIE DIMENSIONS:

4310µm x 5840µm (170 mils x 230 mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kA ± 1.0kA

Top Metallization

Type: AlSiCu
Thickness: 16.0kA ± 2kA

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density:

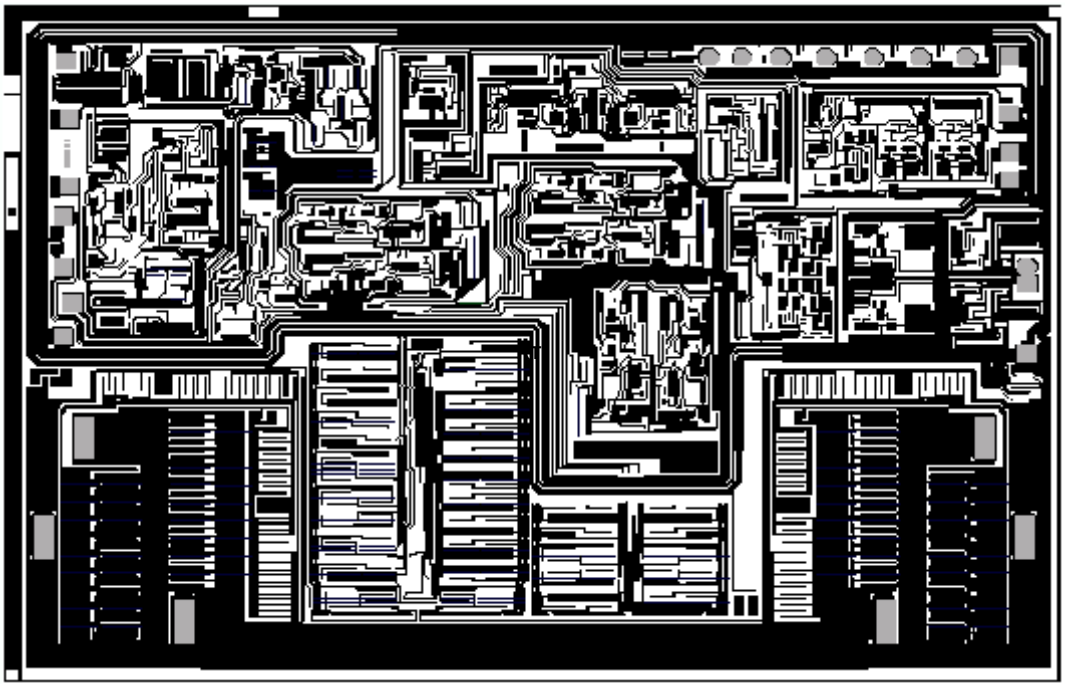
$<2.0 \times 10^5$ A/cm^2

Transistor Count:

585

Metallization Mask Layout

IS-1825ASRH, IS-1825ASEH, ISL71823ASRH



Notes:

1. Both the OGND (oscillator ground) and the GND (control circuit ground) pads must be bonded to ground. These pads are both bonded to the GND pin on the packaged devices.
2. All double-sized bond pads must be double bonded for current sharing purposes.