

**Radiation Hardened Full Bridge N-Channel FET Driver**

The HS-4080ARH is a monolithic, high frequency, medium voltage Full Bridge N-Channel FET Driver IC. The device includes a TTL-level input comparator, which can be used to facilitate the “hysteresis” and PWM modes of operation. Its HEN (high enable) lead can force current to freewheel in the bottom two external power MOSFETs, maintaining the upper power MOSFETs off. The HS-4080ARH is well suited for use in distributed DC power supplies and DC to DC converters, since it can switch at high frequencies.

These devices can also drive medium voltage motors, and two HS-4080ARHs can be used to drive high performance stepper motors, since the short minimum “on-time” can provide fine micro-stepping capability.

Short propagation delays maximize control loop crossover frequencies and dead-times, which can be adjusted to near zero to minimize distortion, resulting in precise control of the driven load.

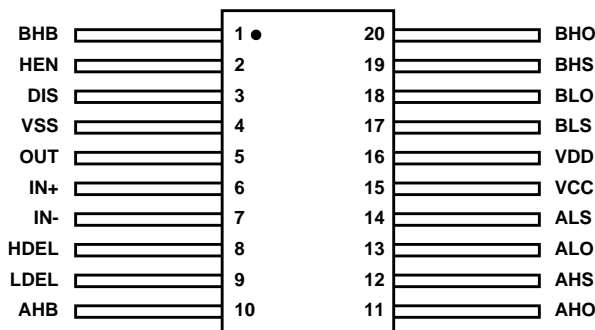
Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) process, these devices are immune to Single Event Latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments. Complete your design with radiation hardened MOSFETs from Intersil.

**Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.**

**Detailed Electrical Specifications for these devices are contained in SMD 5962-99617. A “hot-link” is provided on our homepage for downloading.**  
<http://www.intersil.com/spacedefense/space.htm>

**Pinout**

**HS-4080ARH (FLATPACK, CDFFP3-F20)**  
 TOP VIEW



**Features**

- Electrically Screened to SMD # 5962-99617
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - Gamma Dose . . . . . 300kRAD(Si) (Max)
  - Latch-up Immune RSG DI Process
- Drives N-Channel FET Full Bridge Including High Side Chop Capability
- Bootstrap Supply Max Voltage to 95V<sub>DC</sub>
- TTL Comparator Input Levels
- Drives 1000pF Load with Rise and Fall Times of 50ns
- User-Programmable Dead Time
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- DIS (Disable) Pin Pulls Gates Low
- Operates From Single Supply . . . . . 12V to 18V
- Low Power Consumption
- Undervoltage Protection

**Applications**

- Full Bridge Power Supplies
- PWM Motion Control

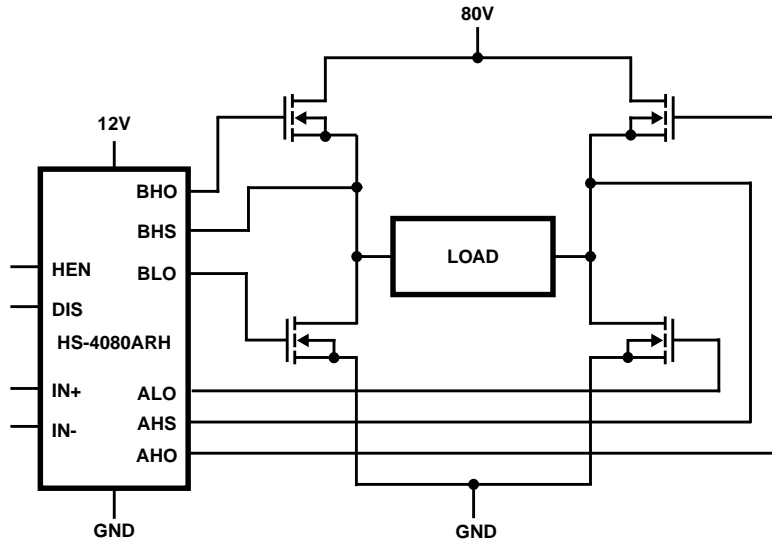
**Ordering Information**

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F9961701VSC	HS9-4080ARH-Q	-55 to 125
5962F9961701QSC	HS9-4080ARH-8	-55 to 125
HS9-4080ARH/Proto	HS9-4080ARH/Proto	-55 to 125

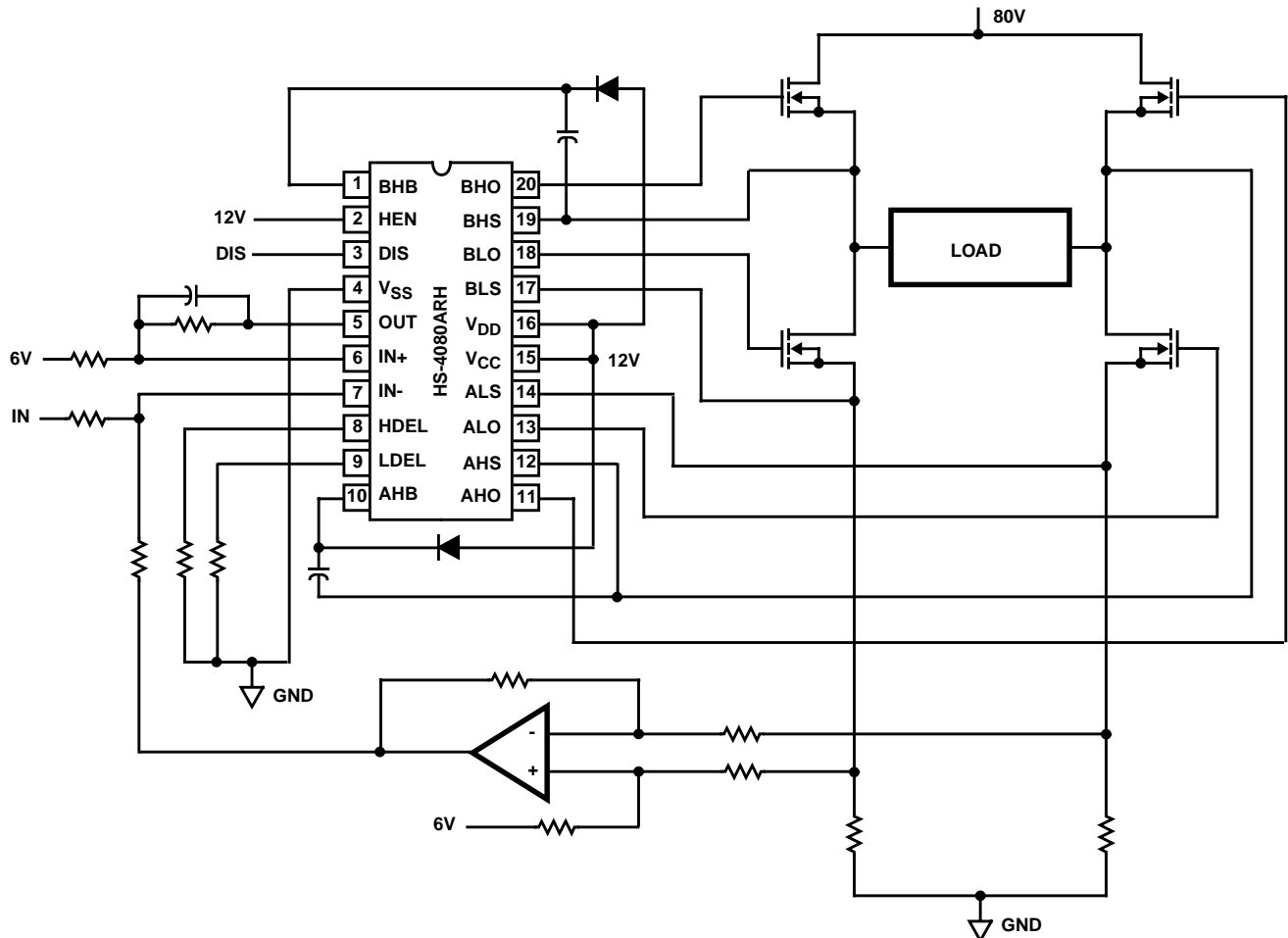
**HS-4080ARH Preliminary Pin Descriptions**

PIN NUMBER	SYMBOL	DESCRIPTION
1	BHB	B High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of boot-strap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 50µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 15V.
2	HEN	High-side Enable input. Logic level input that when low overrides IN+/IN- (Pins 6 and 7) to put AHO and BHO drivers (Pins 11 and 20) in low output state. When HEN is high AHO and BHO are controlled by IN+/IN- inputs. The pin can be driven by signal levels of 0V to 18V (no greater than V <sub>DD</sub> ). An internal 100µA pull-up to V <sub>DD</sub> will hold HEN high, so no connection is required if high-side and low-side outputs are to be controlled by IN+/IN- inputs.
3	DIS	DISable input. Logic level input that when taken high sets all four outputs low. DIS high overrides all other inputs. When DIS is taken low the outputs are controlled by the other inputs. The pin can be driven by signal levels of 0V to 18V (no greater than V <sub>DD</sub> ). An internal 100µA pull-up to V <sub>DD</sub> will hold DIS high if this pin is not driven.
4	V <sub>SS</sub>	Chip negative supply, generally will be ground.
5	OUT	OUTput of the input control comparator. This rail to rail output signal can be used for feedback and hysteresis.
6	IN+	Noninverting input of control comparator. This pin can only be driven by signal levels of 0V to 5.5V. If IN+ is greater than IN- (Pin 7) then ALO and BHO are low level outputs and BLO and AHO are high level outputs. If IN+ is less than IN- then ALO and BHO are high level outputs and BLO and AHO are low level outputs. DIS (Pin 3) high level will override IN+/IN- control for all outputs. HEN (Pin 2) low level will override IN+/IN- control of AHO and BHO. When switching in four quadrant mode, dead time in a half bridge leg is controlled by HDEL and LDEL (Pins 8 and 9).
7	IN-	Inverting input of control comparator. This pin can only be driven by signal levels of 0V to 5.5V. See IN+ (Pin 6) description.
8	HDEL	High-side turn-on DELay. Connect resistor from this pin to V <sub>SS</sub> to set timing current that defines the turn-on delay of both high-side drivers. The low-side drivers turn-off with no adjustable delay, so the HDEL resistor guarantees no shoot-through by delaying the turn-on of the high-side drivers. HDEL reference voltage is approximately 5.1V.
9	LDEL	Low-side turn-on DELay. Connect resistor from this pin to V <sub>SS</sub> to set timing current that defines the turn-on delay of both low-side drivers. The high-side drivers turn-off with no adjustable delay, so the LDEL resistor guarantees no shoot-through by delaying the turn-on of the low-side drivers. LDEL reference voltage is approximately 5.1V.
10	AHB	A High-side Bootstrap supply. External bootstrap diode and capacitor are required. Connect cathode of boot-strap diode and positive side of bootstrap capacitor to this pin. Internal charge pump supplies 30µA out of this pin to maintain bootstrap supply. Internal circuitry clamps the bootstrap supply to approximately 15V.
11	AHO	A High-side Output. Connect to gate of A High-side power MOSFET.
12	AHS	A High-side Source connection. Connect to source of A High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
13	ALO	A Low-side Output. Connect to gate of A Low-side power MOSFET.
14	ALS	A Low-side Source connection. Connect to source of A Low-side power MOSFET.
15	V <sub>CC</sub>	Positive supply to gate drivers. Must be same potential as V <sub>DD</sub> (Pin 16). Connect to anodes of two bootstrap diodes.
16	V <sub>DD</sub>	Positive supply to lower gate drivers. Must be same potential as V <sub>CC</sub> (Pin 15). De-couple this pin to V <sub>SS</sub> (Pin 4).
17	BLS	B Low-side Source connection. Connect to source of B Low-side power MOSFET.
18	BLO	B Low-side Output. Connect to gate of B Low-side power MOSFET.
19	BHS	B High-side Source connection. Connect to source of B High-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
20	BHO	B High-side Output. Connect to gate of B High-side power MOSFET.

**Application Block Diagram**



**Typical Application (Hysteresis Mode Switching)**



**Die Characteristics**

**DIE DIMENSIONS:**

4760μm x 5660μm (188 mils x 223 mils)  
 Thickness: 483μm ±25.4μm (19 mils ±1 mil)

**INTERFACE MATERIALS:**

**Glassivation:**

Type: Phosphorus Silicon Glass  
 Thickness: 8.0kÅ ±1.0kÅ

**Top Metallization:**

Type: AlSiCu  
 Thickness: 16.0kÅ ±2kÅ

**Substrate:**

Radiation Hardened Silicon Gate,  
 Dielectric Isolation

**Backside Finish:**

Silicon

**ASSEMBLY RELATED INFORMATION:**

**Substrate Potential:**

Unbiased (DI)

**ADDITIONAL INFORMATION:**

**Worst Case Current Density:**

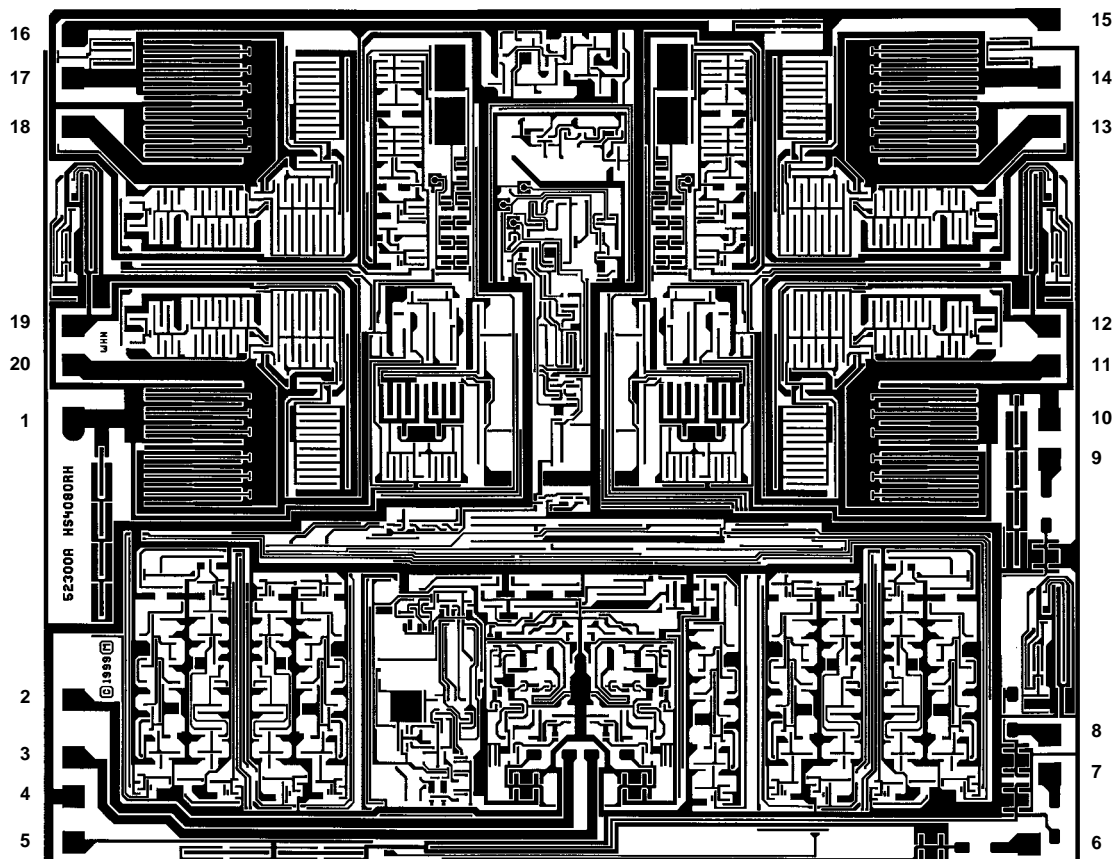
<2.0 x 10<sup>5</sup> A/cm<sup>2</sup>

**Transistor Count:**

432

**Metallization Mask Layout**

HS-4080ARH



All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

*Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see web site [www.intersil.com](http://www.intersil.com)