Data Sheet | August 2000 | File Number 4875

Radiation Hardened Complementary Switch FET Driver

The Radiation Hardened IS-1715ARH is a high speed, high current complementary power FET driver designed for use in synchronous rectification circuits. Soft switching transitions for the two output waveforms may be managed by setting the independently programmable delays. The delay pins can alternatively be configured for zero-voltage sensing to allow for precise switching control.

The IS-1715ARH has a single input, which is PWM and TTL compatible, and can run at frequencies up to 1MHz. The AUX output switches immediately at the rising edge of the INPUT, but waits for the T2 delay before responding to the falling edge. A logic low on the enable pin (ENBL) places both outputs into an active-low mode, and an under voltage lock-out (UVLO) function is set at 9V(max).

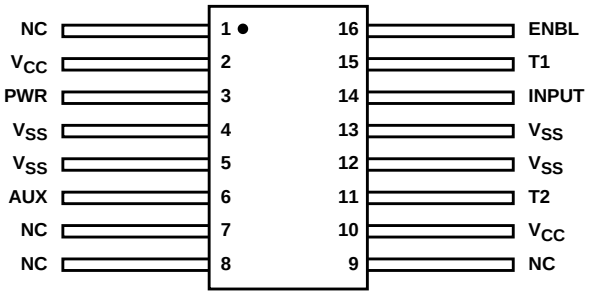
Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) process, these devices are immune to single event latch-up (SEL) and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-00521. A "hot-link" is provided on our homepage for downloading. http://www.intersil.com/spacedefense/space.htm

Pinout

IS9-1715ARH
FLATPACK (CDFP4-F16)
TOP VIEW



Features

- Electrically Screened to SMD # 5962-00521
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
  - Gamma Dose $3x10^5$ RAD(Si)
  - Latch-up Immune
- PWR Output Current (Source and sink) . . . . . 3A (peak)
- AUX Output Current (Source and sink) . . . . . 3A (peak)
- Low Operating Supply Current . . . . . 6mA (max)
- Wide Programmable Delay Range . . . . . 100ns to 600ns
- Configurable for Zero-Voltage Switching
- Switching Frequency to 1MHz
- Both Outputs Active-Low in Sleep Mode
- 9V(max) Under Voltage Lock-out

Applications

- Synchronous Rectification in Power Supplies

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^oC)
5962F0052101VXC	IS9-1715ARH-Q	-55 to 125
5962F0052101QXC	IS9-1715ARH-8	-55 to 125
IS9-1715ARH/Proto	IS9-1715ARH/Proto	-55 to 125

Die Characteristics

DIE DIMENSIONS:

3559µm x 4420µm (129 mils x 174 mils)
Thickness: 483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization

Type: AlSiCu
Thickness: 16.0kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate,
Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density:

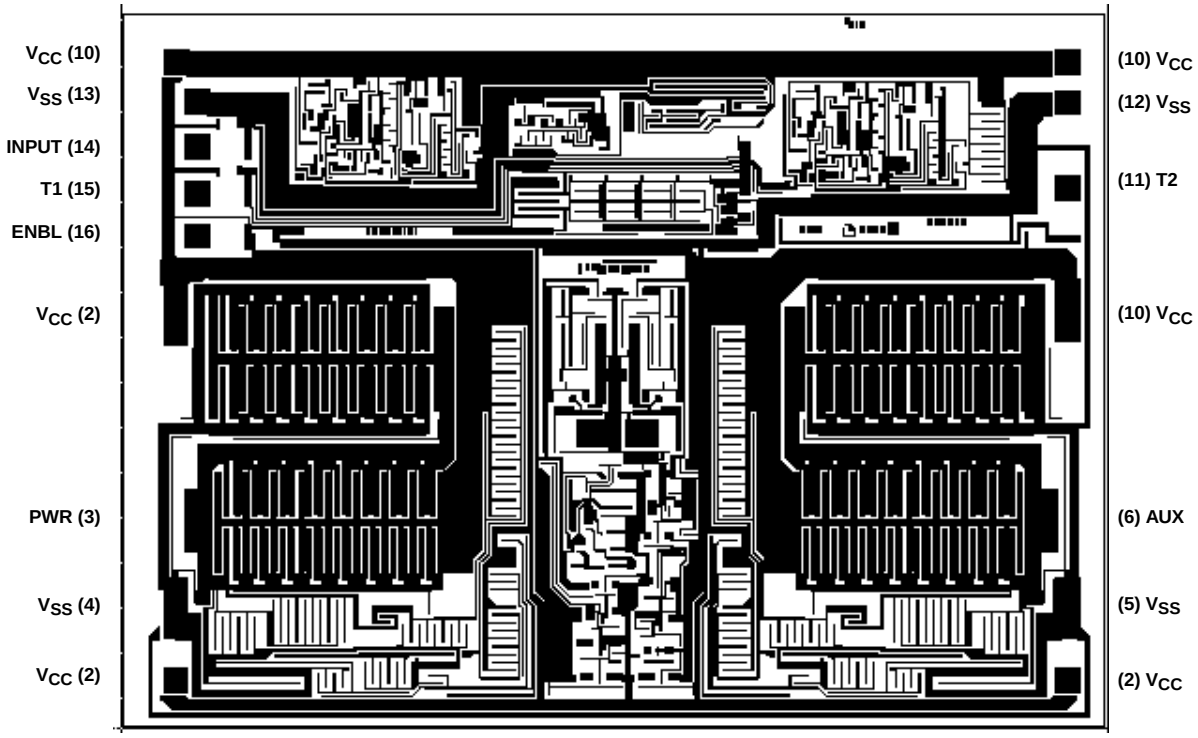
$<2.0 \times 10^5$ A/cm^2

Transistor Count:

222

Metallization Mask Layout

IS-1715ARH



NOTES:

1. All double sized pads should be double bonded.
2. All pin 2 and pin 10 VCC pads are bonded to VCC for power and noise considerations. (These are lead-frame connected in packaged devices.)