

Radiation Hardened Negative Low Dropout Adjustable Voltage Regulator

The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (I_{LIM}) and a shutdown pin (SD) for easy on/off control.

The device incorporates unique circuitry that enables precision performance over the -55°C to +125°C temperature range and post-irradiation. Specifications include a reference voltage of -1.25V +40mV/-50mV (max), line regulation of ±25mV (max), and load regulation of ±15mV (max).

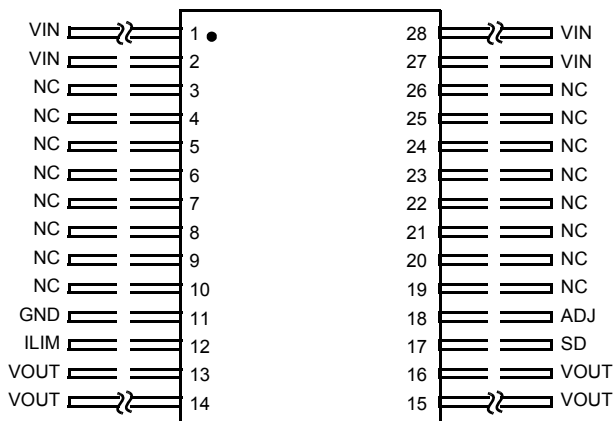
Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to Single Event Latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-02503. A 'hotlink' is provided on the Intersil website for downloading.

Pinout

ISL72991RHF (FLATPACK CDFP3-F28)
TOP VIEW



Features

- Electrically Screened to DSCC SMD # 5962-02503
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Environment
 - Total Dose (Max) 300krad(SI)
 - Latch-Up Immune
- Line Regulation ±25mV (max)
- Load Regulation ±12mV (typ); ±15mV (max)
- Output Voltage Range -2.25V to -26V
- Dropout Voltage (100mA) 0.2V (typ); 0.3V (max)
- Dropout Voltage (1A) 1V (max)
- Minimum Load Current 3.0mA
- TTL Input-Level Shutdown (SD); Low = On

Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)
5962F0250301VXC	ISL72991RHVF	-55 to 125
5962F0250301QXC	ISL72991RHQF	-55 to 125
5962F0250301V9A	ISL72991RHVX	-55 to 125
ISL72991RHF/Proto	ISL72991RHF/Proto	-55 to 125

Application Information

Typical User Application:

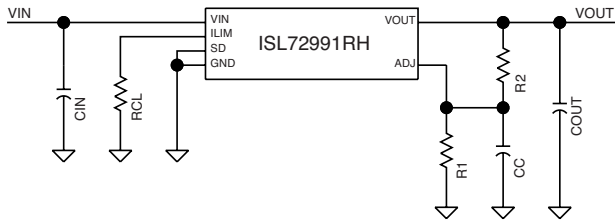


FIGURE 1. TYPICAL APPLICATION SCHEMATIC

Output Voltage Programming

The output voltage of the regulator can be programmed with two external resistors and is described by the following equation: $V_{OUT} = V_{REF} \times (1 + R2/R1) - (I_{ADJ} \times R2)$.

Output Current Limit Programming

The output current limit threshold of the regulator can be programmed with a single external resistor connected from I_LIM to ground. The current flowing into the I_LIM pin is described by the following equation: $I_{LIM} = 1V / (R_{CL} + 2400)$. The graph below shows the relationship between I_LIM and the output current limit threshold, I_OUT_LIM.

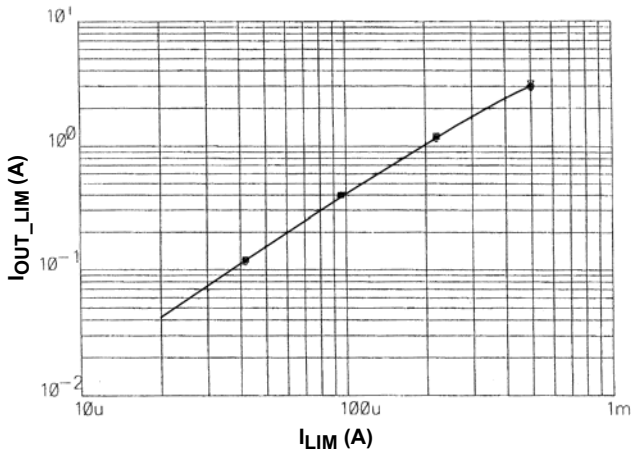


FIGURE 2. I_OUT_LIM vs I_LIM

Capacitor Selection

An input capacitor is required if the regulator is located more than 6 inches from power supply filter capacitors. A 10µF solid tantalum capacitor is recommended.

An output capacitor of at least 10µF must be used to insure stability of the regulator. Additional capacitance may be added as required to improve the dynamic response of the regulator. Solid tantalum and/or ceramic capacitors are recommended.

Loop Compensation

The output capacitor and ESR comprise a zero in the loop transfer function that must be compensated with a pole to insure loop stability in accordance with the following equation: $C_C \times R2 = C_{OUT} \times ESR$. The compensating capacitor should be a low ESR ceramic type.

Layout Guidelines

The stability of the regulator is sensitive to layout. It is strongly recommended that a continuous copper ground plane (1 ounce or greater) be used. In addition, component lead lengths and interconnects should be minimized, but should not exceed 1/2 inch. Finally, the return lead of the compensation capacitor (C_C) should be connected as close as possible to the GND pin of the IC.

Die Characteristics

DIE DIMENSIONS:

5870µm x 5210µm (231.1mils x 205.1mils)
 Thickness: 483µm ± 25.4µm (19mils ± 1mil)

INTERFACE MATERIALS:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
 Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization:

Type: AlSiCu
 Thickness: 16.0kÅ ± 2kÅ

Substrate:

Radiation Hardened Silicon Gate,
 Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

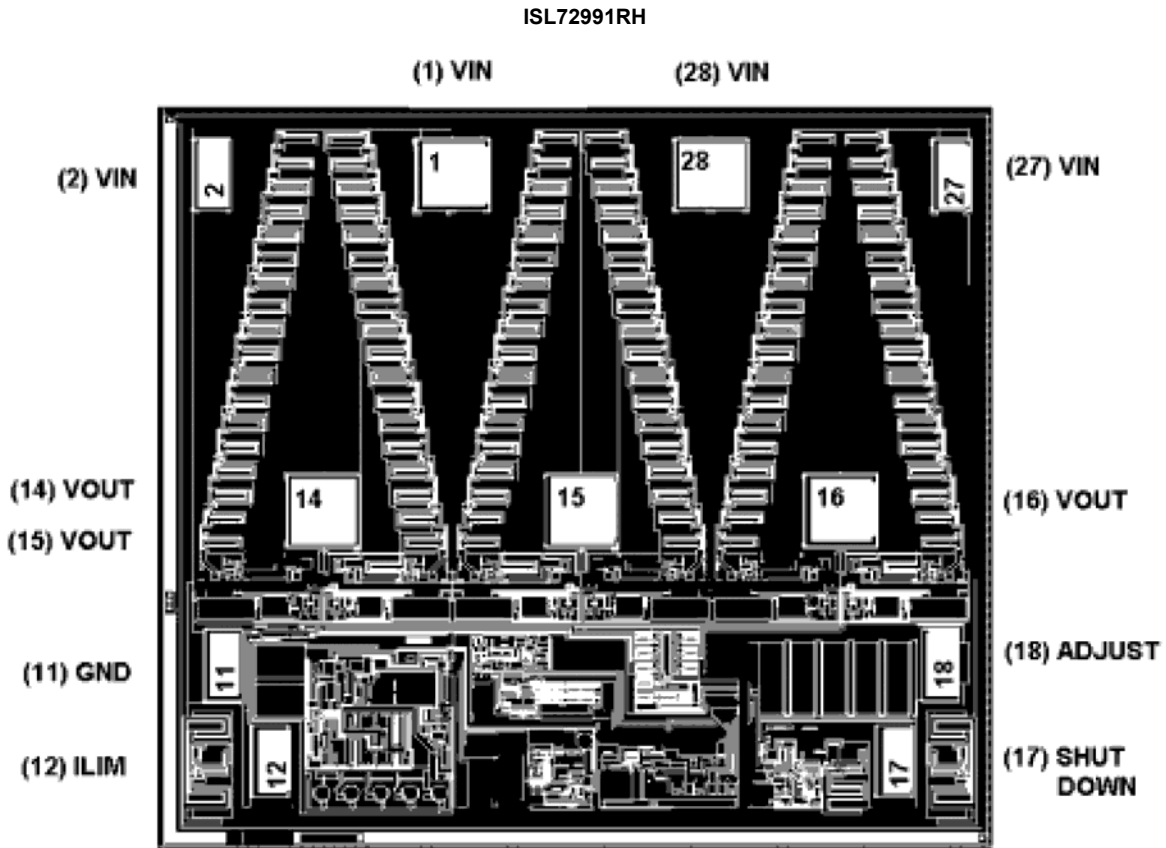
ADDITIONAL INFORMATION:

Worst Case Current Density:

<2.0 x 10⁵ A/cm²

Transistor Count:

Metallization Mask Layout



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
 Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com