TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1 GBIT (128M × 8 BIT) CMOS NAND E^2PROM

DESCRIPTION

The TC58NVG0S3E is a single 3.3V 1 Gbit (1,107,296,256 bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as (2048 + 64) bytes × 64 pages × 1024blocks.
The device has two 2112-byte static registers which allow program and read data to be transferred between the register and the memory cell array in 2112-byte increments. The Erase operation is implemented in a single block unit (128 Kbytes + 4 Kbytes: 2112 bytes × 64 pages).

The TC58NVG0S3E is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

FEATURES

- Organization

	x8
Memory cell array	2112 × 64K × 8
Register	2112 × 8
Page size	2112 bytes
Block size	(128K + 4K) bytes

- Modes
  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy,
  Multi Page Program, Multi Block Erase, Multi Page Copy, Multi Page Read

- Mode control
  Serial input/output
  Command control

- Number of valid blocks
  Min 1004 blocks
  Max 1024 blocks

- Power supply
  V_{CC} = 2.7V to 3.6V

- Access time

Cell array to register	25 μs max
Serial Read Cycle	25 ns min (CL=100pF)

- Program/Erase time

Auto Page Program	300 μs/page typ.
Auto Block Erase	2.5 ms/block typ.

- Operating current

Read (25 ns cycle)	30 mA max.
Program (avg.)	30 mA max
Erase (avg.)	30 mA max
Standby	50 μA max

- Package
  P-TFBGA63-0911-0.80CZ (Weight: 0.15 g typ.)

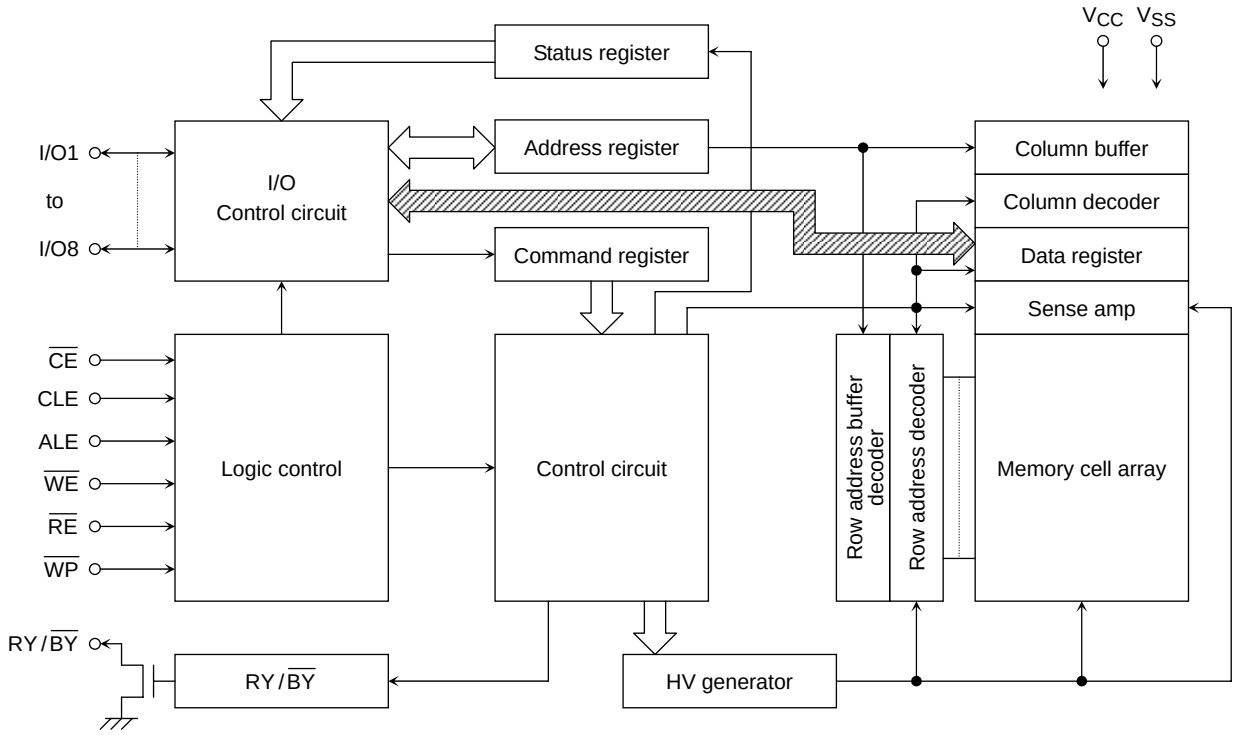
PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			$\overline{WP}$	ALE	V_{SS}	$\overline{CE}$	$\overline{WE}$	RY/$\overline{BY}$		
D			NC	$\overline{RE}$	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	NC	NC	NC	NC	NC		
H			NC	I/O1	NC	NC	NC	V_{CC}		
J			NC	I/O2	NC	V_{CC}	I/O6	I/O8		
K			V_{SS}	I/O3	I/O4	I/O5	I/O7	V_{SS}		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

PIN NAMES

I/O1 to I/O8	I/O port
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{RE}$	Read enable
CLE	Command latch enable
ALE	Address latch enable
$\overline{WP}$	Write protect
RY/$\overline{BY}$	Ready/Busy
V_{CC}	Power supply
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{CC}	Power Supply Voltage	−0.6 to 4.6	V
V_{IN}	Input Voltage	−0.6 to 4.6	V
$V_{I/O}$	Input /Output Voltage	−0.6 to V_{CC} + 0.3 (≤ 4.6 V)	V
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	℃
T_{STG}	Storage Temperature	−55 to 125	℃
T_{OPR}	Operating Temperature	-40 to 85	℃

CAPACITANCE *(Ta = 25℃, f = 1 MHz)

SYMB0L	PARAMETER	CONDITION	MIN	MAX	UNIT
C_{IN}	Input	V_{IN} = 0 V	—	10	pF
C_{OUT}	Output	V_{OUT} = 0 V	—	10	pF

* This parameter is periodically sampled and is not tested for every device.