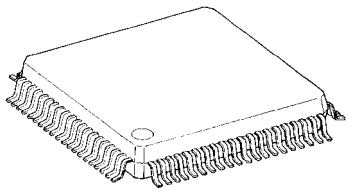
Preliminary TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90A58F

3-Channel AD Converter

The TC90A58F is a 3-channel AD converter for video applications which incorporates a clamp circuit.

The 10-bit converter can be used as either an 8-bit 3-channel AD converter or as a 10-bit 2-channel AD converter.



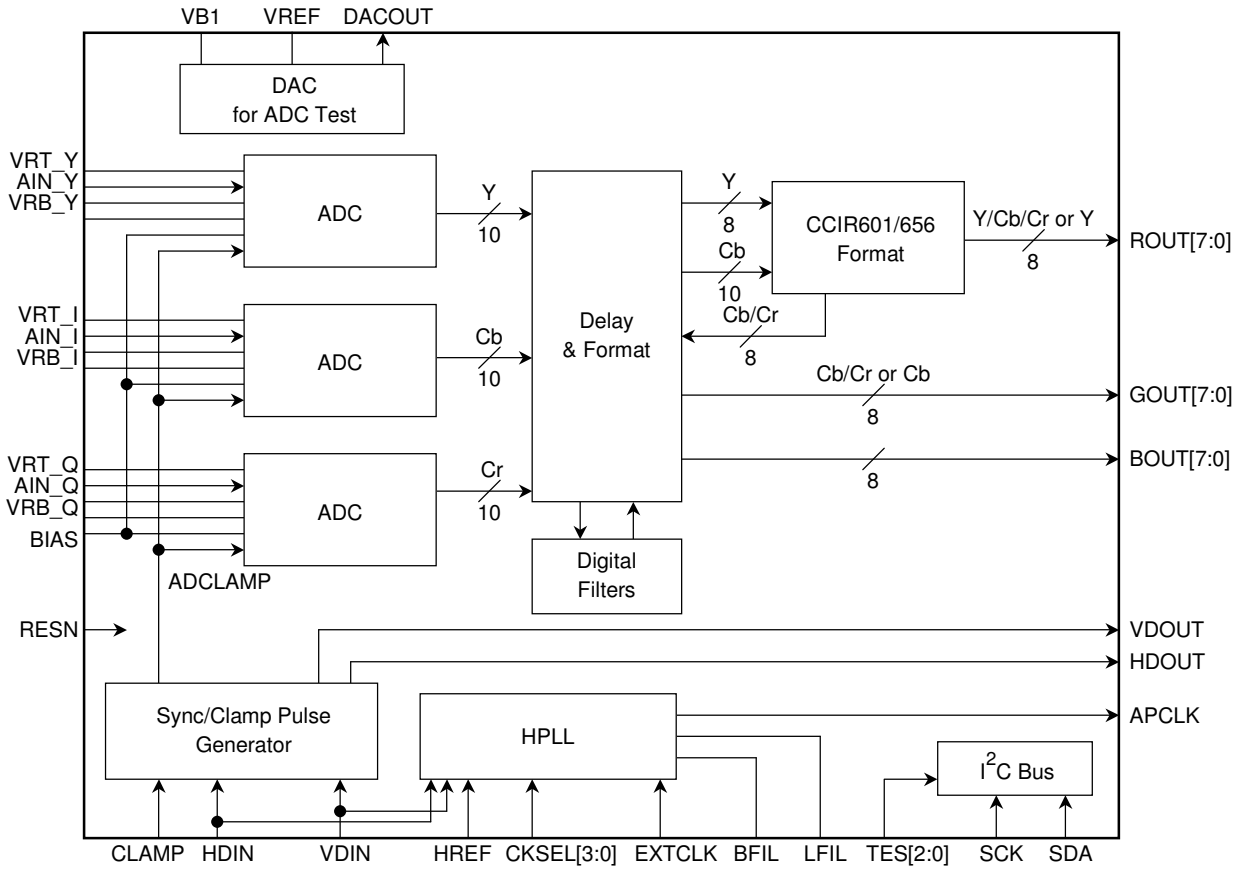
LQFP80-P-1212-0.50A

Weight: g (typ.)

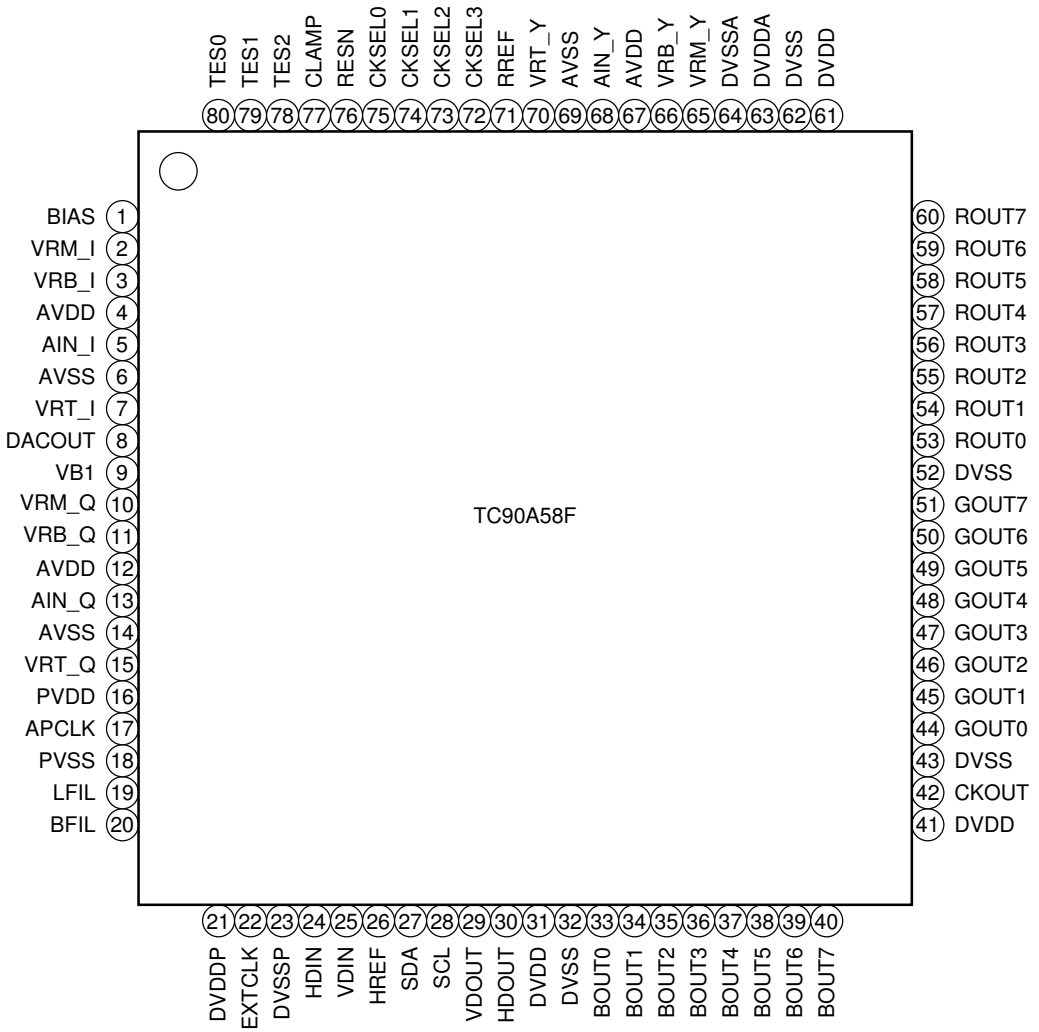
Main Functions and Features

- 3-channel, 8-bit AD converter (input amplitude: 1.32 V_{p-p})
- Y, Cb and Cr or R, G and B inputs.
- Pedestal clamp (Y or RGB: 16 LSB (in 8-bit conversion), Cb, Cr: 128 LSB (in 8-bit conversion)
- Switchable between external input or internal generation of clamp pulse
- Operates at 30 MHz maximum.
- Digital filter
  (Y: 6 MHz, Cb, Cr: 2.8 MHz/6 MHz)
- 10-bit output (only for 2-channel ADC)
- Horizontal PLL (HPLL)
- ITU-R601 and ITU-R656 formats supported
  (For ITU-R656, HD and VD must be input.)
- Y-signal delay circuit (delay amount can be set from 0 to 14 clocks, in units of clocks)
- I^2C bus control
- Built-in color bar generator

Block Diagram



Pin Description



Pin Functions

No.	Pin Name	I/O	Function	Notes
1	BIAS	O	Bias pin (for AD)	Ground to AVSS (pin 6) via 0.1-μF capacitor.
2	VRM_I	O	AD reference voltage (middle)	Same as above
3	VRB_I	O	AD reference voltage (bottom)	Same as above
4	AVDD	—	Analog power supply	—
5	AIN_I	I	AD input	Connect 0.47-μF capacitor and 20-Ω resistor.
6	AVSS	—	Analog GND	—
7	VRT_I	O	AD reference voltage (top)	Ground to AVSS (pin 6) via 0.1-μF capacitor.
8	DACOUT	O	Analog pin (for testing)	For testing purposes
9	VB1	—	Analog pin (for testing)	Ground to AVSS (pin 14) via 0.1-μF capacitor.
10	VRM_Q	O	AD reference voltage (middle)	Ground to AVSS (pin 14) via 0.1-μF capacitor.
11	VRB_Q	O	AD reference voltage (bottom)	Ground to AVSS (pin 14) via 0.1-μF capacitor.
12	AVDD	—	Analog power supply	—
13	AIN_Q	I	AD input	Connect 0.47-μF capacitor and 20-Ω resistor.
14	AVSS	—	Analog GND	—
15	VRT_Q	O	AD reference voltage (top)	Ground to AVSS (pin 14) via 0.1-μF capacitor.
16	PVDD	—	HPLL power supply	—
17	APCLK	O	Clock output	Outputs clock with amplitude of 1 V_{p-p} according to corresponding I^2C bus register setting. When I^2C bus register settings are default values, outputs are fixed to L.
18	PVSS	—	HPLL GND	—
19	LFIL	—	HPLL filter	Connecta 1-μF capacitor and a 1.0-kΩ resistor. Connect other end of capacitor as near to PVSS as possible. Also connect 0.01-μF capacitor in parallel with above capacitor and resistor.
20	BFIL	—	For stabilization	Connect 0.01-μF capacitor.
21	DVDDP	—	Digital power supply	For HPLL
22	EXTCLK	I	External clock input	Used as clock input pin in External Clock Mode. When built-in HPLL is used, set input to H or fix input to L.
23	DVSSP	—	Digital GND	For HPLL
24	HDIN	I	HD input	5-V withstanding voltage
25	VDIN	I	VD input	5-V withstanding voltage
26	HREF	I	HPLL pin	Input for external HPLL reference signal Phase is compared on rising edge.
27	SDA	I/O	I^2C bus data	5-V withstanding voltage
28	SCL	I	I^2C bus clock	5-V withstanding voltage
29	VDOUT	O	VD output	Outputs vertical sync signal pulse. Pulse polarity can be set using I^2C bus register.
30	HDOUT	O	HD output	Outputs horizontal sync signal pulse. Pulse polarity can be set using I^2C bus register.
31	DVDD	—	Digital power supply	Internal, for output PAD
32	DVSS	—	Digital GND	Internal, for output PAD
33	BOUT0	O	-/B/-OUTPUT	—
34	BOUT1	O	-/B/-OUTPUT	—
35	BOUT2	O	-/B/-OUTPUT	—

No.	Pin Name	I/O	Function	Notes
36	BOUT3	O	-/B/-OUTPUT	—
37	BOUT4	O	-/B/-OUTPUT	—
38	BOUT5	O	-/B/-OUTPUT	—
39	BOUT6	O	-/B/-OUTPUT	—
40	BOUT7	O	-/B/-OUTPUT	—
41	DVDD	—	Digital power supply	Internal, for output PAD
42	CKOUT	O	Clock output	Outputs internally-oscillated or externally-input clock. Polarity controllable using I^2C bus register. Clock output can be stopped using I^2C bus register. When clock output is halted, output goes High-Impedance.
43	DVSS	—	Digital GND	Internal, for output PAD
44	GOUT0	O	C/G/-output	—
45	GOUT1	O	C/G/-output	—
46	GOUT2	O	C/G/-output	—
47	GOUT3	O	C/G/-output	—
48	GOUT4	O	C/G/-output	—
49	GOUT5	O	C/G/-output	—
50	GOUT6	O	C/G/-output	—
51	GOUT7	O	C/G/-output	—
52	DVSS	—	Digital GND	—
53	ROUT0	O	Y/R/BS output	—
54	ROUT1	O	Y/R/BS output	—
55	ROUT2	O	Y/R/BS output	—
56	ROUT3	O	Y/R/BS output	—
57	ROUT4	O	Y/R/BS output	—
58	ROUT5	O	Y/R/BS output	—
59	ROUT6	O	Y/R/BS output	—
60	ROUT7	O	Y/R/BS output	—
61	DVDD	—	Digital power supply	Internal, for output PAD
62	DVSS	—	Digital GND	Internal, for output PAD
63	DVDDA	—	Digital power supply	For AD digital block
64	DVSSA	—	Digital GND	For AD digital block
65	VRM_Y	O	AD reference voltage (middle)	Ground to AVSS (pin 69) via 0.1-μF capacitor.
66	VRB_Y	O	AD reference voltage (bottom)	Ground to AVSS (pin 69) via 0.1-μF capacitor.
67	AVDD	—	Analog power supply	—
68	AIN_Y	I	AD input	Connect 0.47-μF capacitor and 20-Ω resistor.
69	AVSS	—	Analog GND	—
70	VRT_Y	O	AD reference voltage (top)	Ground to AVSS (pin 69) via 0.1-μF capacitor.
71	RREF	I	Reference resistance	AD reference resistance: Connect 8.2-kΩ resistor. Connect other end of resistor to analog power supply.

No.	Pin Name	I/O	Function	Notes
72	CKSEL3	I	Clock select	Sets relationship between input H frequency and HPLL oscillation frequency. Also switches between internal oscillation frequency and external clock input. When selecting clock using I^2C bus register, set CKSEL to all L.
73	CKSEL2	I	Clock select	
74	CKSEL1	I	Clock select	
75	CKSEL0	I	Clock select	
76	RESN	I	Reset pin	H for normal operation, L for reset
77	CLAMP	I	Clamp pin	Input for ADC clamp signal. Polarity can be changed using I^2C bus register. By default, clamp is applied by H. Switches between external input / internal generation of clamp signal according to I^2C Bus Register setting.
78	TES2	I	For testing purposes	Set to L.
79	TES1	I	For testing purposes	TES1 and TES0 determine 2 least significant bits of I^2C bus control slave address (details are given later).
80	TES0	I	For testing purposes	

Functions

1. Low-Pass Filter (LPF)

TC90A58F incorporates a low-pass filter (–3dB) for Y and C signals.
When the system clock is 27 MHz, cut-off frequency is 6 MHz for Y signal and 2.8 MHz for C signal.
When the system clock frequency is higher than 27 MHz, cut-off frequencies are determined as follows:

Example: System clock frequency = 29.82 MHz
Y signal cut-off frequency: 6 (MHz) × (29.82 (MHz) ÷ 27 (MHz)) = approx. 6.63 MHz
Cb, Cr cut-off frequency: 2.8 (MHz) × (29.82 (MHz) ÷ 27 (MHz)) = approx. 3.09 MHz
Low-pass filter characteristic for Y and C signals is shown below:

Y (RGB) Signal Cut-off Frequency = 6 MHz

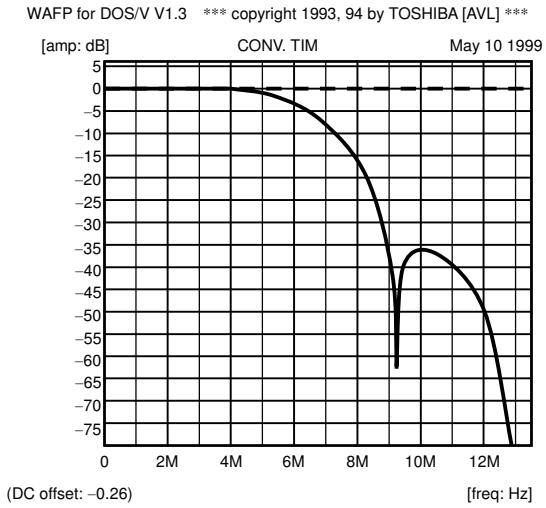


Figure 1 Y Signal LPF Characteristic (system clock = 27 MHz)

Cb, Cr Signal Cut-off Frequency = 2.8 MHz

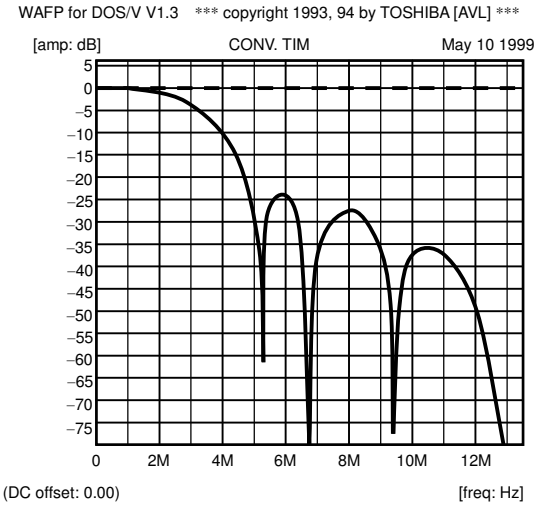


Figure 2 C Signal LPF Characteristic (system clock = 27 MHz)

2. Output Format Setting

Eight output formats are supported as detailed below.
Set the output format in the bits MODE2~MODE0 of the I^2C bus register Sub-Address 00H.

(1) Output format in Standard 4:2:2 Mode

ROUT[7:0]	$Y0_{7\text{-}0}$	$Y1_{7\text{-}0}$	$Y2_{7\text{-}0}$	$Y3_{7\text{-}0}$	$Y4_{7\text{-}0}$	$Y5_{7\text{-}0}$	$Y6_{7\text{-}0}$	$Y7_{7\text{-}0}$
GOUT[7:0]	$Cb0_{7\text{-}0}$	$Cr1_{7\text{-}0}$	$Cb2_{7\text{-}0}$	$Cr2_{7\text{-}0}$	$Cb4_{7\text{-}0}$	$Cr4_{7\text{-}0}$	$Cb6_{7\text{-}0}$	$Cr6_{7\text{-}0}$
BOUT[7:0]	Hi-Z							

(2) Output format in Special 4:2:2 Mode

ROUT[7:0]	$Y0_{7\text{-}0}$	$Y1_{7\text{-}0}$	$Y2_{7\text{-}0}$	$Y3_{7\text{-}0}$	$Y4_{7\text{-}0}$	$Y5_{7\text{-}0}$	$Y6_{7\text{-}0}$	$Y7_{7\text{-}0}$
GOUT[7:0]	$Cb0_{7\text{-}0}$	$Cr1_{7\text{-}0}$	$Cb2_{7\text{-}0}$	$Cr3_{7\text{-}0}$	$Cb4_{7\text{-}0}$	$Cr5_{7\text{-}0}$	$Cb6_{7\text{-}0}$	$Cr7_{7\text{-}0}$
BOUT[7:0]	Hi-Z							

(3) Output format in 4:4:4 Mode

ROUT[7:0]	$Y0_{7\text{-}0}$	$Y1_{7\text{-}0}$	$Y2_{7\text{-}0}$	$Y3_{7\text{-}0}$	$Y4_{7\text{-}0}$	$Y5_{7\text{-}0}$	$Y6_{7\text{-}0}$	$Y7_{7\text{-}0}$
GOUT[7:0]	$Cb0_{7\text{-}0}$	$Cb1_{7\text{-}0}$	$Cb2_{7\text{-}0}$	$Cb3_{7\text{-}0}$	$Cb4_{7\text{-}0}$	$Cb5_{7\text{-}0}$	$Cb6_{7\text{-}0}$	$Cb7_{7\text{-}0}$
BOUT[7:0]	$Cr0_{7\text{-}0}$	$Cr1_{7\text{-}0}$	$Cr2_{7\text{-}0}$	$Cr3_{7\text{-}0}$	$Cr4_{7\text{-}0}$	$Cr5_{7\text{-}0}$	$Cr6_{7\text{-}0}$	$Cr7_{7\text{-}0}$

(4) Output format in Standard 4:4:1 Mode

ROUT[7:0]	$Y0_{7-0}$	$Y1_{7-0}$	$Y2_{7-0}$	$Y3_{7-0}$	$Y4_{7-0}$	$Y5_{7-0}$	$Y6_{7-0}$
GOUT[7:6]	$Cb0_{7-6}$	$Cb0_{5-4}$	$Cb0_{3-2}$	$Cb0_{1-0}$	$Cb4_{7-6}$	$Cb4_{5-4}$	$Cb4_{3-2}$
GOUT[5:4]	$Cr0_{7-6}$	$Cr0_{5-4}$	$Cr0_{3-2}$	$Cr0_{1-0}$	$Cr4_{7-6}$	$Cr4_{5-4}$	$Cr4_{3-2}$
GOUT[3:0]	Hi-Z						
BOUT[7]	TRG						
BOUT[6:0]	Hi-Z						

(5) Output format in Special 4:1:1 Mode

ROUT[7:0]	$Y0_{7-0}$	$Y1_{7-0}$	$Y2_{7-0}$	$Y3_{7-0}$	$Y4_{7-0}$	$Y5_{7-0}$	$Y6_{7-0}$
GOUT[7:6]	$Cb0_{3-2}$	$Cb0_{7-6}$	$Cr2_{3-2}$	$Cr2_{7-6}$	$Cb4_{3-2}$	$Cb4_{7-6}$	$Cb6_{3-2}$
GOUT[5:4]	$Cb0_{1-0}$	$Cb0_{5-4}$	$Cr2_{1-0}$	$Cr2_{5-4}$	$Cb4_{1-0}$	$Cb4_{5-4}$	$Cb6_{1-0}$
GOUT[3:0]	Hi-Z						
BOUT[7]	TRG						
BOUT[6:0]	Hi-Z						

Note1: In the above format, 1-data cycle is the main clock (MCK).

(For example, when the clock generated by HPLL is 29.82 MHz, MCK = 29.82 MHz)

(6) Output format in ITU-R601 16-Bit Mode (data rate: 13.5 MHz)

ROUT[7:0]	$Y0_{7-0}$	$Y1_{7-0}$	$Y2_{7-0}$	$Y3_{7-0}$	$Y4_{7-0}$	$Y5_{7-0}$	$Y6_{7-0}$	$Y7_{7-0}$
GOUT[7:0]	$Cb0_{7-0}$	$Cr0_{7-0}$	$Cb2_{7-0}$	$Cr2_{7-0}$	$Cb4_{7-0}$	$Cr4_{7-0}$	$Cb6_{7-0}$	$Cr6_{7-0}$
BOUT[7:0]	Hi-Z							

(7) Output format in ITU-R601 8-Bit Mode (data rate: 27 MHz)

ROUT[7:0]	$Cb0_{7-0}$	$Y0_{7-0}$	$Cr0_{7-0}$	$Y1_{7-0}$	$Cb2_{7-0}$	$Y2_{7-0}$	$Cr2_{7-0}$	$Y3_{7-0}$
GOUT[7:0]	Hi-Z							
BOUT[7:0]	Hi-Z							

(8) ITU-R656

Adds SAV and EAV (H, V and F information) to the data in format 7 and outputs the result.

3. Y Signal Delay Circuit

The circuit can delay the Y signal by 0 to 14 clocks in relation to the C signal.
The delay can be set in the bits YDLY3~YDLY0 of the I^2C bus register Sub-Address 17H.

4. Color Bar Generator

Color bars for both NTSC and PAL can only be generated internally in ITU-R656 or ITU-R601 (either 8- or 16-bit) Mode.
The color bar mode can be set in the BAR bit of the I^2C bus register Sub-Address 2AH.

5. HD Output

The output timing and width of HDOUT (pin 30) can be set in the I^2C bus registers (see figure below).
Timing: HDSTA10~HDSTA5 in Sub-Address 05H and HDSTA4~HDSTA0 in Sub-Address 06H
Output width: HDPW10~HDPW8 in Sub-Address 06H and HDPW7~HDPW0 in Sub-Address 07H

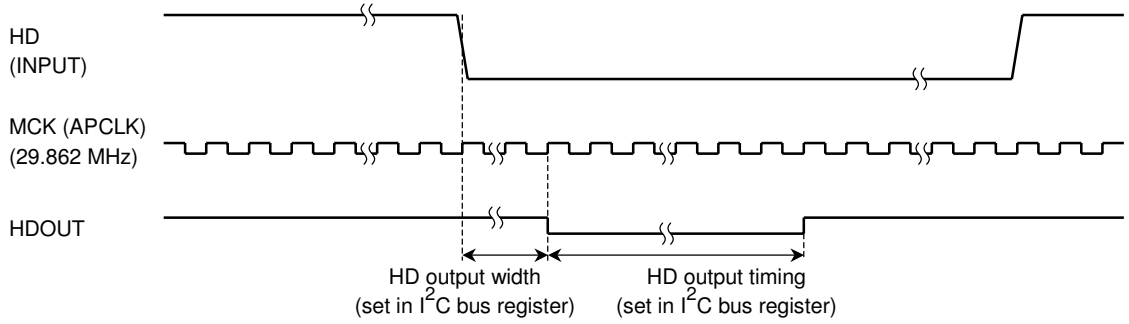


Figure 3 HDOUT Timing Chart

The HD signal input from the HDIN (pin 24) can pass through unaltered and be output from HDOUT. In this case, the HDOUT output is delayed by 15 clocks from the HDIN input.
Through Mode can be set using the HDSELB bit in the I^2C bus register Sub-Address 00H.

6. VD Output

The VD signal output from the VDIN (pin 24) can pass through unaltered and be output from VDOUT (pin 29).

There are two output timings: output delayed by 15 clocks from VDIN or output at the same timing as HDOUT. The timing can be selected in the I^2C bus register VDOSEL Sub-Address 09H. The VD signal can also be generated internally.
Select internal generation using the VRNMOD bit in the I^2C bus register Sub-Address 02H.

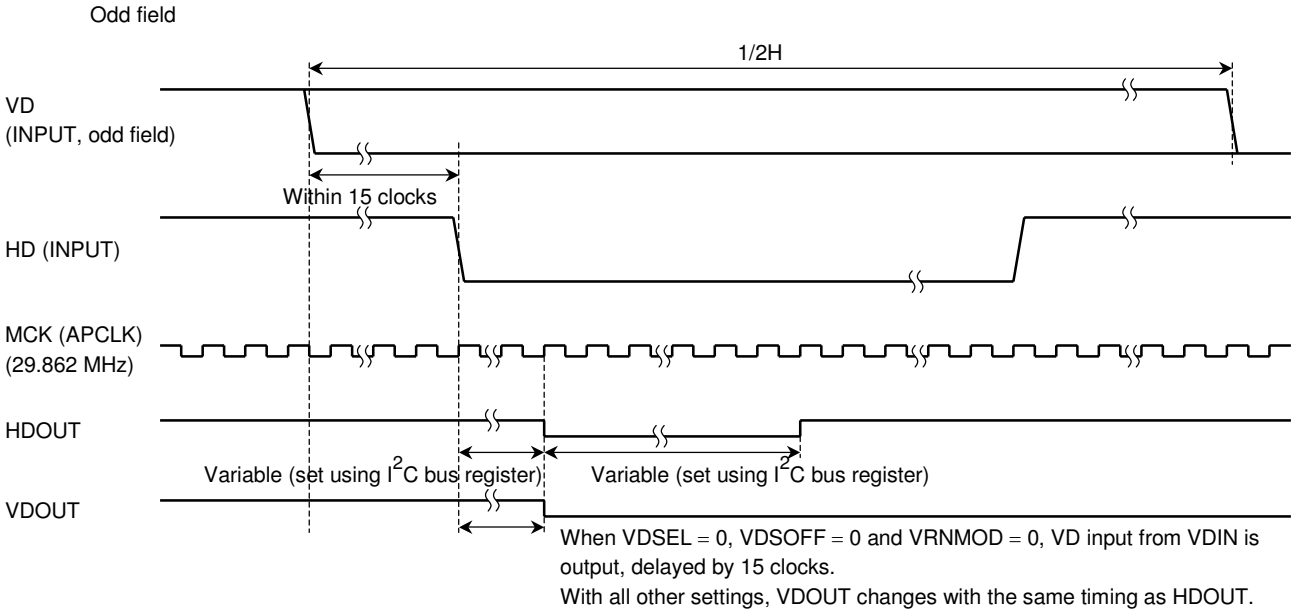


Figure 4 VDOUT Timing Chart

7. Multiplexing H, V and F

In ITU-R656 Mode only, SAV and EAV (H, V and F information) are multiplexed in the data.
Where data is multiplexed depends on the HD output timing.

8. I^2C Bus

The TC90A58F bus control format conforms to the Philips I^2C bus control format.
The two least significant bits (A0 and A1) of the slave address can be set using TES1 and TES0 (pins 79 and 80).

Slave Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	1	1	A1	A0	—

Set two least significant bits (A0 and A1).

TES1	TES0	Slave Address
0	0	10011000
0	1	10011010
1	0	10011100
1	1	10011110

9. Countermeasure against HDIN and VDIN Pulse Noise (to avoid misinterpretation)

A countermeasure is taken to prevent spike noise in the pulse input to the HDIN and VDIN pins from being misinterpreted as genuine HD and VD input.
The noise-detection width (either all pulses of less than 8 clocks or all pulses of less than 1 clock are regarded as noise) can be set using the bits HDDIRECT and VDDIRECT in the I^2C bus registers Sub-Address 03H.

10. Countermeasure against VDIN Noise (to avoid misinterpretation)

A countermeasure is taken to prevent noise in 1 V (during vertical scanning) from being misinterpreted as VD.
Noise rejection can be switched ON/OFF using the VGATEON bit in the I^2C bus register Sub-Address 11H.
The noise detection range can be set using the VGTEGA and VGTEGB bits in Sub-Address 0FH~ Sub-Address 11H).

11. Internal Generation of Clamp Pulse

The clamp pulse can be internally generated.
Switching between external input and internal generation of the clamp pulse can be set using the CLPSEL bit in the I^2C bus register Sub-Address 0EH.
The clamp pulse generation timing and width can be set using the corresponding I^2C bus registers.
Timing: CLPSTA10~CLPSTA4 in Sub-Address 0CH and CLPSTA3~CLPSTA0 in Sub-Address 0DH
Pulse width: CLPWID10~CLPWID7 in Sub-Address 0DH and CLPWID6~CLPWID0 in Sub-Address 0EH

12. Built-in HPLL

The TC90A58F has a built-in horizontal PLL. The following parameters can be set using the I^2C bus registers.

- Divider control (when using internal divider): DIVIIC3~DIVIIC0 in Sub-Address 14H
  Can also be set using CKSEL[3:0] (pins 72~75) as well as in the I^2C bus register.
  CKSEL[3:0] is enabled only when DIVIIC3~DIVIIC0 in is all 0s.
- Selection of phase comparator (PC) in HPLL (PC2 or PC3): PCSEL0~PCSEL1 in Sub-Address 01H
- Selection of divider (internal or external): DIVSEL in Sub-Address 01H
- 1-V_{p-p} output / full-swing output (APCLK output): OUTSEL in Sub-Address 01H
- HPLL oscillation/oscillation halt: HPLLSTOP in Sub-Address 01H

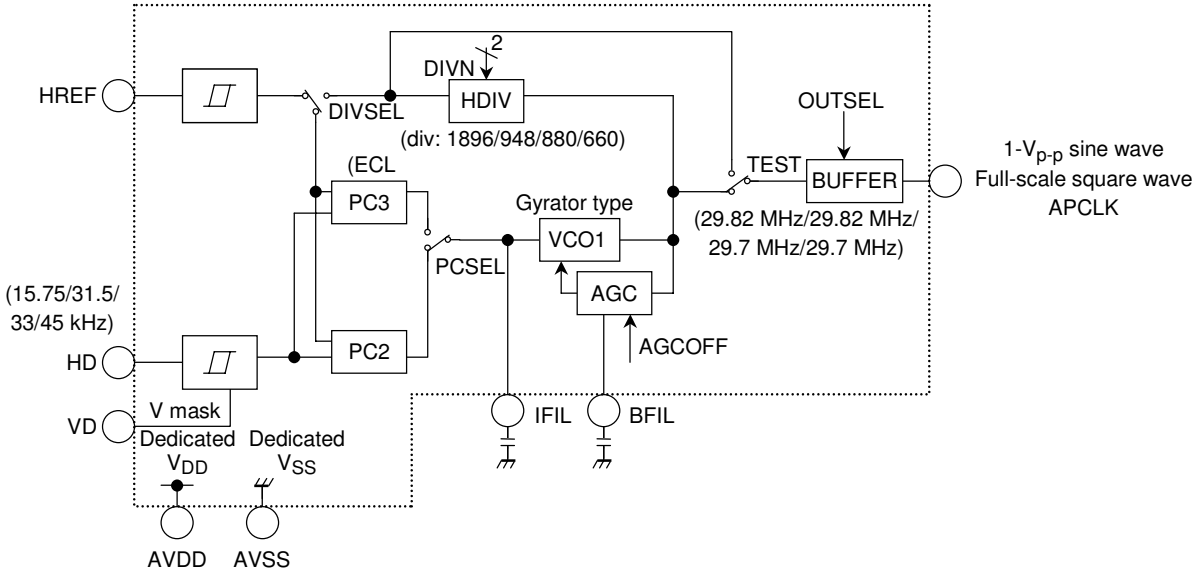


Figure 5 Block Diagram of HPLL

13. 10-Bit ADC

The TC90A58F can also be used as a 10-bit AD converter. This setting can be made using the M10B bit in the I^2C bus register Sub-Address 1CH.

Note that when the device is used as a 10-bit AD converter, only two channels (the Y and Cb signals) are output from the following output pins.

Y signal: ROUT[7:0], GOUT[7:6]
Cb signal: GOUT[1:0], BOUT[7:0]

When the TC90A58F is used as a 10-bit AD converter, only certain functions can be used.

【Available functions】

1. Low-pass filter
2. Output format setting (4:4:4 only)
3. Y delay (Y signal only)
4. Color bar generation (4:4:4 only)
5. HDOUT timing adjustment
6. VDOUT timing adjustment
8. I^2C bus register setting
9. Countermeasure against HDIN and VDIN pulse noise
10. Countermeasure against VDIN noise
11. Clamp pulse timing
12. HPLL settings
14. Clamp level setting

【Unavailable functions】

Processing for R601, R656, 4:1:1 and 4:2:2 modes (for functions 2, 4 and 7 in the list of available functions shown above)

14. Clamp Level

The clamp level is set to the following values:

Y (RGB): 16 (for 8-bit conversion)

C: 128 (for 8-bit conversion)

15. ADC Input Signal

The input signal band and range are as follows:

Band: 10 MHz

Range: 1.32 V_{p-p} (typ.), 0.99 V_{p-p}~2.31 V_{p-p}

16. 5-V Withstanding Voltage

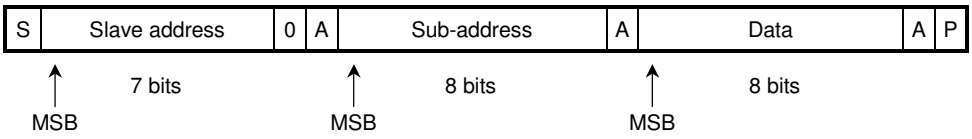
HDIN, VDIN, SDA and SCL (pins 24, 25, 27 and 28) have a withstanding voltage of 5 V.

I^2C Bus Register Map

1. Format

The TC90A58F bus control format conforms to the Philips I^2C bus control format standard.

Data transfer format

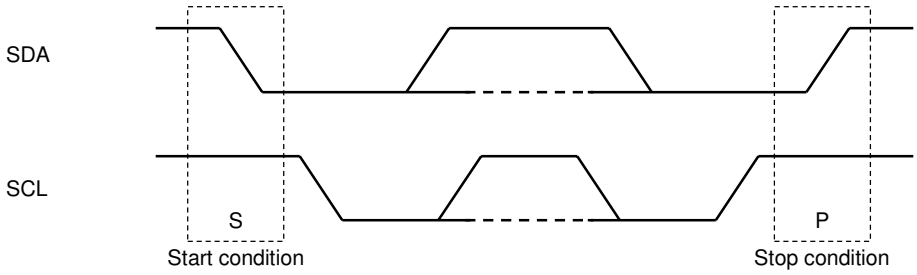


S: Start condition

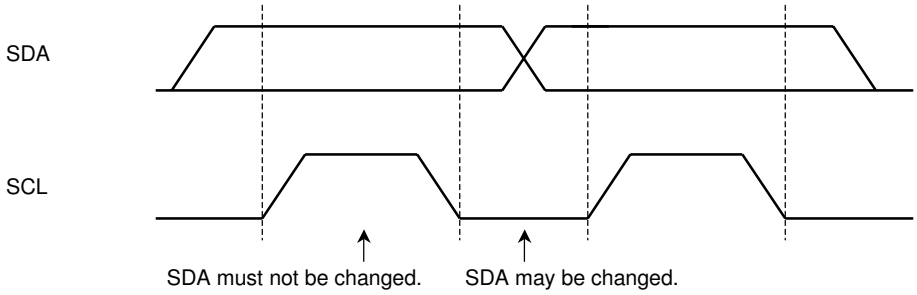
P: Stop condition

A: Acknowledgement

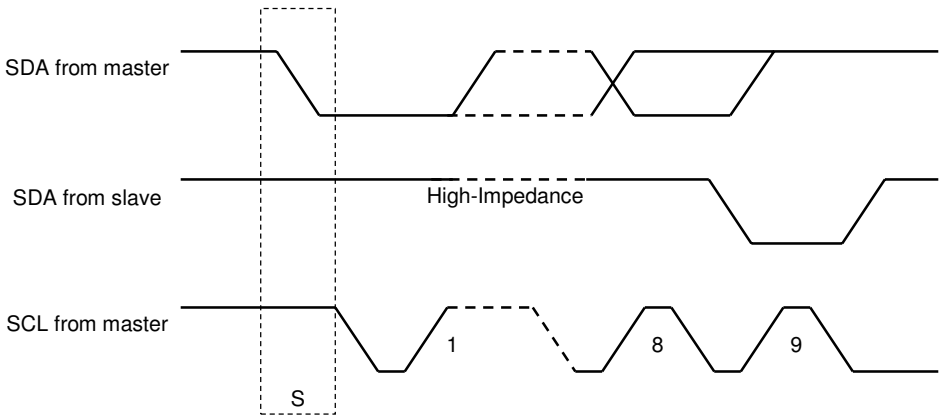
(1) Start and stop conditions



(2) Bit transfer



(3) Acknowledgement



(4) Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	1	1	A1	A0	—

Note2: A1 and A0 are set using pins 79 and 80.

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Right to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

2. Settings

Sub-Address (H)	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
00	*	NTPAL	MODE2	MODE1	MODE0	RGBC	VLINSEL	HDSELB
01	*	PCSEL0	PCSEL1	DIVSEL	VCOAGC	OUTSEL	CLKSEL	CKPOL
02	DAPWDN	ADPWDN	VRNMOD	VCNTCR	HDPQO	VDPQO	HDPOL	*
03	HVSEL656	INTER	VNSOFF	VDPO	VDDIRECT	HDPO	HDDIRECT	HRTMG10
04	HRTMG9	HRTMG8	HRTMG7	HRTMG6	HRTMG5	HRTMG4	HRTMG3	HRTMG2
05	HRTMG1	HRTMG0	HDSTA10	HDSTA9	HDSTA8	HDSTA7	HDSTA6	HDSTA5
06	HDSTA4	HDSTA3	HDSTA2	HDSTA1	HDSTA0	HDPW10	HDPW9	HDPW8
07	HDPW7	HDPW6	HDPW5	HDPW4	HDPW3	HDPW2	HDPW1	HDPW0
08	IHVD	VRTMG9	VRTMG8	VRTMG7	VRTMG6	VRTMG5	VRTMG4	VRTMG3
09	VRTMG2	VRTMG1	VRTMG0	VDOSELGT	VDOSEL	VGSTA	REGF1	REGF2
0C	ADCLAPO	CLPSTA10	CLPSTA9	CLPSTA8	CLPSTA7	CLPSTA6	CLPSTA5	CLPSTA4
0D	CLPSTA3	CLPSTA2	CLPSTA1	CLPSTA0	CLPWID10	CLPWID9	CLPWID8	CLPWID7
0E	CLPWID6	CLPWID5	CLPWID4	CLPWID3	CLPWID2	CLPWID1	CLPWID0	CLPSEL
0F	*	*	*	VGTEDA9	VGTEDA8	VGTEDA7	VGTEDA6	VGTEDA5
10	VGTEDA4	VGTEDA3	VGTEDA2	VGTEDA1	VGTEDA0	VGTEDB9	VGTEDB8	VGTEDB7
11	VGTEDB6	VGTEDB5	VGTEDB4	VGTEDB3	VGTEDB2	VGTEDB1	VGTEDB0	VGATEON
12	*	ODEV10	ODEV9	ODEV8	ODEV7	ODEV6	ODEV5	ODEV4
13	ODEV3	ODEV2	ODEV1	ODEV0	ODDETPO	*	*	*
14	DIVIIC3	DIVIIC2	DIVIIC1	DIVIIC0	DIVHDSEL	HRESVAR	*	*
17	REG4	REG5	REG6	REG10	YDLY3	YDLY2	YDLY1	YDLY0
18	REG11	LPFYPASS	LPI0ON2	LPI0ON1	LPI0ON0	LPQ0ON2	LPQ0ON1	LPQ0ON0
19	REG9	REG7	REG8	QDSEL1	QDSEL0	IDSEL1	IDSEL0	LPYON
1A	REG12	*	*	*	*	*	*	*
1B	REGSWR7	REGSWR1	REGSWG7	REGSWG3	REGSWG1	REGSWB7	REGSWB6	REGSWHV
1C	M10B	*	*	CKOUTSTP	*	*	*	*
2A	*	*	*	*	*	*	BAR	*

Note3: * indicates that use is prohibited. Set to L.

3. Settings in Detail

Sub-Address 00H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	—	NTPAL	MODE2	MODE1	MODE0	RGBC	VLINSEL	HDSELB
Default	—	0	0	0	0	0	0	0

- NTPAL: Switches between NTSC and PAL.
  0 (default): NTSC 1: PAL

- MODE2~MODE0: Switches output format.

MODE2	MODE1	MODE0	Output Format
0	0	0	4:2:2 (standard, default)
0	0	1	4:2:2 (special)
0	1	0	4:1:1 (standard)
0	1	1	4:1:1 (special)
1	0	0	4:4:4
1	0	1	R601 16-Bit Mode
1	1	0	R601 8-Bit Mode
1	1	1	R656

- RGBC: Switches the ADC clamp level for Cb and Cr.
  0 (default): The ADC clamp level is 16 LSB for Y (for 8-bit conversion) and 128 LSB for Cb and Cr (for 8-bit conversion).
  The clamp level is the pedestal clamp.
  1: The clamp level for Y, Cb and Cr is 16 LSB (for 8-bit conversion) (for RGB)
  The clamp level is the pedestal clamp.

- VLINSEL: Sets the number of vertical lines.
  0 (default): 525 (when NTPAL = 0) or 625 (when NTPAL = 1)
  1: Any value from 1 to 1023 (Set using bits VLIN9~VLIN0 in Sub-Addresses 08H and 09H.)

- HDSELB: Switches HD output signal.
  0 (default): Variable HD output timing 1: Fixed HD output timing

Sub-Address 01H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	—	PCSEL0	PCSEL1	DIVSEL	HPLLSTOP	OUTSEL	CLKSEL	CKPOL
Default	—	0	0	0	0	0	0	0

- PSCEL0~PSCEL1 Switches the phase comparator in HPLL.

PCSEL0	PCSEL1	PC Used
0	0	PC2 (default)
1	0	Use prohibited
0	1	Use prohibited
1	1	PC3

- DIVSEL: Switches the reference HD.
  0 (default): the Reference HD generated internally
  1: Reference HD input externally (via HREF pin)

- HPLLSTOP: Switches HPLL oscillation ON/OFF.
  0 (default): HPLL oscillates. 1: HPLL stops oscillating.

- OUTSEL: Switches the clock (APCLK) output.
  0 (default): Full-swing (square) output 1: 1-$V_{p\text{-}p}$ output

- CLKSEL: Switches the clock.
  0 (default): Uses clock generated by HPLL.
  1: Uses clock input externally.

- CKPOL: Switches the polarity of output clock (APCLK and CKOUT).
  0 (default): Positive polarity 1: Negative polarity

Sub-Address 02H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	DAPWDN	ADPWDN	VRNMOD	VCNTCR	HDPQO	VDPQO	HDPOL	—
Default	0	1	0	0	0	0	0	—

- DAPWDN: DAC power-down ON/OFF
  0 (default): DAC power-down ON 1: DAC power-down OFF

- ADPW: ADC power-down ON/OFF
  0: ADC power-down ON 1 (default): ADC power-down OFF

- VRNMOD: Used to set the VD output timing before the VD input timing.
  0 (default): VD outputs VD input signal.
  1: Because the VD signal is generated internally, the VD output timing can be before the VD input timing.

- VCNTCR: Sets the V counter reset timing.
  0 (default): Resets at H counter = 0.
  1: Reset on falling edge of HDOUT

- HDPOQ: Switches the HD output polarity.
  0 (default): Negative polarity (HDOTD = 0), same polarity as the input HD (HDSELB = 1 and HDPO = 0), or opposite polarity from the input HD (HDSELB = 1 and HDPO = 1)
  1: Positive polarity (HDOTD = 0), opposite polarity from the input HD (HDSELB = 1 and HDPO = 0), or same polarity as the input HD (HDSELB = 1 and HDPO = 1)

- VDPOQ: Switches the VD output polarity.
  0 (default): Negative polarity (VNSOFF = 1 or VRNMOD = 1), same polarity as the input VD (VNSOFF = 0, VRNMOD = 0 and VDPO = 0), or opposite polarity from the input VD (VNSOFF = 0, VRNMOD = 0 and VDPO = 1)
  1: Positive polarity (VNSOFF = 1 or VRNMOD = 1), opposite polarity from the input VD (VNSOFF = 0, VRNMOD = 0 and VDPO = 0), or same polarity as the input VD (VNSOFF = 0, VRNMOD = 0 and VDPO = 1)

- HDPOL: Switches the HPLL HD input polarity.
  0 (default): Same polarity as the input HD 1: Opposite polarity from the input HD

Sub-Address 03H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	HVSEL65	INTER	VNSOFF	VDPO	VDDIRECT	HDPO	HDDIRECT	HRTMG10
Default	0	0	0	0	0	0	0	1

- HVSEL65: Changes the HD and VD output timing in relation to EAV.
  0 (default): HD and VD output timing is the same as EAV.
  1: HD and VD output timing is delayed in relation to EAV by +32 clocks for NTSC and by +24 clocks for PAL.

- INTER: Sets the VD output to be once or twice per frame (Note4).
  (Enabled only when VRNMOD = 1)
  0 (default): Outputs VD for each field.
  1: Outputs VD per frame.

  Note4: A frame consists of 525 lines for NTSC; 625 lines for PAL.

- VNSOFF: Enables/Disables VD input.
  0 (default): Enables VD input. 1: Disables VD input.

- VDPO: Sets the VD input polarity.
  0 (default): Same polarity 1: Opposite polarity

- VDDIRECT: Selects VD input.
  0 (default): Identifies input pulses of 8 clocks or more as VD input.
  1: Identifies input pulses of 1 clock or more as VD input.

- HDPO: Sets the HD input polarity.
  0 (default): Same polarity 1: Opposite polarity

- HDDIRECT: Selects HD input.
  0 (default): Identifies input pulses of 8 clocks or more as HD input.
  1: Identifies input pulses of 1 clock or more as HD input.

- HRTMG10: Sets the number of samples per 1H. Sets in combination with HRTMG9~HRTMG2 in Sub-Address 04H and HRTMG1~HRTMG0 in Sub-Address 05H.

Sub-Address 04H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	HRTMG9	HRTMG8	HRTMG7	HRTMG6	HRTMG5	HRTMG4	HRTMG3	HRTMG2
Default	1	0	1	0	1	1	0	0

- HRTMG9~HRTMG2: Sets the number of samples per 1H. This setting works in combination with HRTMG10 in Sub-Address 03H and HRTMG1~HRTMG0 in Sub-Address 05H.

Sub-Address 05H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	HRTMG1	HRTMG0	HDSTA10	HDSTA9	HDSTA8	HDSTA7	HDSTA6	HDSTA5
Default	1	1	0	0	0	0	0	0

- HRTMG1~HRTMG0: Sets the number of samples per 1H. This setting works in combination with the settings of HRTMG10 in Sub-Address 03H and HRTMG9~HRTMG2 in Sub-Address 04H.

- HDSTA10~HDSTA5: Sets the HD output timing. This setting works in combination with the setting of HDSTA4~HDSTA0 in Sub-Address 06H.

Sub-Address 06H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	HDSTA4	HDSTA3	HDSTA2	HDSTA1	HDSTA0	HDPW10	HDPW9	HDPW8
Default	1	0	0	0	0	0	0	0

- HDSTA4~HDSTA0: Sets the HD output timing. This setting works in combination with the setting of HDSTA10~HDSTA5 in Sub-Address 05H.

- HDPW10~HDPW8: Sets the HD width. This setting works in combination with the setting of HDPW7 ~HDPW0 in Sub-Address 07H.

Sub-Address 07H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	HDPW7	HDPW6	HDPW5	HDPW4	HDPW3	HDPW2	HDPW1	HDPW0
Default	1	0	0	0	0	0	0	0

- HDPW7~HDPW0: Sets the HD width. This setting works in combination with the setting of HDPW10 ~HDPW8 in Sub-Address 06H.

Sub-Address 08H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	IHVD	VRTMG9	VRTMG8	VRTMG7	VRTMG6	VRTMG5	VRTMG4	VRTMG3
Default	0	1	0	0	0	0	0	1

- IHVD: Sets whether the I^2C bus data is updated continuously or at the VD cycle.
  0 (default): I^2C bus data is updated continuously.
  1: I^2C bus data is updated at VD cycle.

- VRTMG9~VRTMG3: Sets the number of lines per frame. Enabled only when VLINSEL in Sub-Address 00H = 1. This setting works in combination with the setting of VRTMG2~VRTMG0 in Sub-Address 09H.

Sub-Address 09H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VRTMG2	VRTMG1	VRTMG0	VDOSELGT	VDOSEL	VGSTA	REGF1	REGF2
Default	1	0	0	0	0	0	0	0

- VRTMG2~VRTMG0: Sets the number of lines per frame. Enabled only when VLINSEL in Sub-Address 00H = 1.
  This setting works in combination with VRTMG9~VRTMG3 in Sub-Address 08H.

- VDOSELGT: Selects VD after noise rejection by VGATE (VD gate pulse) or VDIN as the signal output to VDOUT.
  0 (default): Outputs VDIN unchanged.
  1: Outputs VD after noise rejection by VGATE.

- VDOSEL: Selects VD generated by the internal V counter or VD selected by VDOSELGT as the signal output to VDOUT.
  0 (default): Outputs VD selected by VDOSELGT.
  1: Outputs VD generated by the internal V counter.

- VGSTA: Selects the falling or rising edge of VDIN as the VGATE starting point.
  0 (default): Selects falling edge of VDIN as the VGATE starting point.
  1: Selects rising edge of VDIN as the VGATE starting point.
  Set to 0 if VDIN has positive polarity. Set to 1 if VDIN has negative polarity.

- REGF1: Forces serial byte processing (alternately outputs color difference signal and Y signal as 8-bit data).
  0 (default): Performs serial byte processing only in R656 and R601 8-Bit Modes.
  1: Forces serial byte processing to be performed.

- REGF2: Sets the data between EAV and SAV.
  0 (default): Sets data between EAV and SAV to be 80H (Cb or Cr) or 10H (Y).
  1: Does not set data between EAV and SAV but outputs the input data unchanged.

Sub-Address 0CH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	ADCLAPO	CLPSTA10	CLPSTA9	CLPSTA8	CLPSTA7	CLPSTA6	CLPSTA5	CLPSTA4
Default	0	0	0	0	1	0	0	1

- ADCLAPO: Sets the polarity for clamp pulse.
  0 (default): Inverts polarity. 1: Does not invert polarity.

- CLPSTA10~CLPSTA4: Sets the starting point of the clamp pulse generated internally in Clamp Pulse Internal Generation Mode (i.e. when CLPSEL = 1 in Sub-Address 0EH).
  This setting works in combination with the setting of CLPSTA3~CLPSTA0 in Sub-Address 0DH.

Sub-Address 0DH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CLPSTA3	CLPSTA2	CLPSTA1	CLPSTA0	CLPWID10	CLPWID9	CLPWID8	CLPWID7
Default	0	0	0	0	0	0	0	0

- CLPSTA3~CLPSTA0: Sets the starting point of the clamp pulse generated internally in Clamp Pulse Internal Generation Mode (i.e. when CLPSEL = 1 in Sub-Address 0EH).
  This setting works in combination with the setting of CLPSTA10~CLPSTA4 in Sub-Address 06H.

- CLPWID10~CLPWID7: Sets the width of the clamp pulse generated internally in Clamp Pulse Internal Generation Mode (i.e. when CLPSEL = 1 in Sub-Address 0EH).
  This setting works in combination with the setting of CLPWID6~CLPWID0 in Sub-Address 0EH.

Sub-Address 0EH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	CLPWID6	CLPWID5	CLPWID4	CLPWID3	CLPWID2	CLPWID1	CLPWID0	CLPSEL
Default	1	1	0	0	0	0	0	0

- CLPWID6~CLPWID0: Sets the width of the clamp pulse generated internally in Clamp Pulse Internal Generation Mode (i.e. when CLPSEL = 1 in Sub-Address 0EH).
  This setting works in combination with the setting of CLPWID10~CLPWID7 in Sub-Address 0DH.

- CLPSEL: Selects the externally input clamp pulse or internally generated clamp pulse.
  0 (default): Externally input clamp pulse 1: Internally generated clamp pulse

Sub-Address 0FH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	—	—	—	VGTEDA9	VGTEDA8	VGTEDA7	VGTEDA6	VGTEDA5
Default	—	—	—	0	0	0	0	0

- VGTEDA9~VGTEDA5: Sets stop point 1 of VD-noise-rejected gate pulse.
  Enabled only when VGATEON in Sub-Address 11H = 1
  This setting works in combination with the setting of VGTEDA4~VGTEDA0 in Sub-Address 10H.

Sub-Address 10H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VGTEDA4	VGTEDA3	VGTEDA2	VGTEDA1	VGTEDA0	VGTEDB9	VGTEDB8	VGTEDB7
Default	0	0	0	0	0	0	0	0

- VGTEDA4~VGTEDA0: Sets stop point 1 of VD-noise-rejected gate pulse.
  VGATEON = Enabled only when VGATEON in Sub-Address 11H = 1.
  This setting works in combination with the setting of VGTEDA9~VGTEDA5 in Sub-Address 0FH.

- VGTEDB9~VGTEDB7: Sets stop point 2 of VD-noise-rejected gate pulse.
  Enabled only when VGATEON in Sub-Address 11H = 1.
  This setting works in combination with the setting of VGTEDB6~VGTEDB0 in Sub-Address 11H.

Sub-Address 11H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	VGTEDB6	VGTEDB5	VGTEDB4	VGTEDB3	VGTEDB2	VGTEDB1	VGTEDB0	VGATEO
Default	0	0	0	0	0	0	0	0

- VGTEDB6~VGTEDB0: Sets stop point 2 of VD-noise-rejected gate pulse.
  Enabled only when VGATEON in Sub-Address 11H = 1.
  This setting works in combination with the setting of VGTEDB9~VGTEDB7 in Sub-Address 10H.

- VGATEON: Sets VD noise rejection ON/OFF.

  0 (default): VD noise rejection OFF
  1: VD noise rejection ON

Sub-Address 12H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	—	ODEV10	ODEV9	ODEV8	ODEV7	ODEV6	ODEV5	ODEV4
Default	—	0	0	0	0	0	0	0

- ODEV10~ODEV4: Sets the point (within 1H) where odd- or even-numbered field is identified.
  This setting works in combination with the setting of ODEV3~ODEV0 in Sub-Address 13H.

Sub-Address 13H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	ODEV3	ODEV2	ODEV1	ODEV0	ODDETPO	—	—	—
Default	0	0	0	0	0	—	—	—

- ODEV3~ODEV0: Sets the point (within 1H) where odd- or even-numbered field is identified.
  This setting works in combination with the setting of ODEV10~ODEV4 in Sub-Address 12H.

- ODDETPO: Sets polarity of pulse used to determine odd- or even-numbered field.

  0 (default): Not inverted 1: Inverted

Sub-Address 14H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	DIVIIC3	DIVIIC2	DIVIIC1	DIVIIC0	DIVHDSEL	HRESVAR	—	—
Default	0	0	0	0	0	0	—	—

- DIVIIC3~DIVIIC0: Switches the HPLL oscillation frequency. Enabled when CKSEL[3:0] (pins 72 to 75) are all set to 0.
  CKSEL[3:0] (pins 72 to 75) is enabled when DIVIIC3~DIVIIC0 is set to all 0s.

DIVIIC3	DIVIIC2	DIVIIC1	DIVIIC0	Clock Frequency	Horizontal Frequency
0	0	0	0	29.8 MHz	31.5 kHz, 480P
0	0	0	1	29.7 MHz	33.7 kHz, 1080I
0	0	1	0	29.7 MHz	45.0 kHz, 720P
0	0	1	1	27 MHz	31.5 kHz
0	1	0	0	29.8 MHz	15.7 kHz, 480I
0	1	0	1	—	—
0	1	1	0	—	—
0	1	1	1	27 MHz	15.7 kHz, general-purpose
1	0	0	0	—	External clock input
1	0	0	1	—	—
1	0	1	0	—	—
1	0	1	1	—	—
1	1	0	0	14.9 MHz	15.7 kHz (Note5)
1	1	0	1	—	—
1	1	1	0	—	—
1	1	1	1	13.5 MHz	15.7 kHz (Note6)

For Note5 and Note6, the clocks are generated by dividing the main clock by 29.8 MHz and 27 MHz respectively.

- DIVHDSEL: When using an internal HPLL, selects whether to use HDIN or the HPLL reference signal (generated internally) as HD in the logic block.
  0 (default): Uses the HPLL reference signal (internally generated) as HD in the logic block.
  1: Uses HDIN as HD in the logic block.

- HRESVAR: Selects whether reset values for built-in H-counters are to be set internally or externally
  0 (default): The reset values are set internally.
  1: The reset values can be set externally.

Sub-Address 17H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REG4	REG5	REG6	REG10	YDLY3	YDLY2	YDLY1	YDLY0
Default	0	0	0	0	0	0	0	0

- REG4: Sets the polarity of the control signal (CK2) for both Standard and Special 4:1:1 Modes. Changing the polarity enables the output order of Cb and Cr to be changed.
  0 (default): Polarity is not inverted.
  For Standard 4:1:1 Mode: Outputs in the order (b7, b6), (b5, b4), (b3, b2), (b1, b0).
  For Special 4:1:1 Mode: Outputs in the order (b3, b2, b1, b0), (b7, b6, b5, b4).
  1: Polarity is inverted.
  For Standard 4:1:1 Mode: Outputs in the order (b5, b4), (b7, b6), (b1, b0), (b3, b2).
  For Special 4:1:1 Mode: Outputs in the order (b7, b6, b5, b4), (b3, b2, b1, b0).

- REG5: Sets the polarity of the control signal for serial byte (R656 or R601 8-Bit Mode) processing. Changing the polarity enables the output order of Cb (Cr) and Y to be changed.
  0 (default): Polarity is not inverted. Outputs in the order Cb0, Y0, Cr0, Y1.
  1: Polarity is inverted. Outputs in the order Y0, Cb0, Y1, Cr0.

- REG6: Sets inversion/non-inversion of Cb and Cr MSB.
  0 (default): Cb, Cr MSB is not inverted. Straight binary output
  1: Cb, Cr MSB is inverted. Two's-complement output

- REG10: Sets the polarity of the control signal for Standard 4:1:1 Mode and Standard and Special 4:2:2 Modes.
  0 (default): Polarity is not inverted.
  For Standard 4:1:1 Mode: Outputs in the order (b7, b6), (b5, b4), (b3, b2), (b1, b0).
  For Standard and Special 4:2:2 Modes: Outputs in the order Cb, Cr, Cb, Cr.
  1: The polarity is inverted.
  For standard 4:1:1 Mode: Outputs in the order (b3, b2), (b1, b0) (b7, b6), (b5, b4).
  For Standard and Special 4:2:2 Modes: Outputs in the order Cr, Cb, Cr, Cb.

- YDLY3~YDLY0: Sets Y delay.

YDLY3	YDLY2	YDLY1	YDLY0	Y Delay
0	0	0	0	0 clocks
0	0	0	1	1 clock
—	—	—	—	
1	1	0	1	13 clocks
1	1	1	0	14 clocks
1	1	1	1	Invalid

Sub-Address 18H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REG11	LPFYPASS	LPI0ON2	LPI0ON1	LPI0ON0	LPQ0ON2	LPQ0ON 1	LPQ0ON0
Default	0	0	0	0	0	0	0	0

- REG11: Sets the sampling point when down-sampling Y signal.
  0 (default): Samples Y0, Y2 and Y4.
  1: Samples Y1, Y3 and Y5.

- LPFYPASS: Sets whether the Y signal passes or bypasses the LPF circuit.
  0 (default): The Y signal passes through the LPF circuit. System delay (9 clocks) is added by the LPF circuit.
  1: The Y signal bypasses the LPF circuit which adds a 1-clock delay.

- LPI0ON2~LPI0ON0: Sets whether the Cb signal passes or bypasses the LPF circuit.

LPI0ON2	LPI0ON1	LPI0ON0	
0	0	0	The Cb signal passes through the LPF circuit but is not filtered (9-clock delay is added).
0	0	1	Filter ON (6 MHz) (9-clock delay is added)
0	1	0	Invalid
0	1	1	Filter ON (2.8 MHz) (9-clock delay is added)
1	0	0	The Cb signal bypasses the LPF circuit (1-clock delay is added).
1	0	1	} Invalid
—	—	—	
1	1	1	

- LPQ0ON2~LPQ0ON0: Sets whether the Cr signal passes or bypasses the LPF circuit.

LPQ0ON2	LPQ0ON1	LPQ0ON0	
0	0	0	The Cb signal passes through the LPF circuit but the filter is not ON (9-clock delay is added).
0	0	1	Filter ON (6 MHz) (9-clock delay is added)
0	1	0	Invalid
0	1	1	Filter ON (2.8 MHz) (9-clock delay is added)
1	0	0	The Cb signal bypasses the LPF circuit (1-clock delay is added)
1	0	1	} Invalid
—	—	—	
1	1	1	

Sub-Address 19H

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REG9	REG7	REG8	QDSEL1	QDSEL0	IDSEL1	IDSEL0	LPYON
Default	0	0	0	0	0	0	0	0

- REG9: Sets the polarity of the signal used to control Y signal down-sampling and the signal used to control the Cr signal down-sampling rate (down-sampling using 1/2 or 1/4 the main clock).
- 0 (default): Down-samples the Y signal only in R656 or R601 Modes.
  Down-samples the Cr signal only in R656, R601 or 4:1:1 Modes using 1/4 the main clock.

  1: Down-samples the Y signal in all modes other than R656 or R601 Modes.
  Down-samples the Cr signal in all modes other than R656, R601, 4:4:4 or 4:1:1 Modes using 1/4 the main clock.

- REG7: Enables/Disables QDSEL0 for the Cr signal.
  0 (default): Disables QDSEL0.
  1: Enables QDSEL0.

- REG8: Enables/Disables QDSEL1 for the Cr signal.
  0 (default): Disables QDSEL1.
  1: Enables QDSEL1.

- QDSEL [1:0]: Sets the sampling point for when the Cr signal is down-sampled.

QDSEL1	QDSEL0	Sampling Using 1/2 the Main Clock	Sampling Using 1/4 the Main Clock
0	0	Cr0, Cr2, Cr4, …	Cr0, Cr4, Cr8, …
0	1	Cr1, Cr3, Cr5, …	Cr1, Cr5, Cr9, …
1	0	Unused	Cr2, Cr6, Cr10, …
1	1	Unused	Cr3, Cr7, Cr11, …

- IDSEL1~IDSEL0: Sets the sampling point for when the Cb signal is down-sampled.

IDSEL1	IDSEL0	Sampling Using 1/2 the Main Clock	Sampling Using 1/4 the Main Clock
0	0	Cb0, Cb2, Cb4, …	Cb0, Cb4, Cb8, …
0	1	Cb1, Cb3, Cb5, …	Cb1, Cb5, Cb9, …
1	0	Unused	Cb2, Cb6, Cb10, …
1	1	Unused	Cb3, Cb7, Cb11, …

- LPYON: Turns the Y LPF ON/OFF. Enabled only when LPFYPASS in Sub-Address 18H = 0.
  0 (default): Y LPF OFF
  1: Y LPF ON (6 MHz)

Sub-Address 1AH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REG12	—	—	—	—	—	—	—
Default	0	—	—	—	—	—	—	—

- REG12: Sets inversion/non-inversion of the Y MSB.
  0 (default): Does not invert the Y MSB. Straight binary output
  1: Inverts the Y MSB. Two's-complement output

Sub-Address 1BH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	REGSWR7	REGSWR1	REGSWG7	REGSWG3	REGSWG1	REGSWB7	REGSWB6	REGSWH
Default	0	0	0	0	0	0	0	0

- REGSWR7: Forces ROUT[7:2] to Input Mode.
  0 (default): Input and output settings depend on test mode.
  1: Forces ROUT[7:2] to Input Mode.

- REGSWR1: Forces ROUT[1:0] to Input Mode.
  0 (default): Input and output settings depend on test mode.
  1: Forces ROUT[1:0] to Input Mode.

- REGSWG7: Forces GOUT[7:4] to High-Impedance.
  0 (default): Output and High-Impedance settings depend on test mode.
  1: Forces GOUT[7:4] to High-Impedance.

- REGSWG3: Forces GOUT[3:2] to High-Impedance.
  0 (default): Output and High-Impedance settings depend on test mode.
  1: Forces GOUT[3:2] to High-Impedance.

- REGSWG1: Forces GOUT[1:0] to High-Impedance.
  0 (default): Output and High-Impedance settings depend on test mode.
  1: Forces GOUT[1:0] to High-Impedance.

- REGSWB7: Forces BOUT7 to High-Impedance.
  0 (default): Output and High-Impedance settings depend on test mode.
  1: Forces BOUT7 to High-Impedance.

- REGSWG6: Forces BOUT6~BOUT0 to High-Impedance.
  0 (default): Output and High-Impedance settings depend on test mode.
  1: Forces BOUT[6:0] to High-Impedance.

- REGSWHV: Forces HDOUT and VDOUT to Input Mode.
  0 (default): Input and output settings depend on test mode.
  1: Forces HDOUT and VDOUT to Input Mode.

Sub-Address 1CH

Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	M10B	—	—	CKOUTSTP	—	—	—	—
Default	0	—	—	0	—	—	—	—

- M10B: Sets 10-Bit Output Mode. Note that only two channels, Y ADC and Cb ADC, can be set to 10-Bit Output Mode.
  0 (default): 8-Bit Output Mode for all three channels
  1: 10-Bit Output Mode for two channels (Y and Cb)

- CKOUTSTP: Turns CKOUT output ON/OFF.
  0 (default): CKOUT output ON
  1: CKOUT output OFF. The output is High-Impedance.

Sub-Address 2AH

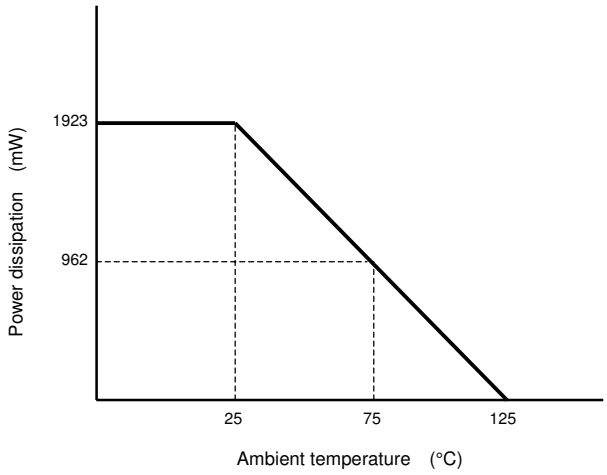
Bit	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Name	—	—	—	—	—	—	BAR	—
Default	—	—	—	—	—	—	0	—

- BAR: Sets Y, Cb and Cr signal output to internal color bar signal output (for testing purposes).
  0 (default): Normal operating mode
  1: Sets Y, Cb and Cr signal output to internal color bar signal output.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	V_{SS} to V_{SS} + 4.5	V
Input voltage	V_{IN}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	1923	mW
Storage temperature	T_{stg}	−55 to 125	°C

Ta-P_D (4-layer board mounting)



Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IN}	0	—	V_{DD}	V
Operating temperature	T_{opr}	−20	—	70	°C

DC Characteristics

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Current Dissipation		I_{DD}	—	—		200	—	mA
High-level input voltage	CMOS	V_{IH}	—	—	2.4	—	—	V
	Schmitt			—	2.65	—	—	
Low-level input voltage	CMOS	V_{IL}	—	—	—	—	0.9	V
	Schmitt			—	—	—	0.65	
Input current	High-level	I_{IH}	—	$V_{IN} = V_{DD}$	−10	—	10	μA
	Low-level	I_{IL}	—	$V_{IN} = V_{SS}$	−10	—	10	
Output voltage	High-level	V_{OH}	—	$I_{OH} = 4$ mA	2.4	—	—	V
	Low-level	V_{OL}	—	$I_{OH} = -4$ mA	—	—	0.4	

AC Characteristics

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Notes
Operating frequency condition	Fclk	—	—	—	—	30	MHz	—
Input set-up time	t_s	—	EXTCLK reference	1	—	—	ns	—
Input hold time	t_h	—	EXTCLK reference	7	—	—	ns	—
Clock data output phase difference 1	t_{data1}	—	EXTCLK input Output load = 30 pF	0	—	9	ns	CKPOL = 0 (CKOUT output and internal clock have Same polarity.)
Clock data output phase difference 2	t_{data2}	—	EXTCLK input Output load = 30 pF	0	—	7	ns	CKPOL = 0 (CKOUT output and internal clock have Same polarity.)
Clock data output phase difference 3	t_{data3}	—	EXTCLK input Duty = 50%, Output load = 30 pF	−18	—	−9	ns	CKPOL = 1 (CKOUT output and internal clock have Opposite polarity.)
Clock data output phase difference 4	t_{data4}	—	EXTCLK input, Duty = 50%, Output load = 30 pF	−18	—	−10	ns	CKPOL = 1 (CKOUT output and internal clock have Opposite polarity.)
Output signal delay time 1	t_{pd1}	—	—	6	—	17	ns	CKPOL = 0 (CKOUT output and internal clock have Same polarity.)
Output signal delay time 2	t_{pd2}	—	—	23	—	35	ns	CKPOL = 1 (CKOUT output and internal clock have Opposite polarity.)
Output signal delay time 3	t_{pd3}	—	—	8	—	23	ns	—
Output signal delay time 4	t_{pd4}	—	—	8	—	22	ns	—

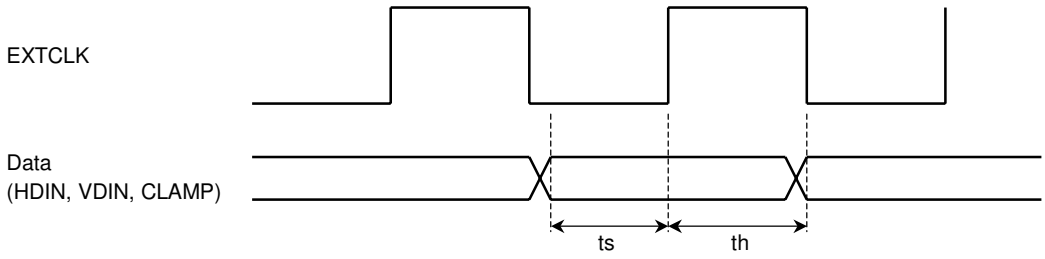
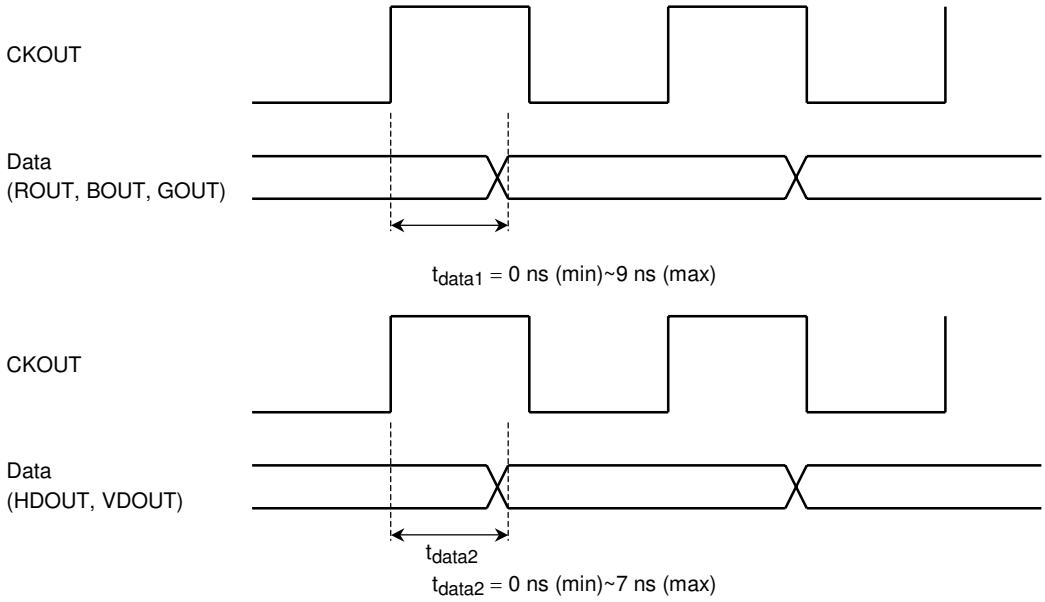


Figure 6 Data Set-up Hold Time

(1) Same polarity output of CKOUT (CKPOL = 0, default, set by I^2C bus register)



(2) Inverted-polarity output of CKOUT (CKPOL = 1, clock duty = 50%, set by I^2C bus register)

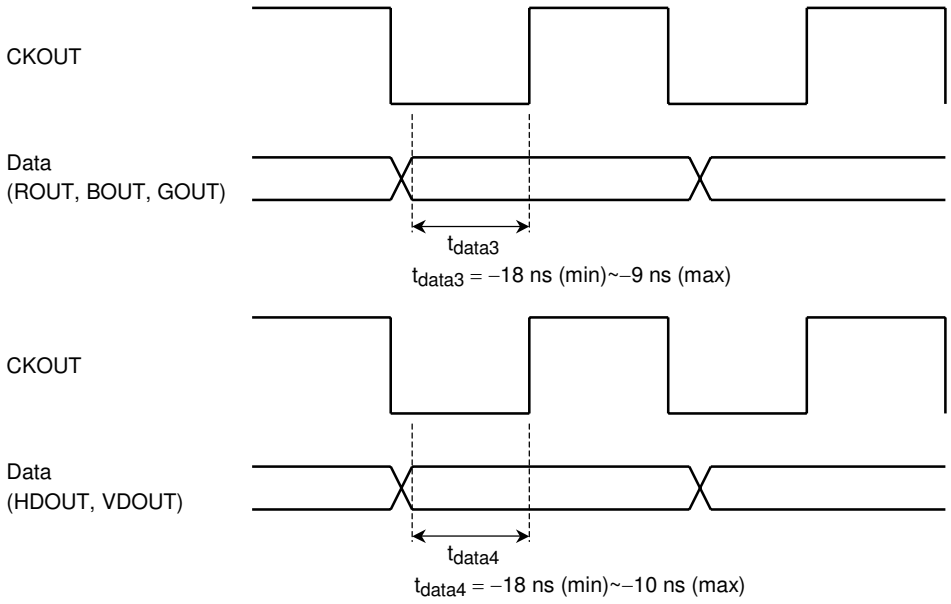
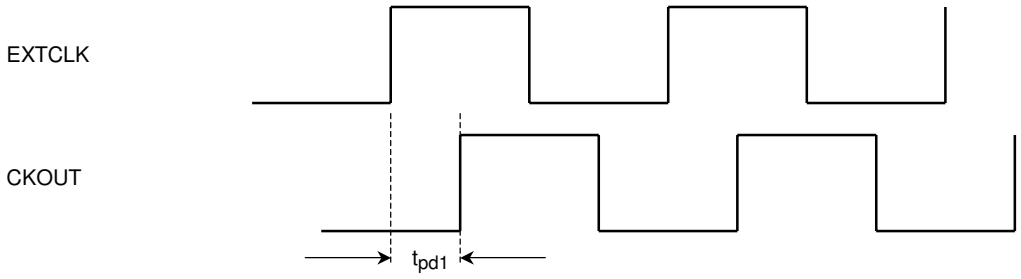


Figure 7 Phase Difference between Clock and Data Output

(1) Same polarity output of CKOUT (CKPOL = 0, default, set by I^2C bus register)



(2) Inverted-polarity output of CKOUT (CKPOL = 1, set by I^2C bus register)

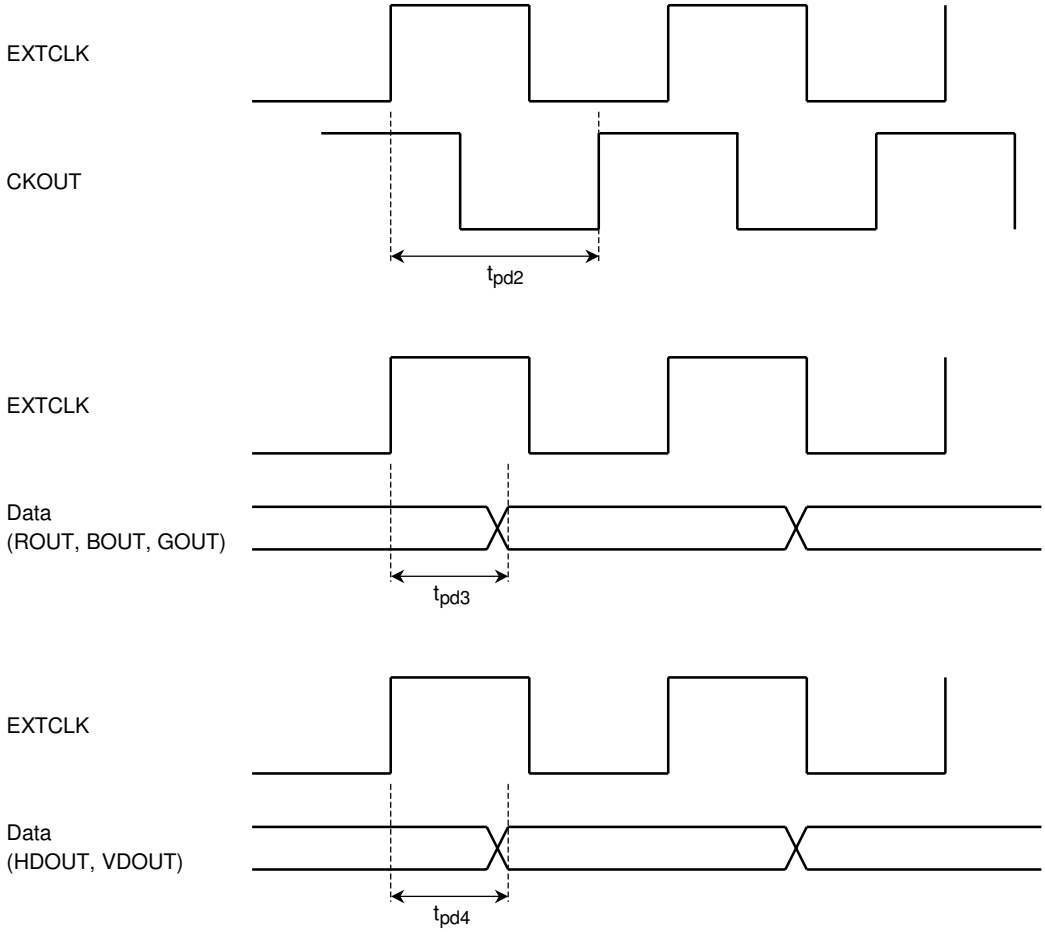


Figure 8 Output Signal Delay Time

Note7: When the clock duty (TC90A58F internal clock duty) changes, the output signal delay times t_{pd3} and t_{pd4} (when CKPOL = 1) change only by CKOUT output delay. Thus, the phase difference between CKOUT and the data changes by the change in the CKOUT output delay.

The TC90A58F internal clock is the output from the CKOUT pin when CKPOL = 0 (default).

Electrical Characteristics of ADC Block (f_{clk} = 30 MHz, A_{VDD} = 3.3 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Note
Input voltage level	VAD^{in}	—	—	—	1.32	—	V_{p-p}	—
Conversion speed	f_{clk}	—	—	—	—	30	MHz	—
Analog input band	BW	—	80% amplitude input −1dB	—	10	—	MHz	—
Differential non-linear error	ED	—	—	—	±1.5	—	LSB	10-bit conversion value
Integral non-linear error	EL	—	—	—	±4	—	LSB	10-bit conversion value
Zero-scale error	V_{zd}	—	—	Theoretical value	—	Theoretical value	mV	$V_{DD} \times 0.3$ (zero-scale theoretical value)
				−10	—	+50		
Full-scale error	V_{fd}	—	—	Theoretical value	—	Theoretical value	mV	$V_{DD} \times 0.7$ (full-scale theoretical value)
				−50	—	+10		
Input capacity	C_{in}	—	—	—	6.5	—	pF	—

Electrical Characteristics of HPLL Block

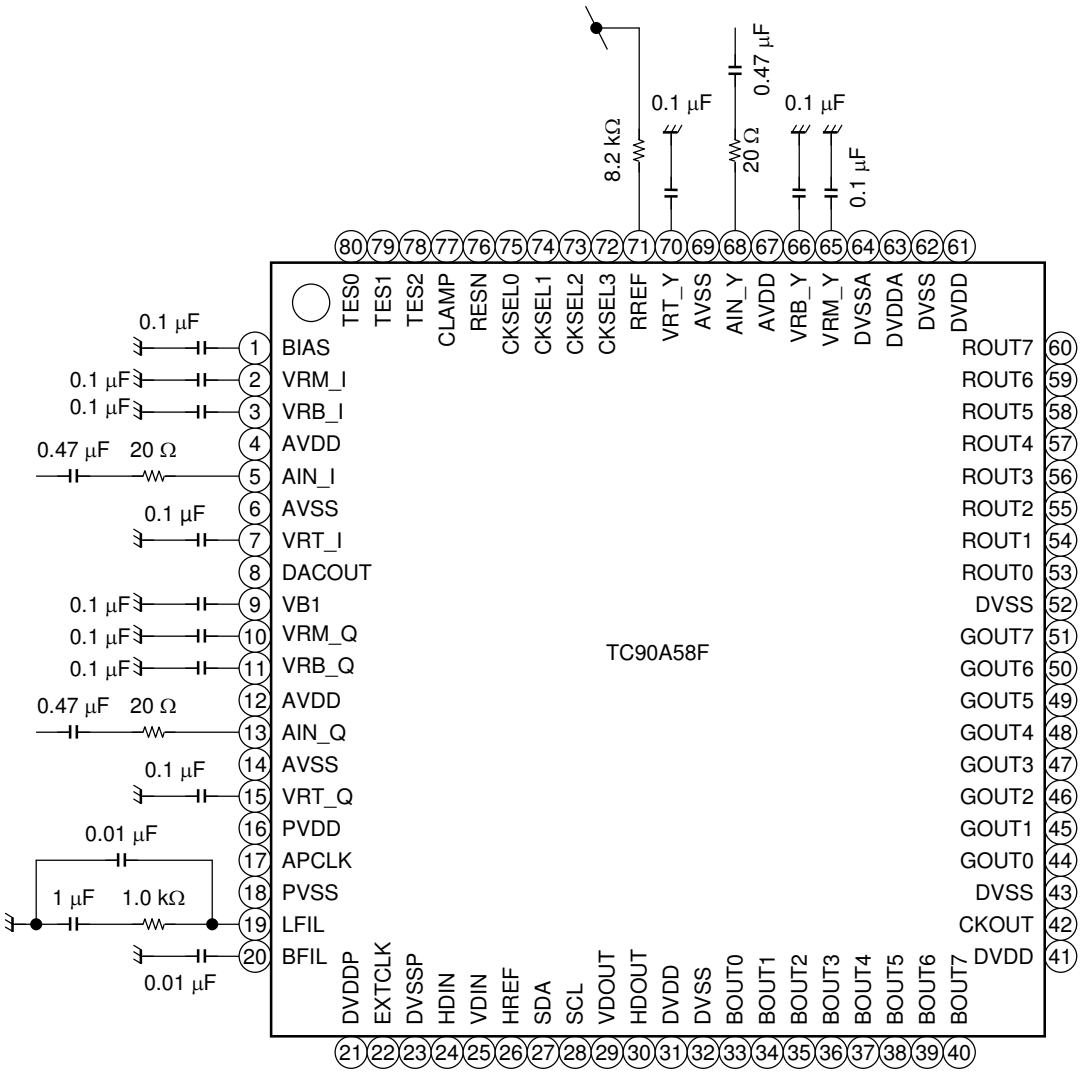
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Note
Output frequency range	fu	—	—	27	—	29.82	MHz	See table below (Note9)
Jitter	tjit	—	480i mode	—	8 (Note8)	—	ns	—
			720p mode	—	6 (Note8)	—		

Note8: The jitter value depends to a large extent on the circuit layout on the board and the constants for the external circuits. It is also affected by external devices. Take care when designing the pattern for the board.

Note9: Oscillation frequencies for each screen mode are as listed below.

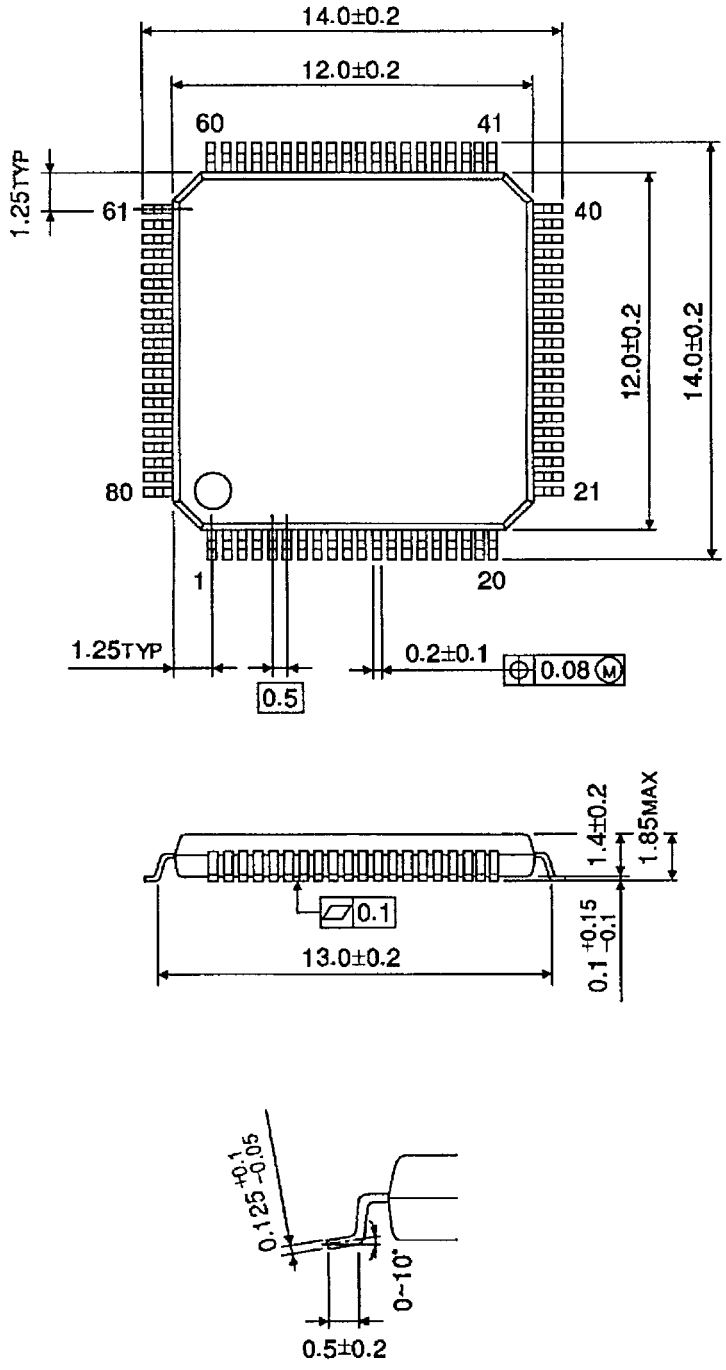
Screen Mode	fH (kHz)	Times	Oscillation Frequency
480i	15.75	1896	29.82 MHz
480p	31.5	948	29.82 MHz
1080i	33.7	880	29.7 MHz
720p	45	660	29.7 MHz
R656, R601 (NTSC)	15.734	1716	27 MHz
R656, R601 (PAL)	15.625	1728	27 MHz

Application Circuit Example



Package Dimensions

LQFP80-P-1212-0.50A Unit : mm



Weight: g (typ.)

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