

TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

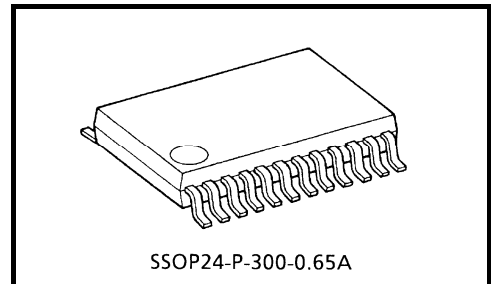
TB31373FNG

Single Chip Receiver IC

The TB31373FNG, which realizes a reception block on a single chip, can greatly reduce the number of components comprising most functions (i.e. RF block, IF block, VCO block, PLL block), and allows for thinner, smaller devices.

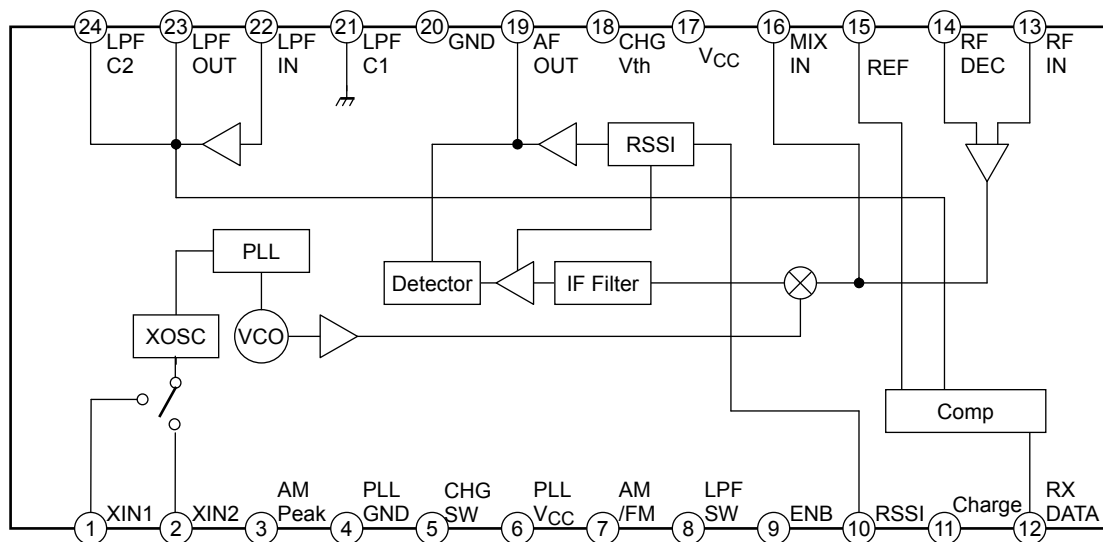
Features

- Application: Remote keyless entry (remote door lock and unlock of equipment), low tire pressure detector of equipment, remote controller, etc
- RF: 434 MHz, IF: 220 kHz
- Combines LNA, image rejection MIX, IF, PLL, VCO, detector circuit, and comparator block onto a single chip
- Operating voltage range: $V_{CC} = 3.6$ to 5.5 V
- Current consumption: $I_{CC} = 6.4$ mA (AM mode, $V_{CC} = 5.0$ V)
 $I_{CC} = 6.6$ mA (FM mode, $V_{CC} = 5.0$ V)
- Current consumption during BS: 0 μ A (typ.)
- On-chip IF filter, detector circuit
- Package: 24-pin SSOP (0.65-mm pitch)



Weight: 0.14 g (typ.)

Block Diagram



Note: There are cases where content such as a function block, circuit, or constant will be partially omitted or simplified in block diagrams to facilitate the explanation of functions in the diagram.

Pin Functions (all the values (resistance, capacity, etc.) shown in the internal equivalent circuit diagram are typical values.)

Pin No.	Pin Name	Description	Internal Equivalent Circuit
1	XIN1	Locally generated reference clock pin	
2	XIN2	Locally generated reference clock pin	
3	AM Peak	Peak hold pins when in the AM mode (for CHARGE2) Please set open when not using this pin.	
4	PLL GND	GND pins for the PLL and VCO blocks	—
5	CHG SW	CHARGE2 setting SW pin. This pin is also used as the test pin. Do not perform V _{CC} (Hi) processing on this pin.	
6	PLL V _{CC}	PLL, VCO block power pin	—
7	AM/FM	AM/FM switching SW pin. High: FM mode Low: AM mode Do not set open.	

The equivalent circuit diagram for the pin periphery is intended to aid in understanding the connected external circuit design, not to precisely describe the internal circuit.

Pin No.	Pin Name	Description	Internal Equivalent Circuit
8	LPF SW	Bit rate filter switching SW pin. High: High bit rate Low: Low bit rate Is also used as the X1/X2 control SW. Do not perform open processing on this pin.	
9	ENB	ENABLE pin. (IC operation ON/OFF control pin) High: Circuit operation ON Low: Circuit operation OFF mode Do not set open.	
10	RSSI	RSSI output pin	
11	CHARGE	Quick charge circuit control pin. (For CHARGE1) Please attach a capacitor when using this pin. Please set open when not using this pin.	
12	RX DATA	AM/FM waveform output pin. This pin is used for open collector output. Connect pull-up resistance to this pin.	
13	RF IN	RF signal input pin	
14	RF DEC	RF decoupling pin	

The equivalent circuit diagram for the pin periphery is intended to aid in understanding the connected external circuit design, not to precisely describe the internal circuit.

Pin No.	Pin Name	Description	Internal Equivalent Circuit
15	REF	Data comparator REF pin.	
16	MIX IN	This pin is also used as an RF signal output pin and a mixer input pin.	
17	VCC	Power pin	—
18	CHG Vth	Quick charge circuit threshold setting pin when in the FM mode (for CHARGE2). Please set open when not using this pin.	
19	AF OUT	Detection output pin	
20	GND	GND pin	—

The equivalent circuit diagram for the pin periphery is intended to aid in understanding the connected external circuit design, not to precisely describe the internal circuit.

Pin No.	Pin Name	Description	Internal Equivalent Circuit
21	LPF C1	Bit rate filter pin. (For low bit rate)	
22	LPF IN	Bit rate filter input pin.	
23	LPF OUT	Bit rate filter output pin.	
24	LPF C2	Bit rate filter output pin. (For low bit rate)	

The equivalent circuit diagram for the pin periphery is intended to aid in understanding the connected external circuit design, not to precisely describe the internal circuit.

Overview

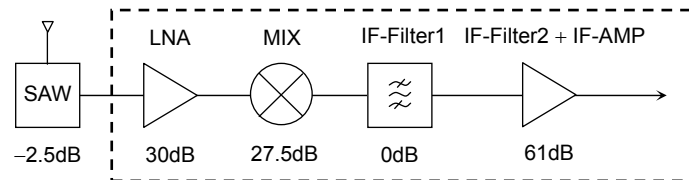
1. V_{CC}, GND Supply Block Distribution

This is the block distribution of each V_{CC} and GND pin. Because elements such as protection diodes are connected inside the IC, please use each V_{CC} pin with identical power sources so the same electrical potential results. Also, even when using identical power sources, note that there must be no electrical potential difference between these pins. To ensure that this is the case, take measures such as mounting a bypass capacitor next to each V_{CC} pin having the same capacitance value.

V _{CC}	GND	Block
V _{CC}	GND	LNA, MIX, IF-AMP, RSSI, FIL-AMP, DATA-COMP, Detector
PLL-V _{CC}	PLL-GND	VCO, PLL, XOSC

2. Gain Distribution

The following diagram shows the distribution of each gain during reception. Each value is treated as a rough design target value.



Functions

1. LNA Current Regulation

The current consumption and gain of LNA can be regulated by changing resistance R in the following diagram. When $R = 1\text{ k}\Omega$, the consumption current is about $600\text{ }\mu\text{A}$.

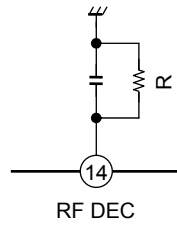


Figure 1

2. LNA Gain

The design value is 30dB.

3. Locally Oscillating Oscillators

Local oscillation circuits in this product have on-chip capacitance. Please use quartz oscillators with a load capacitance of 8 pF.

4. Local Oscillation External Injection Method

When inputting an external oscillation frequency from pin 1, set the pin 1 signal level to 95 to 110dB μ V. Set the pin 2 GND for external injection only from pin 1.

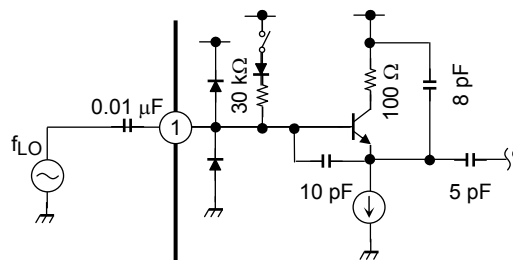


Figure 2

5. IF Filter Block

Under the standard conditions for this IC, signals are converted into 220 kHz signals in the mixer block then are input to the IF block. The frequency MIX(in) which is input from the mixer input pins is 433.9192 MHz and the local frequency is 40.6593 MHz.

This IC has an on-chip IF filter, but does not have any output pins. To measure the IF filter characteristics, measure the RSSI voltage at the RSSI pin. The frequency characteristics of the RSSI block are included in the IF filter characteristics explained in this document.

The center frequency of the standard IF filter characteristics is 220 kHz, -3dB bandwidth is 300 kHz.

Figure 3 shows the IF filter characteristics. The filter deviation is about ±10%.

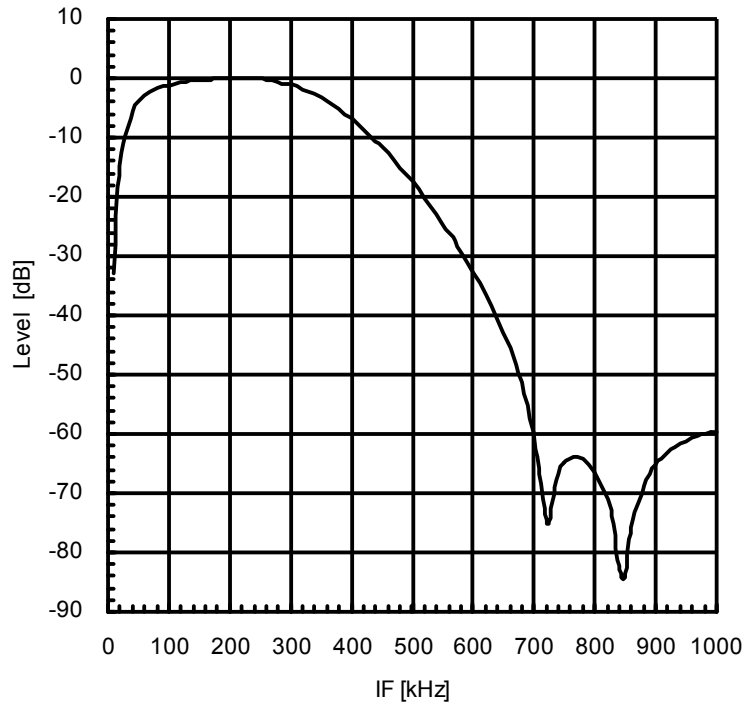


Figure 3

6. Detection Circuit

Detection is performed using the quadrature detection method. The detector is built into the IC and doesn't require an external ceramic discriminator. Demodulation output is kept at a fixed level since adjustment can't be made using the dumping resistor.

7. Bit Rate Filter

The standard bit rate is 600 bps. Therefore, the FSK bit rate filter is a 600-bps 2nd order filter. Using a 3rd order filter is also possible. When using a bit rate other than 600 bps, please change the filter constant. You can also use two types of filters and switch between them. When switching, pin 21 and pin 24 are used for the low bit rate. (However, only 2nd order filters can be used when switching filters.)

The LPF SW is used to switch the bit rate between FSK bit rate filters. However, if you are switching the bit rate between FSK and ASK, use the AM/FM SW.

Additionally, the bit rate filter is Manchester encoded.

- Bit rate switching

Bit Rate Switching Mode Switching	Low Bit Rate		High Bit Rate	
	AM/FM SW	LPF SW	AM/FM SW	LPF SW
ASK/ASK	Low	Low	Low	High
FSK/FSK	High	Low	High	High
FSK/ASK	High	Low	Low	High
ASK/FSK	Low	Low	High	High

Note: If you use the ASK/FSK mode, AM/FM SW and LPF SW can use connect.

- (1) ASK bit rate filter

The current ASK bit rate filter is a 600-bps 2nd order filter. When using a bit rate other than 600 bps, please change the filter constant.

Table 1 2nd Order Bit Rate Filter Reference Constant (Manchester encoded)

	R4	R2	C6	C8
600 bps	68 kΩ	68 kΩ	4700 pF	1500 pF
1200 bps	68 kΩ	68 kΩ	2200 pF	680 pF
2400 bps	68 kΩ	68 kΩ	1000 pF	390 pF
4800 bps	68 kΩ	68 kΩ	560 pF	180 pF
9600bps	68 kΩ	68 kΩ	270 pF	82 pF

- (2) FSK bit rate filter

The current FSK bit rate filter is a 600-bps 2nd order filter. When using a bit rate other than 600 bps, please change the filter constant.

Table 2 2nd Order Bit Rate Filter Reference Constant (Manchester encoded)

	R4	R2	C6	C8
600 bps	68 kΩ	68 kΩ	4700 pF	1500 pF
1200 bps	68 kΩ	68 kΩ	2200 pF	680 pF
2400 bps	68 kΩ	68 kΩ	1000 pF	390 pF
4800 bps	68 kΩ	68 kΩ	560 pF	180 pF
9600 bps	68 kΩ	68 kΩ	270 pF	82 pF

(3) Switching 2nd order bit rate filters (Manchester encoded)

When using E12 series capacitors:

- Only 2nd order filters can be switched when switching bit rate filters
- Bit rate filter constants are simulation values. These values have not been confirmed through actual measurement.
- Cut-off frequency (demodulation frequency \times 1.5/demodulation frequency \times 1.5)

Table 3 2nd Order Bit Rate Filter Reference Constant (Manchester encoded)

	R4	R2	C6	C8	C3	C9
600 bps / 4800 bps	68 k Ω	68 k Ω	560 pF	180 pF	3900 pF	1500 pF
600 bps / 9600 bps	68 k Ω	68 k Ω	270 pF	82 pF	4700 pF	1500 pF
1000 bps / 4800 bps	68 k Ω	68 k Ω	560 pF	180 pF	2200 pF	820 pF
1000 bps / 9600 bps	68 k Ω	68 k Ω	270 pF	82 pF	2700 pF	820 pF
1200 bps / 4800 bps	68 k Ω	68 k Ω	560 pF	180 pF	1800 pF	560 pF
1200 bps / 9600 bps	68 k Ω	68 k Ω	270 pF	82 pF	2200 pF	680 pF
2400 bps / 4800 bps	68 k Ω	68 k Ω	560 pF	180 pF	560 pF	180 pF
2400 bps / 9600 bps	68 k Ω	68 k Ω	270 pF	82 pF	820 pF	270 pF

Note: The cut-off frequency is only set to demodulation frequency \times 2.0 for FSK when the transfer rate is 9600 bps.

8. Quick Charge/Discharge Circuit (CHARGE pin)

The CHARGE pin (pin 11)/ the CHG Vth pin (pin 18)/ the AM Peak pin (pin 3) are quick charge/discharge pins. There are two types of quick charge/discharge function: CHARGE1 and CHARGE2. Switching is made possible by combining the control of the CHG SW pin (pin 5) and the LPF SW pin (pin 8).

The CHARGE1 function uses a time constant between the internal resistors and external capacitors to automatically quick charge/discharge the REF pin (pin 15) for a constant period of time. The CHARGE pin (11 pin) is control terminal for quick charge time. This function can be used by attaching capacitors, so be sure to attach capacitors with the same capacity as the REF pin (pin 15) during normal operation.

External capacitors with a capacitance (C20) of 0.1 μ F are used, and the quick charge time is set to about 8 ms.

The control ways of the CHARGE2 function are different between in the AM mode and FM mode.

The CHARGE2 function quick charges/ discharges the REF pin (pin 15) when the difference between the input signal and the REF pin (pin 15) voltage exceeds the range of the threshold ($-V_{chgth}$ to $+V_{chgth}$).

When in the FM mode, the threshold is determined by the external resistance Rchgth (R9) of the CHG Vth pin (pin 18).

For external resistance Rchgth of the CHG Vth pin (pin 18), use resistance which is considered variation of receiver and transmitter signal and within the range from 33 k Ω to 150 k Ω .

Threshold V_{chgth} equation:

$$V_{chgth} = 1.2 \times \frac{10k}{R_{chgth} + 1k} \quad (V)$$

To adjust the threshold V_{chgth} , check the swing of REF pin (pin 15) voltage in CHARGE2 mode. If the REF pin (pin 15) voltage is big, start-up time of IC will be quick but it is disadvantage for receiver sensitivity.

To switch the bit rate between CHARGE2 functions when in the FM mode, add a switch to the external Rchgth resistance of the CHG Vth pin (pin 18).

The threshold is determined inside the IC when in the AM mode.
 Please attach capacitor according to bit rate, and with 1/3 capacity at the AM Peak pin (pin 3) as the REF pin (pin 15).

Table 4 Reference Constant (Manchester encoded)

Bit Rate	C4
9600 bps	0.022 μ F
4800 bps	0.047 μ F

9. RSSI Function

Direct current potential is output to the RSSI pin according to the input level of the IF AMP. Because the RSSI output is converted into voltage by internal resistance, you can change the slope of the RSSI output by connecting external resistor R . In this case however, note that the difference in temperature coefficient between external resistor R and the IC-internal resistors might cause the temperature characteristics of the RSSI output to change.

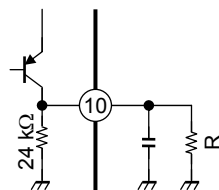


Figure 4

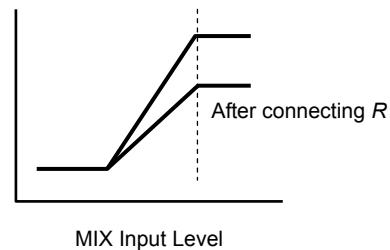


Figure 5

10. PLL Block

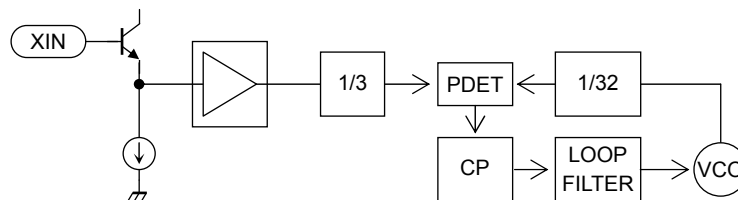


Figure 6

The PLL is composed of 1/32 fixed dividing prescalers. Additionally, it is equipped with third order loop filters. The charge pump current is 6.2 μ A.

Loop Filter

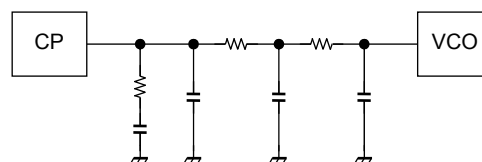


Figure 7

11. VCO Block

This balanced oscillation type block has built-in oscillation transistors and variable capacitor diodes. Oscillation frequency: 434 MHz band.

12. Control Pins

(1) ENABLE bits

These are the bits that perform ENABLE control on the entire circuit. Set Enable to “High” after VCC has completely powered up.

ENABLE	Circuit
High	ON
Low	BS

(2) AM/FM switch

AM/FM	Modulation
High	FM mode
Low	AM mode

(3) LPF switch

This bit controls the bit rate filter that is used. Please select this bit according to the bit rate. Select the bit rate even when using the bit rate filter as a fixed filter, and select the bit according to the local oscillation (XIN1/2). However, please set LPF C1 (pin 21) and LPF C2 (pin 24) to “Open”.

LPF SW	Bit Rate	XIN Operation Mode	
		XIN2: GND	XIN2: Mount
High	High bit rate	XIN1	XIN2
Low	Low bit rate	XIN1	XIN1

Note : When not switching bit rate, it is possible to set XIN2 to “OPEN”.

(4) CHARGE switch

CHG SW	LPF SW	CHARGE2 Operation Mode	CHARGE1 Operation Mode
OPEN	High	ON	OFF
	Low	OFF	ON* ¹
Lo	High	ON	OFF
	Low	ON	ON* ¹
High	Test mode* ²		

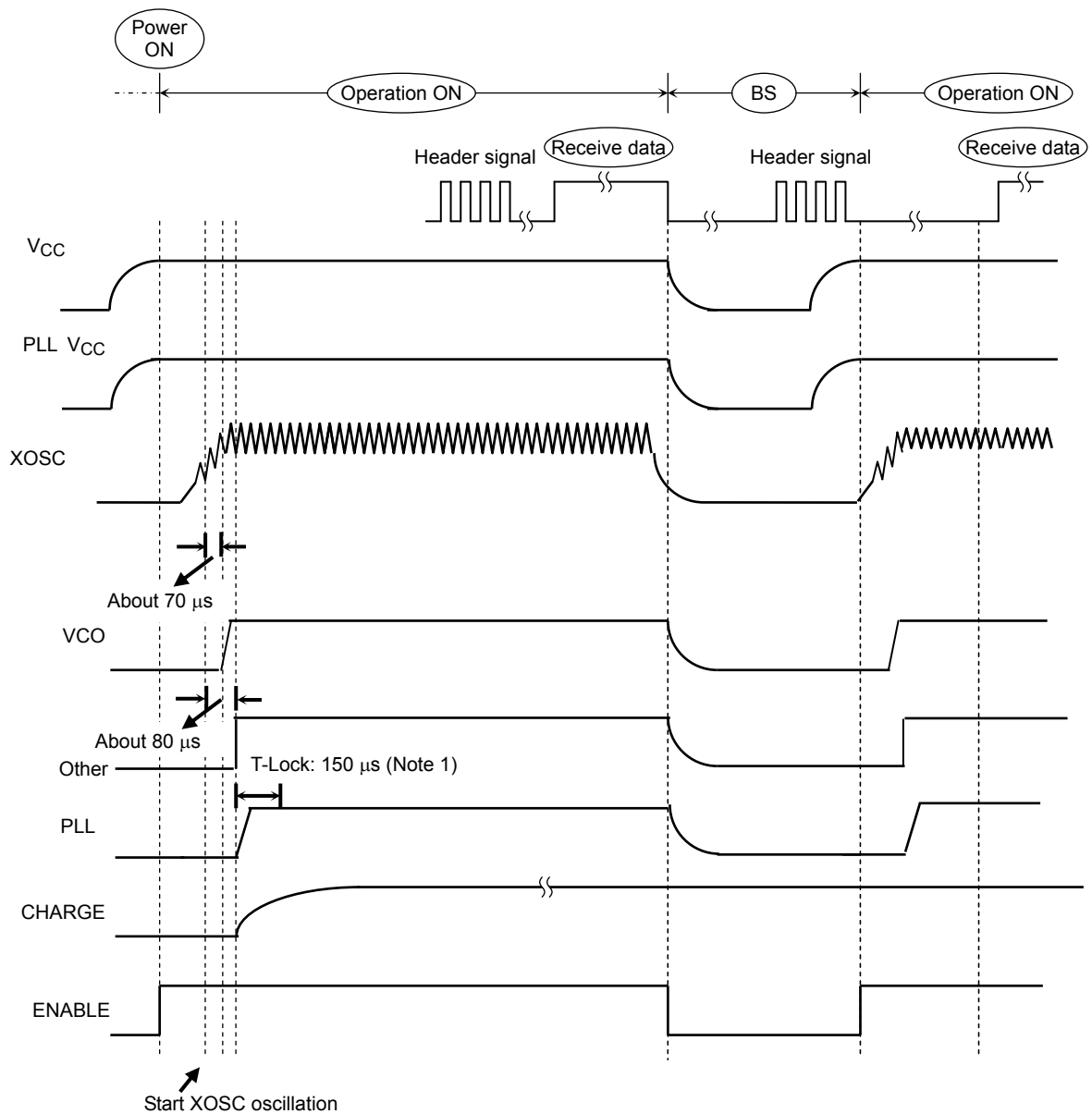
Note 1: When not using CHARGE1, set the CHARGE pin (pin 11) to “OPEN”.

Note 2: Do not set CHG SW (pin 5) to High.

Example of controlling pins

Bit Rate selection	X1/ X2 selection	XIN1	XIN2	LPF SW	LPF C1/ C2
Use	Use	Mount	Mount	H / L	Mount
Use	Unnecessary	Mount	GND	H / L	Mount
Unnecessary	Use	Mount	Mount	H / L	OPEN
Unnecessary	Unnecessary	Mount	OPEN	L	OPEN

Control Timing Chart



Note : There are cases where content such as a function block, circuit, or constant will be partially omitted or simplified in block diagrams to facilitate the explanation of functions in the diagram.

Note 1: "T-Lock" in the above diagram represents the time within which the PLL clock frequency converges to within ± 1 kHz of the set value.

Cautions for Designing Circuit Board Patterns

Observe the following cautions when designing circuit patterns for this product.

Local Oscillation Circuit (Pins 1, 2)

- This circuit must be sufficiently isolated from the LNA block.
- The local oscillation circuit must be isolated so that it will not affect into the mixer input.
- The GND of the local oscillation circuit portion must be connected using narrow lines.
- When using two crystal oscillators, be sure to sufficiently isolate each oscillator.

Data Output Block (Pin 12)

- Be sure to isolate the output pattern so the output will not affect other circuits and no noise will be generated from any stages following the data output stage.

LNA Circuit Block

- (1) Prevent LNA oscillation
 - Be sure that the patterns do not get too close to the patterns of the RF input block (pin 13) and the RF-DEC block (pin 14).
 - Isolate the patterns of the input block (pin 13) and the output block (pin 16).
 - Design the RF input lines to be as narrow as is practical.
 - Be sure there are plenty of GND patterns between the RF-IN (pin 13) and RF-DEC (pin 14).
- (2) Secure gain
 - To secure ample LNA gain, be sure to select the optimum value for the input matching circuit (pin 13) in accordance to the die pattern.

IC mounting block

- Be sure to provide GND underneath the mounted IC and prepare relatively many through holes.

Cautions for Mounting

- Do not mount the IC incorrectly. Incorrect mounting may result in failure, damage and/or degradation to the IC and other devices used with the IC.
- Make connection to the power pins as close as possible to prevent voltage differences in the bypass capacitor. In addition, be sure to use the correct type of capacitor with the correct capacity rating.

About solderability, following conditions were confirmed

- Solderability
 - (1) Use of Sn-37Pb solder Bath
 - solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

Absolute Maximum Ratings (the temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	6.0	V
Power dissipation	P _D	780	mW
Input pin voltage	AM/FM, LPF SW, ENB, CHG SW	6.0	V
Storage temperature range	T _{stg}	-55 to 150	°C

The absolute maximum rating is a technical specification that must never be exceeded, even for an instant. Please do not operate at conditions which exceed this technical specification.

Operating Ranges (the temperature for unspecified temperature ranges is Ta = 25°C; voltage is ground referenced.)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Power operating voltage range	V _{CC}	—	—	3.6	5.0	5.5	V
Operating temperature range	T _{opr}	—	—	-40	25	85	°C
RF operating frequency range	F _{RF}	—	IF = 220 kHz	430	433.9192	435	MHz
XIN setting range	OSC	—	IF = 220 kHz	40.2919	40.6593	40.7606	MHz

The operating range indicates the conditions under which basic functional operation is possible even when there are fluctuations in the electrical characteristics of a device.

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, V_{CC} = 5.0 V, fin (RF) = 433.9192 MHz, fin (Lo) = 40.6593 MHz, Dev = ±20 kHz, CHG SW = Open, AM/FM = H, LPF SW = L, ENB = H).

RF + IF Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Current consumption when no signal (ASK mode)	I _{CC} (ASK)	2 (1)	V(Lo) = 110dBμV	4.8	6.4	8.0	mA
Current consumption when no signal (FSK mode)	I _{CC} (FSK)	2 (2)	V(Lo) = 110dBμV	4.9	6.6	8.2	mA
Power consumption in battery saving mode	I _{CCO}	2 (3)	ENB = L	—	0	5	μA
LNA gain 1	G _V (RF) 1	1 (6)	50 Ω I/O	-9	-6	-3	dB
IF (L) band	IF _L	1 (1)	fo-3dB, RSSI pin (pin 10)	—	60	80	kHz
IF (H) band	IF _H	1 (1)	fo-3dB, RSSI pin (pin 10)	300	360	—	kHz
RSSI output voltage 1	V _{RSSI1}	1 (1)	V _{in} (MIX) = 25dBμVEMF AM/FM = L	0.25	0.5	0.75	V
RSSI output voltage 2	V _{RSSI2}	1 (1)	V _{in} (MIX) = 50dBμVEMF AM/FM = L	1	1.3	1.6	V
RSSI output voltage 3	V _{RSSI3}	1 (1)	V _{in} (MIX) = 80dBμVEMF AM/FM = L	1.85	2.2	2.55	V
RSSI output resistance	R _{RSSI}	1 (9)	—	18	24	30	kΩ
Detection output level	V _{OD}	1 (3)	Dev. = ±20 kHz V _{in} (MIX) = 60dBμVEMF	73	94	115	mVrms
CHARGE2 current	I _{CHG2}	—	—	0.6	0.95	1.3	mA
Peak hold input resistance	R _{PEAK}	1(10)	—	75	100	125	kΩ
Peak hold current	I _{PAEK}	—	—	170	260	350	μA

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Peak hold voltage	V _{PAEK}	—	AM Peak pin (pin 3), -5 μ A input	-140	-115	-90	mV
CHARGE2 threshold (FSK mode)	V _{THFM}	—	R ₉ = 100 k Ω Pin REF(pin 15), $\pm 5\mu$ A input	185	245	305	mVp-p
CHARGE2 threshold (ASK mode)	V _{THAM}	—	Pin LPF IN(pin 22), 0.8V input Pin REF(pin 15), $\pm 5\mu$ A input	165	220	275	mVp-p
Waveform shaping output duty rate	DR	1 (2)	V _{in} (MIX) = 60dB μ VEMF Single tone	45	50	55	%
Comparator input resistance	R _{COMP}	1 (10)	—	75	100	125	k Ω
Switchover switch pin input level	V _{IL}	—	AM/FM, LPF SW, ENB pins	0	—	0.2	V
Switchover switch pin input level	V _{IH}	—	AM/FM, LPF SW, ENB pins	2.0	—	5.5	V
DATA output voltage (L level)	V _{DATAL}	1 (7)	I _{DATAL} = 200 μ A	—	—	0.4	V
DATA output leak current (H level)	I _{DATAH}	1 (8)	—	—	0	2	μ A

Reference Characteristics Data*

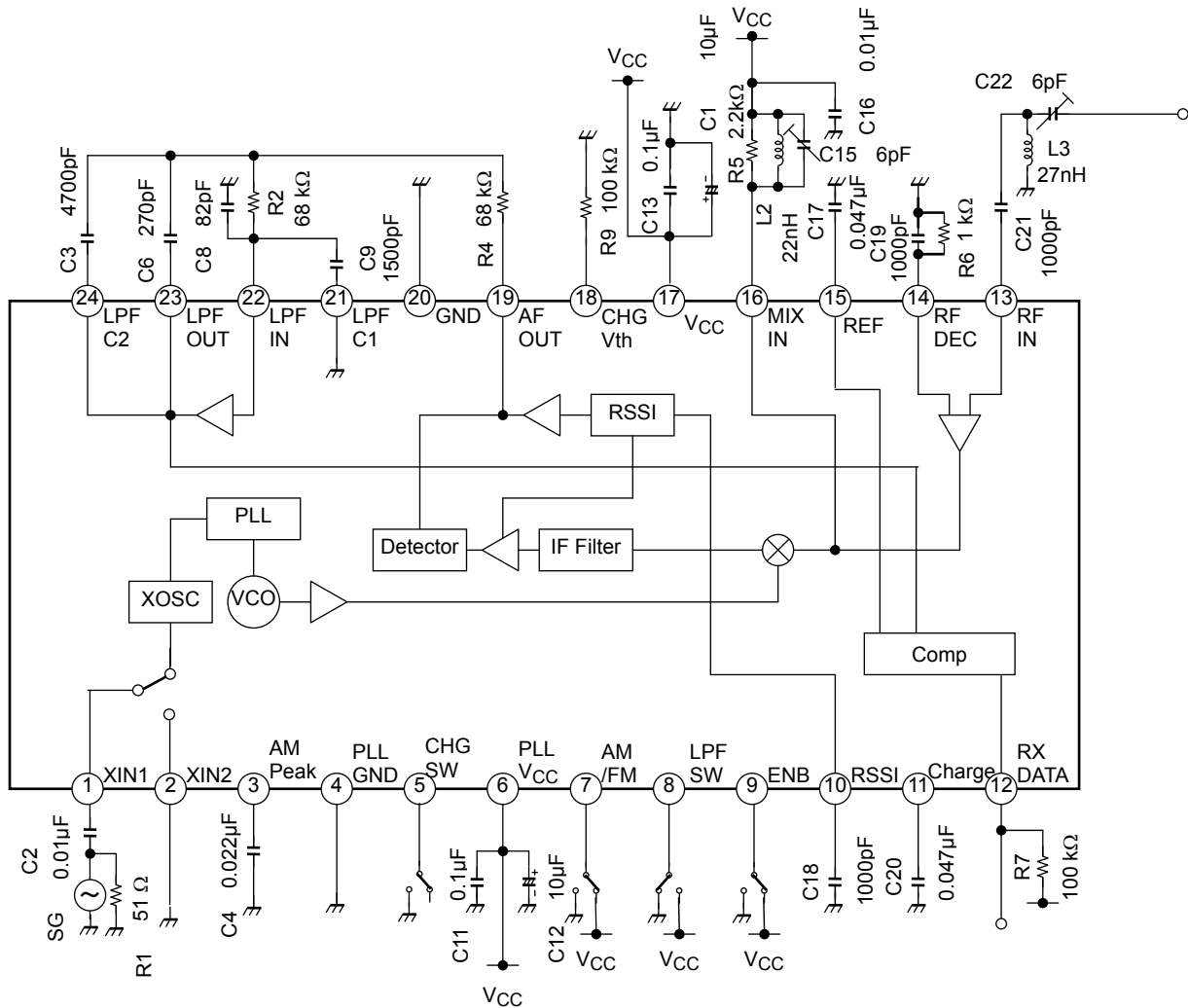
Characteristics	Symbol	Test Circuit	Test Condition	Typ.	Unit
Reception sensitivity (12dB SINAD)	12dB SINAD	1(4)	600 bps (Manchester) No SAW filter, dev = ± 20 kHz	0	dB μ V EMF
LNA gain 2	G _V (RF) 2	—	V _{in} (RF) = 50dB μ V	30	dB
LNA input capacitance	C (RF) IN	—	—	2	pF
LNA input resistance	R (RF) IN	—	—	1.2	k Ω
Mixer conversion gain	G _V MIX	—	V _{in} = 50dB μ V	27.5	dB
Mixer input resistance	R MIX	—	LNA OFF	0.8	k Ω
Mixer input capacitance	C MIX IN	—	LNA OFF	2.5	pF
Mixer interception points	IP3	—	—	96	dB μ V
Mixer 1dB compression	1dB comp	—	Input conversion value	85	dB μ V
Image reduction ratio	I _{RR}	—	—	35	dB
IF amp gain	G _V (IF)	—	—	61	dB
Signal to noise ratio 1	S/N1	1(5)	V _{in} (mix) = 30dB μ V, V(Lo) = 110dB μ V, 600 bps (Manchester)	35	dB
Signal to noise ratio 2	S/N2	1(5)	V _{in} (mix) = 60dB μ V, V(Lo) = 110dB μ V, 600 bps (Manchester)	53	dB
Rising time	T	—	CHARGE2, 9600bps (Manchester), dev= ± 20 kHz, Time from Vcc ON to Duty more than 40%	1	ms
VCO phase noise	C/N	—	@500 kHz detuning points	-90	dBc/Hz
VCO conversion sensitivity	V _{VIN1}	—	VCO Frequency: 434 MHz band	80	MHz/V
Lockup time	PLL lock	—	Local external implantation	150	μ s
LPFC1SW pin ON resistance	R _{SW}	—	V _{SW} = 0.2 V	700	Ω

Note that this item contains reference values and does not contain any guaranteed values.

Unit: dB μ V indicates the load terminal display. (0dBm = 107dB μ V = 113dB μ VEMF @ 50 Ω)

Typical Test Circuit

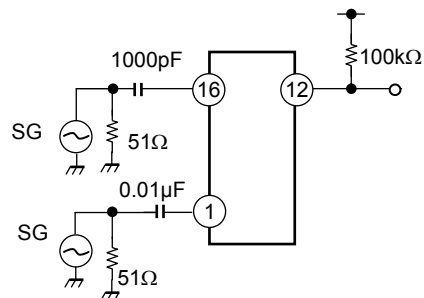
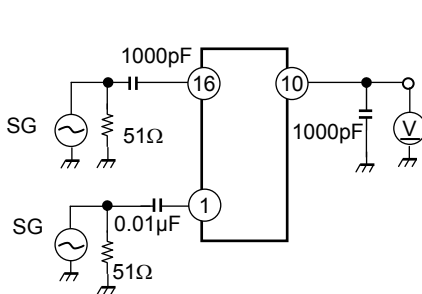
(The components illustrated in the test circuit diagrams that follow are only used to confirm device characteristics. Toshiba does not guarantee that these components will prevent malfunction or failure in your particular application device.)



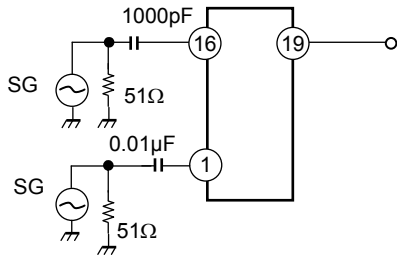
Test Circuit 1

(1) V_{RSSI} , I_{FL} , I_{FH}

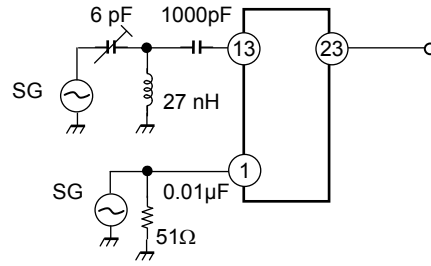
(2) DR



(3) Vod

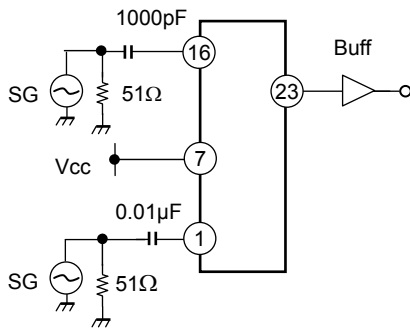


(4) 12dB SINAD

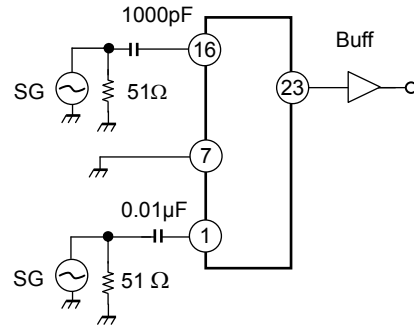


(5) S/N1, S/N2, AMR

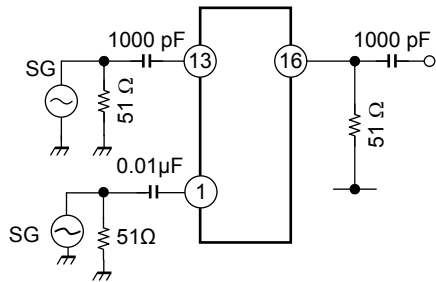
FSK Mode



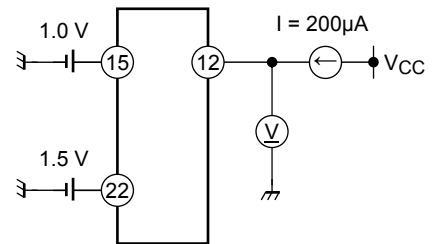
ASK Mode



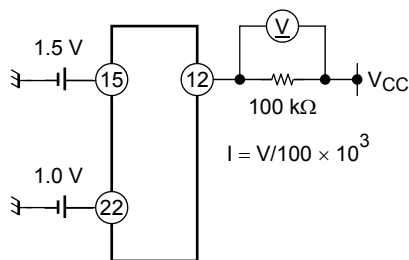
(6) $G_{V(RF)1}$



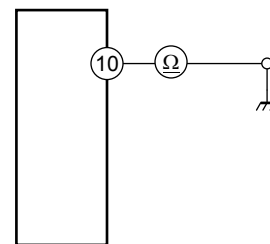
(7) V_{DATA1}



(8) I_{DATAH}

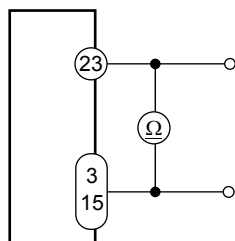


(9) R_{RSSI}



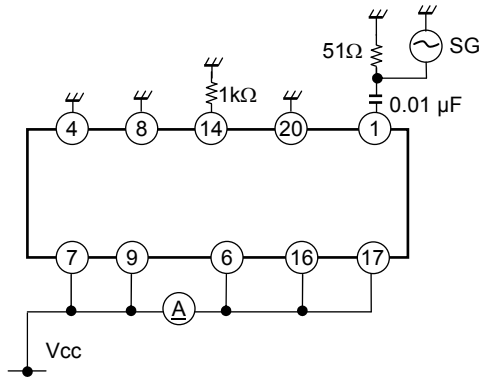
* Set voltage to 0.2 V or less, then measure.

(10) R_{PEAK} , R_{COMP}

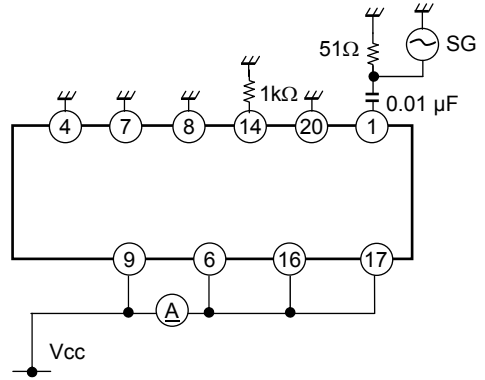


Test Circuit 2

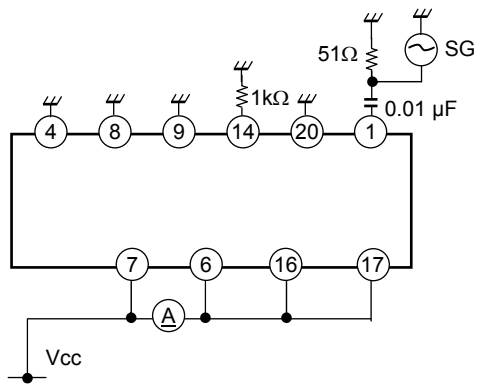
(1) I_{ccq} FM



(2) I_{ccq} AM

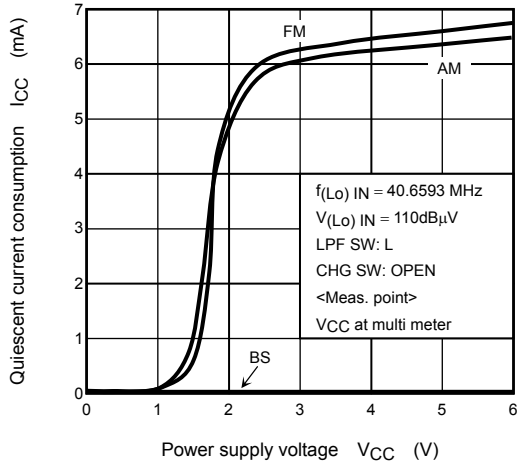


(3) I_{cco}

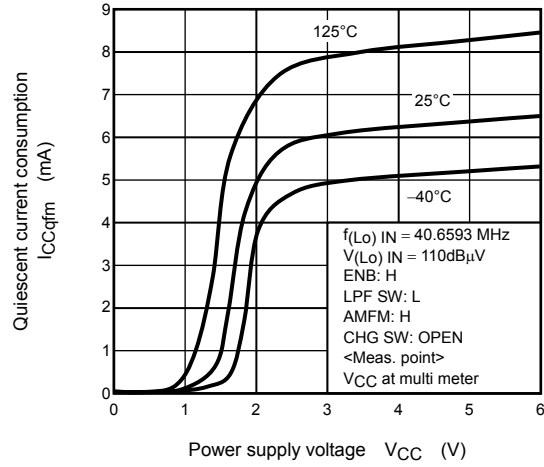


Reference data (This is temperature characteristics data when it used evaluation boards. This is not guarantee on condition that it is stating except electrical characteristics.)

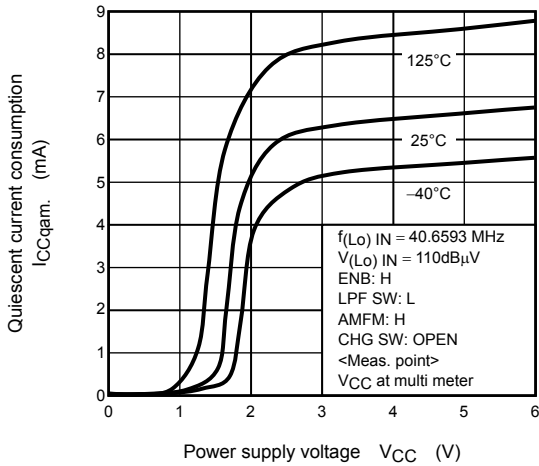
Quiescent Current Consumption vs. Power Supply Voltage Characteristics



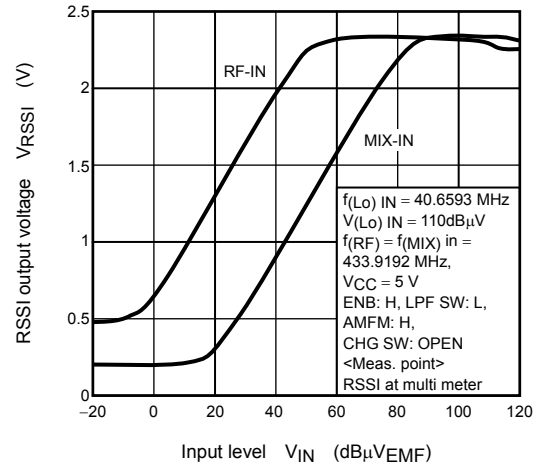
Quiescent Current Consumption vs. Power Supply Voltage Characteristics FM Mode



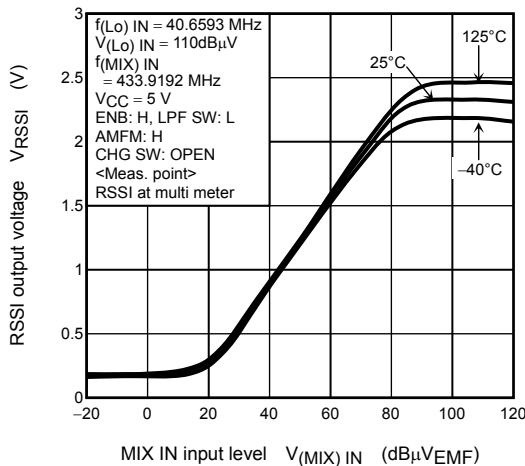
Quiescent Current Consumption vs. Power Supply Voltage Characteristics AM Mode



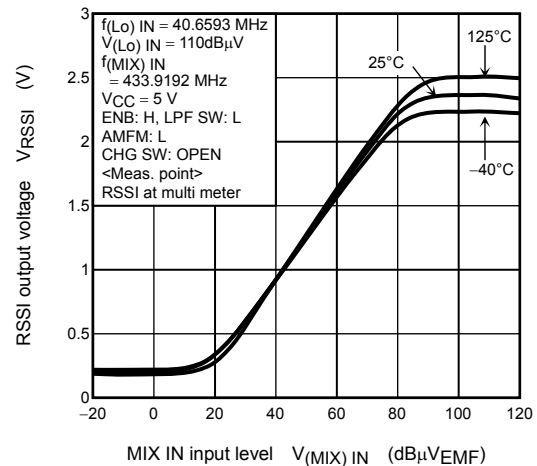
RSSI Output Voltage Characteristics (MIX, RF input)



RSSI Output Voltage Characteristics (MIX input) FM Mode

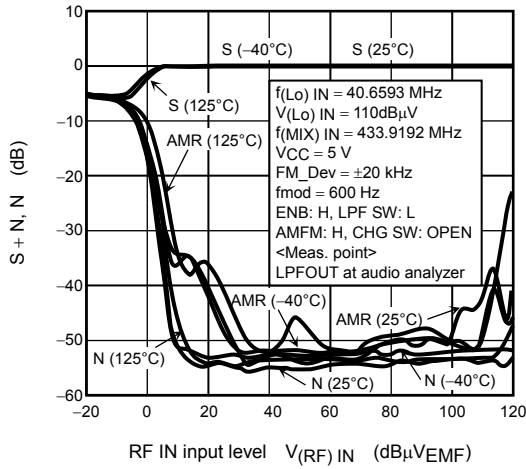


RSSI Output Voltage Characteristics (MIX input) AM Mode

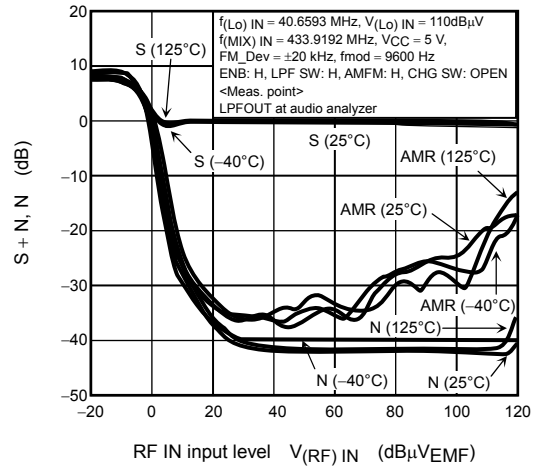


Reference data (This is temperature characteristics data when it used evaluation boards. This is not guarantee on condition that it is stating except electrical characteristics.)

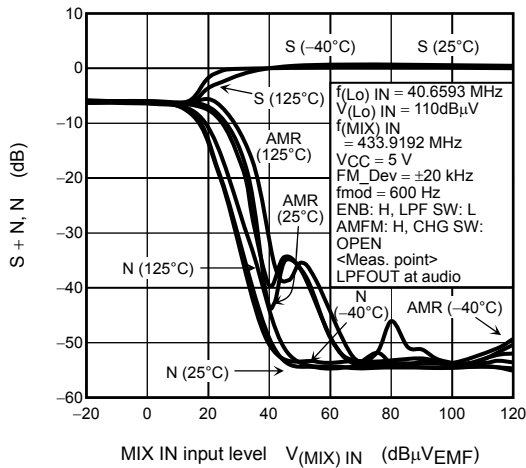
S/N, AMR Characteristics (RF input), FM Mode Filer for Low-Bit



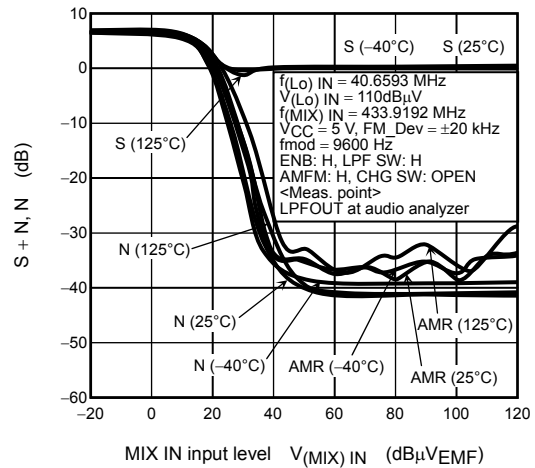
S/N, AMR Characteristics (RF input), FM Mode Filer for High-Bit



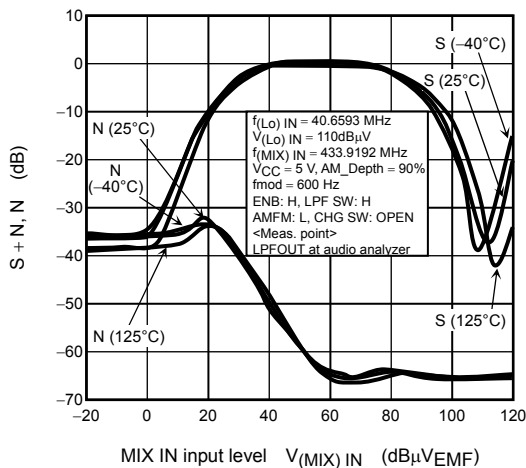
S/N, AMR Characteristics (MIX input), FM Mode Filer for Low-Bit



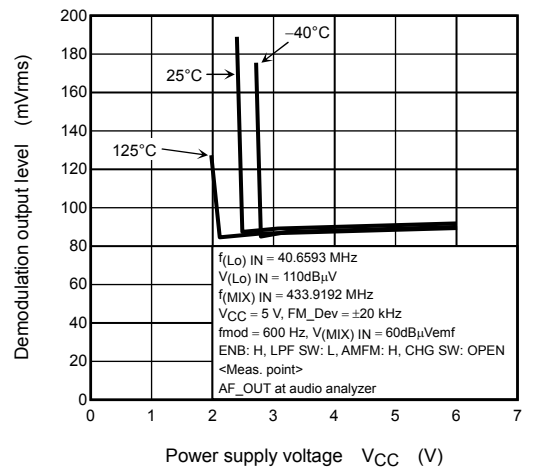
S/N, AMR Characteristics (MIX input), FM Mode Filer for High-Bit



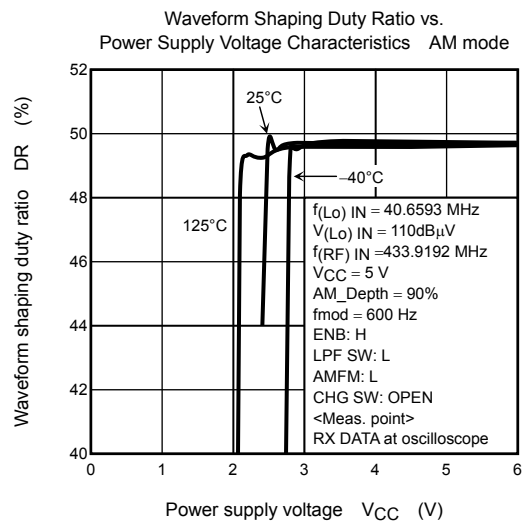
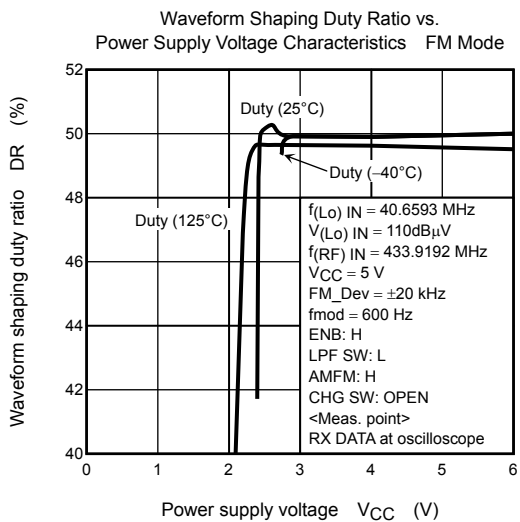
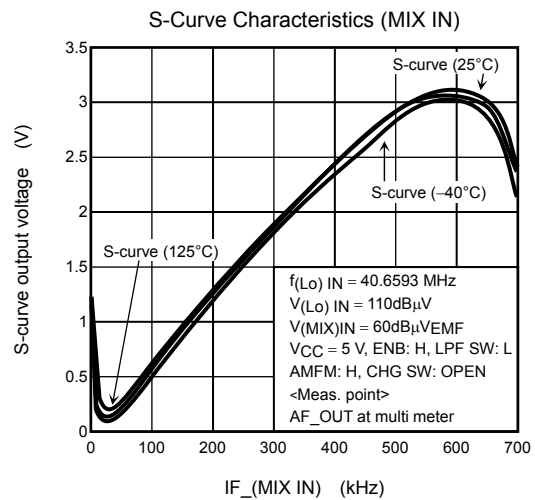
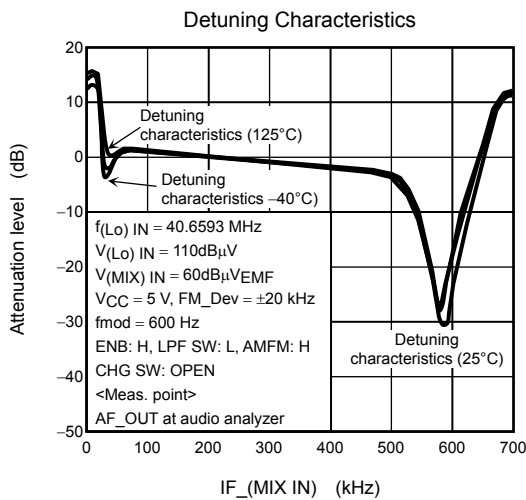
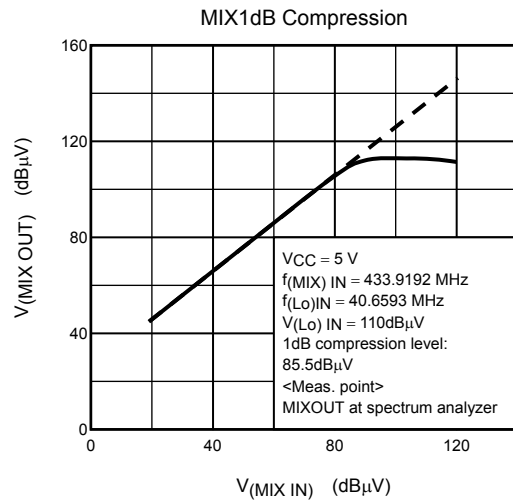
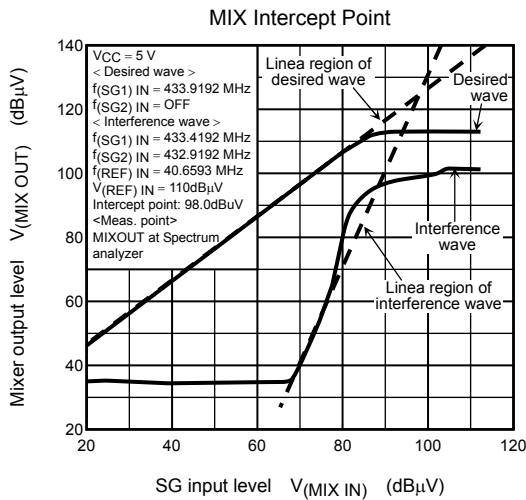
S/N, AMR Characteristics (MIX input), AM Mode Filer for Low-Bit



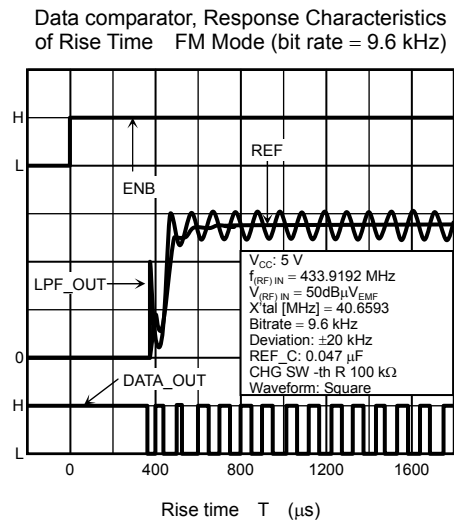
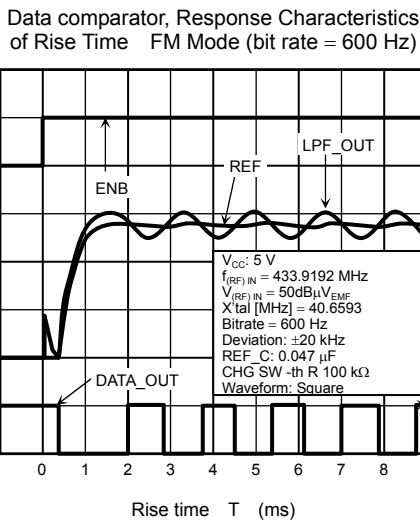
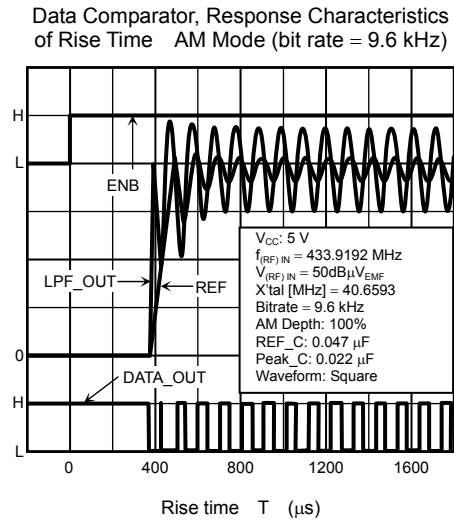
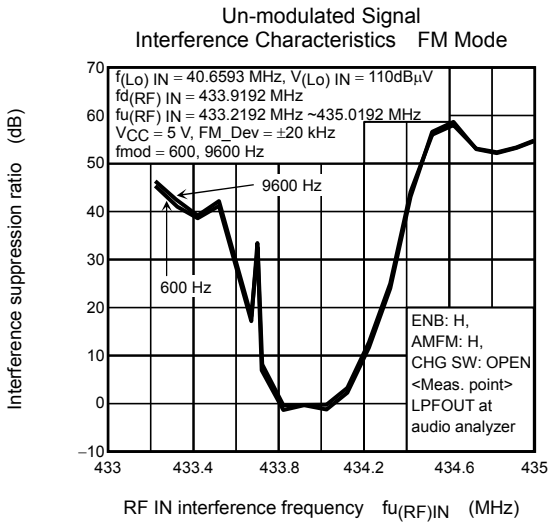
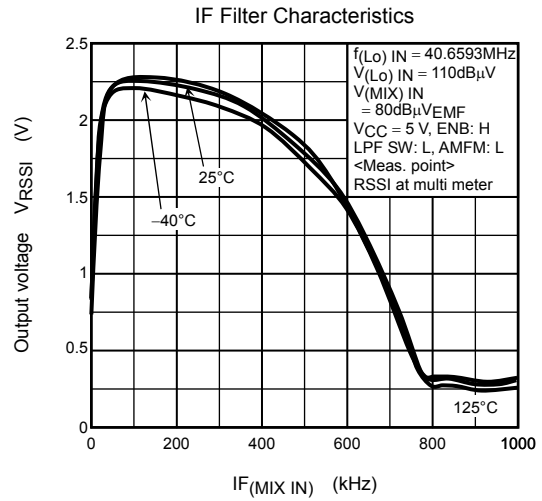
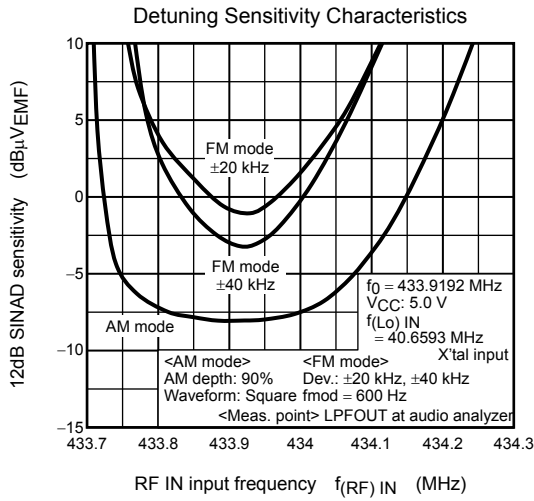
Demodulation Output Level vs. Power Supply Voltage (FM)



Reference data (This is temperature characteristics data when it used evaluation boards. This is not guarantee on condition that it is stating except electrical characteristics.)

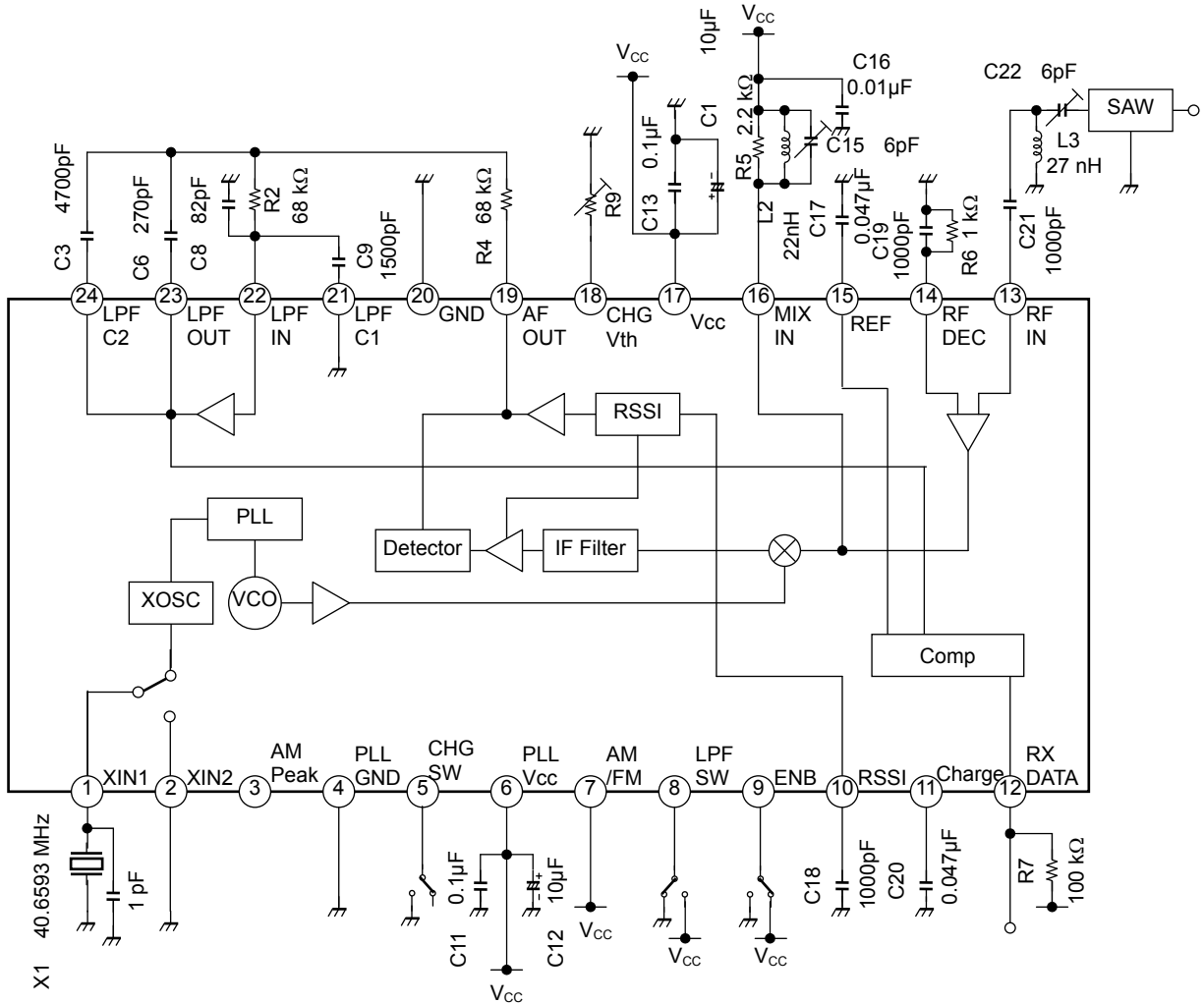


Reference data (This is temperature characteristics data when it used evaluation boards. This is not guarantee on condition that it is stating except electrical characteristics.)



Application Circuit (Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application.)

(1) FSK mode, Bit rate selection: use, XIN1/ XIN2 selection: unnecessary, CHARGE1/2 selection: use



SAW filter: Murata Manufacturing (SAFCH434MAM0T00)
 X1: RIVER ELETEC (FCX-03)/ KDS (DSX530GK)

*: R9 value is reference. Please evaluate carefully when developing the production design for your application

Data Rate

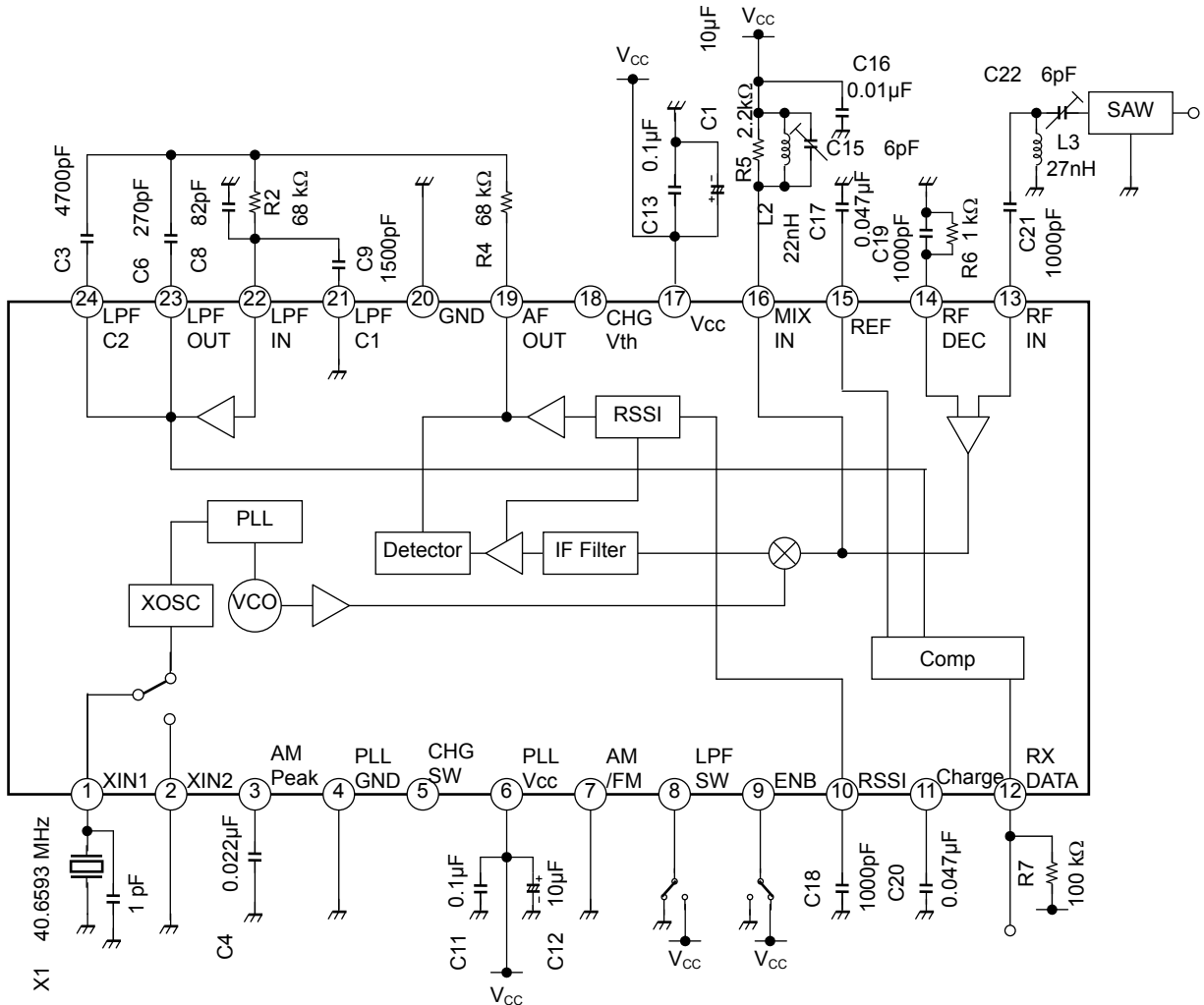
LPF SW	Lo	Hi
Data Rate (Manchester encoded)	600 bps	9600 bps

Example of controlling pins

	LPF SW	CHG SW
Hi bit rate, CHARGE2 use	H	OPEN
Low bit rate, CHARGE1 use	L	OPEN
Low bit rate, CHARGE2 use	L	L

Application Circuit (Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application.)

(2) ASK mode, Bit rate selection: use, XIN1/ XIN2 selection: unnecessary, CHARGE1/2 selection: use



SAW filter: Murata Manufacturing (SAFCH434MAM0T00)
 X1: RIVER ELETEC (FCX-03)/ KDS (DSX530GK)

Data Rate

LPF SW	Lo	Hi
Data Rate (Manchester encoded)	600 bps	9600 bps
C4	CHARGE2 not use	0.022 μF

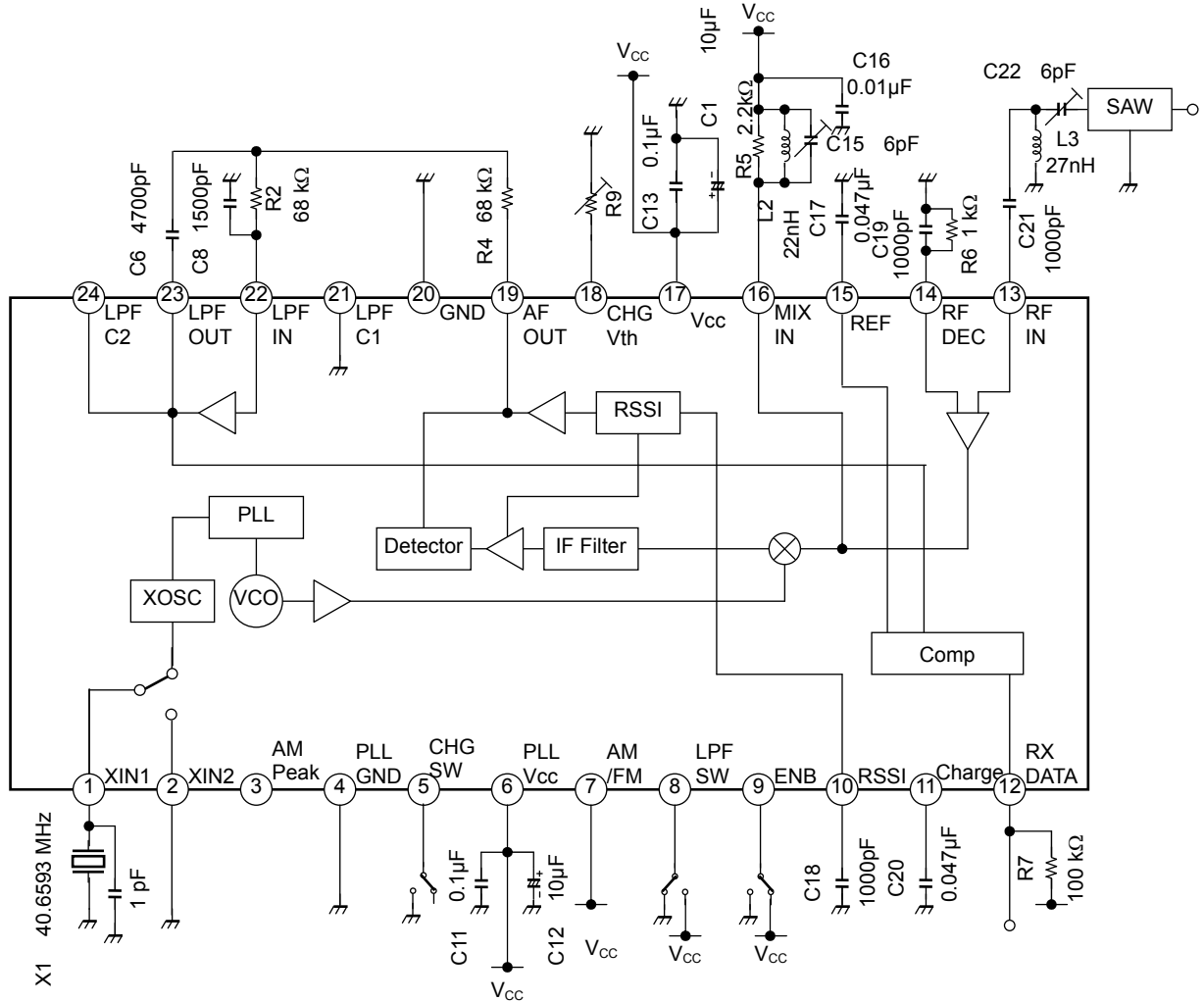
*: C4 value is reference. Please evaluate carefully when developing the production design for your application

Example of controlling pins

	LPF SW	CHG SW
Hi bit rate, CHARGE2 use	H	OPEN
Low bit rate, CHARGE1 use	L	OPEN

Application Circuit (Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application.)

(3) FSK mode, Bit rate selection: unnecessary, XIN1/ XIN2 selection: unnecessary, CHARGE1/2 selection: use



SAW filter: Murata Manufacturing (SAFCH434MAM0T00)
 X1: RIVER ELETEC (FCX-03)/ KDS (DSX530GK)

*: R9 value is reference. Please evaluate carefully when developing the production design for your application

Data Rate

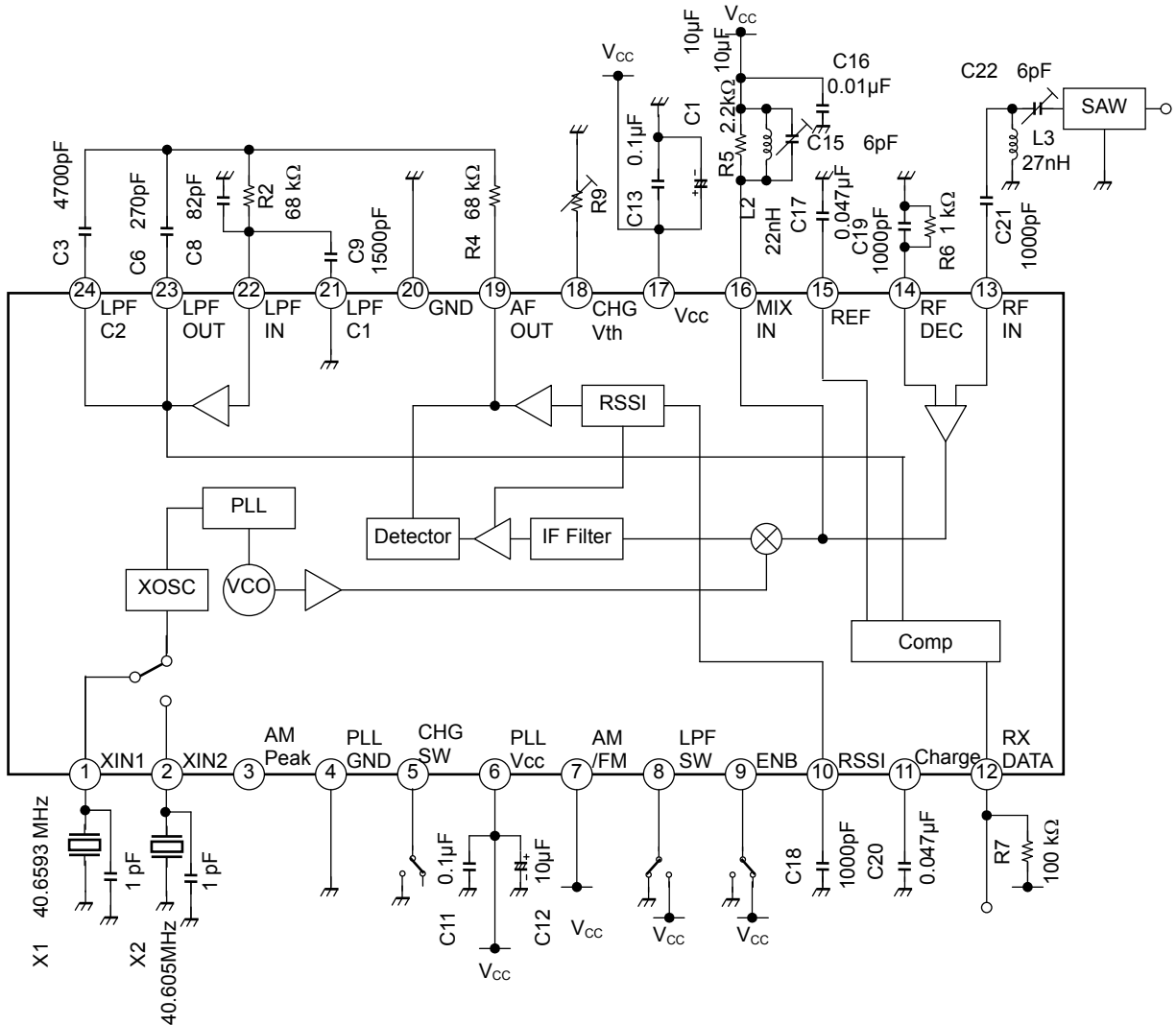
LPF SW	Lo	Hi
Data Rate (Manchester encoded)	600 bps	

Example of controlling pins

	LPF SW	CHG SW
CHARGE2 use	H	OPEN
	L	L
CHARGE1 use	L	OPEN

Application Circuit (Toshiba does not guarantee this application circuit example as a production design. Please evaluate carefully when developing the production design for your application.)

(4) FSK mode, Bit rate selection: use, XIN1/ XIN2 selection: use, CHARGE1/2 selection: use



SAW filter: Murata Manufacturing (SAFCH434MAM0T00)
 X1/ X2: RIVER ELETEC (FCX-03)/ KDS (DSX530GK)

*: R9 value is reference. Please evaluate carefully when developing the production design for your application

Data Rate

LPF SW	Lo	Hi
Data Rate (Manchester encoded)	600 bps	9600 bps

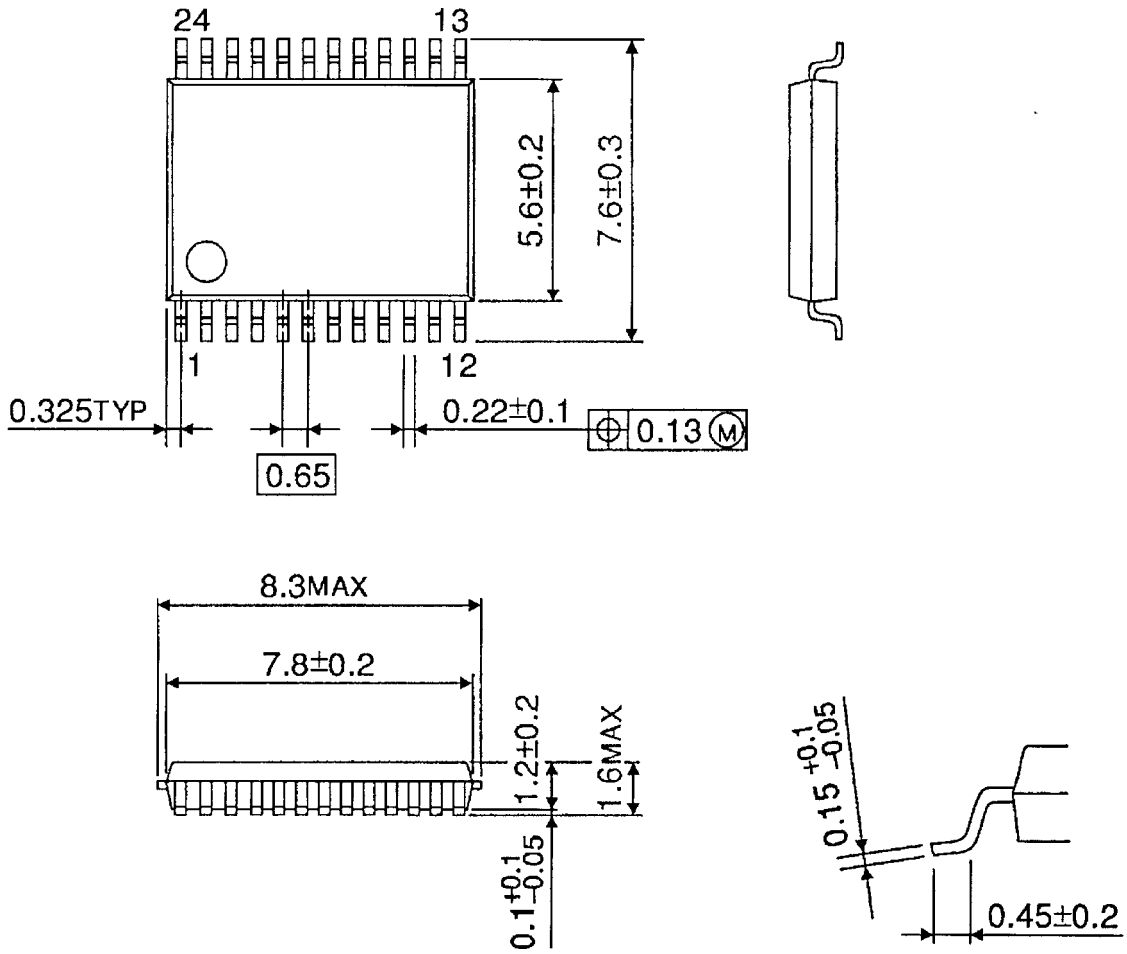
Example of controlling pins

	LPF SW	CHG SW	Xtal
Hi bit rate, CHARGE2 use	H	OPEN	XIN2
Low bit rate, CHARGE1 use	L	OPEN	XIN1
Low bit rate, CHARGE2 use	L	L	XIN1

Package Dimensions

SSOP24-P-300-0.65A

Unit : mm



Weight: 0.14 g (typ.)

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