

# TPN14006NH

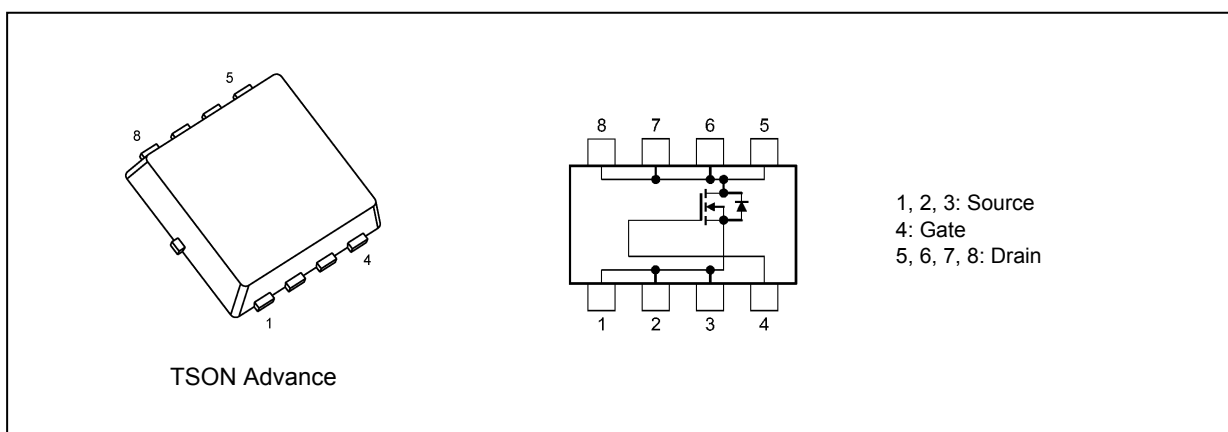
## 1. Applications

- Switching Voltage Regulators
- Motor Drivers
- DC-DC Converters

## 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 5.5 \text{ nC}$  (typ.)
- (3) Low drain-source on-resistance:  $R_{DS(ON)} = 11 \text{ m}\Omega$  (typ.)
- (4) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A}$  (max) ( $V_{DS} = 60 \text{ V}$ )
- (5) Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 0.2 \text{ mA}$ )

## 3. Packaging and Internal Circuit



## 4. Absolute Maximum Ratings (Note) ( $T_a = 25 \text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	60	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	V
Drain current (DC) (Silicon limit) (Note 1), (Note 2)	$I_D$	33	A
Drain current (DC) (Note 1)	$I_D$	13	
Drain current (pulsed) ( $t = 1 \text{ ms}$ ) (Note 1)	$I_{DP}$	65	A
Power dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_D$	30	W
Power dissipation ( $t = 10 \text{ s}$ ) (Note 3)	$P_D$	1.9	W
Power dissipation ( $t = 10 \text{ s}$ ) (Note 4)	$P_D$	0.7	W
Single-pulse avalanche energy (Note 5)	$E_{AS}$	43	mJ
Avalanche current	$I_{AR}$	13	A
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance (T <sub>c</sub> = 25 °C)	R <sub>th(ch-c)</sub>	4.16	°C/W
Channel-to-ambient thermal resistance (t = 10 s) (Note 3)	R <sub>th(ch-a)</sub>	65.7	
Channel-to-ambient thermal resistance (t = 10 s) (Note 4)	R <sub>th(ch-a)</sub>	178.1	

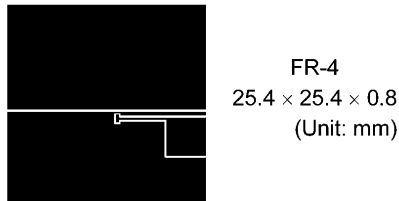
Note 1: Ensure that the channel temperature does not exceed 150 °C.

Note 2: Limited by silicon chip capability.

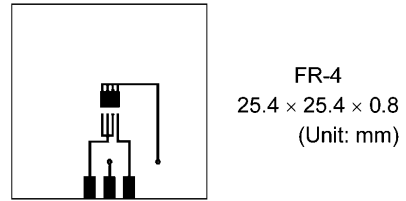
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5: V<sub>DD</sub> = 48 V, T<sub>ch</sub> = 25 °C (initial), L = 0.2 mH, R<sub>G</sub> = 1 Ω, I<sub>AR</sub> = 13 A



**Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)**



**Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)**

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics**

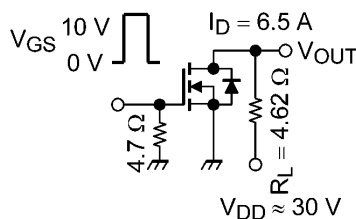
**6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	60	—	—	V
Drain-source breakdown voltage (Note 6)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	45	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ mA}$	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 6.5\text{ V}, I_D = 6.5\text{ A}$	—	18	41	$\text{m}\Omega$
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 6.5\text{ A}$	—	11	14	$\text{m}\Omega$

Note 6: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

**6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1000	1300	$\mu\text{F}$
Reverse transfer capacitance	$C_{rss}$		—	25	55	$\text{pF}$
Output capacitance	$C_{oss}$		—	310	—	$\text{pF}$
Gate resistance	$r_g$	—	—	2.0	3.0	$\Omega$
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	9	—	ns
Switching time (turn-on time)	$t_{on}$		—	18	—	ns
Switching time (fall time)	$t_f$		—	5.5	—	ns
Switching time (turn-off time)	$t_{off}$		—	18	—	ns



Duty  $\leq 1\%$ ,  $t_w = 10\text{ }\mu\text{s}$

**Fig. 6.2.1 Switching Time Test Circuit**

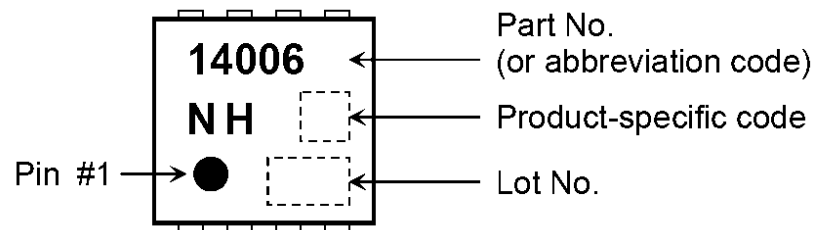
**6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 13\text{ A}$	—	15	—	nC
Gate-source charge 1	$Q_{gs1}$		—	4.9	—	
Gate-drain charge	$Q_{gd}$		—	3.2	—	
Gate switch charge	$Q_{sw}$		—	5.5	—	

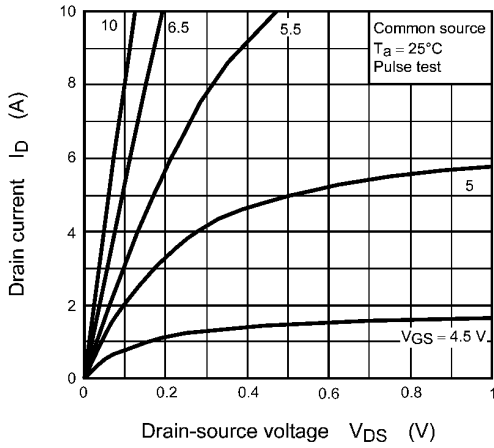
**6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 7)	$I_{DRP}$	—	—	—	65	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 13\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

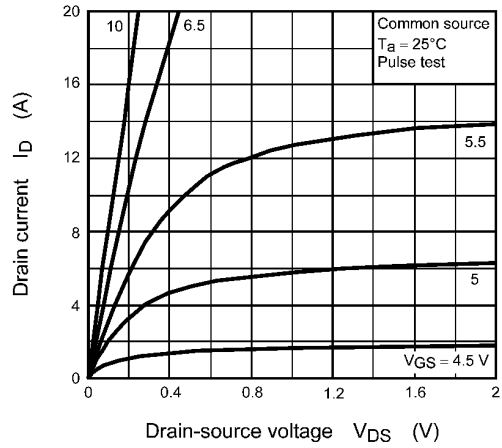
Note 7: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

**7. Marking****Fig. 7.1 Marking**

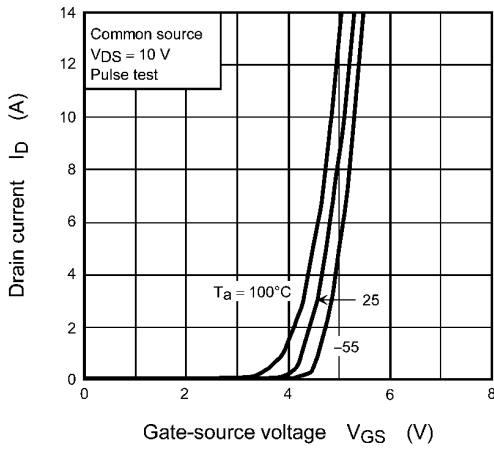
**8. Characteristics Curves (Note)**



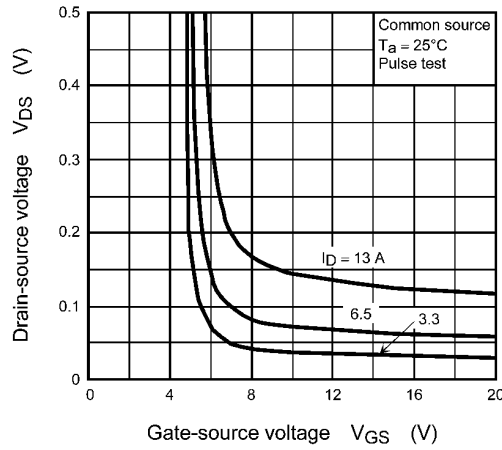
**Fig. 8.1  $I_D - V_{DS}$**



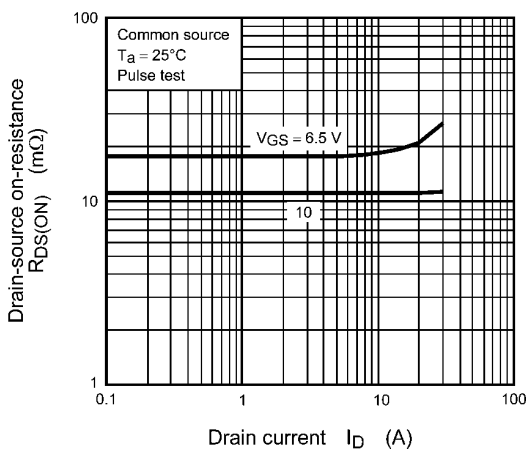
**Fig. 8.2  $I_D - V_{DS}$**



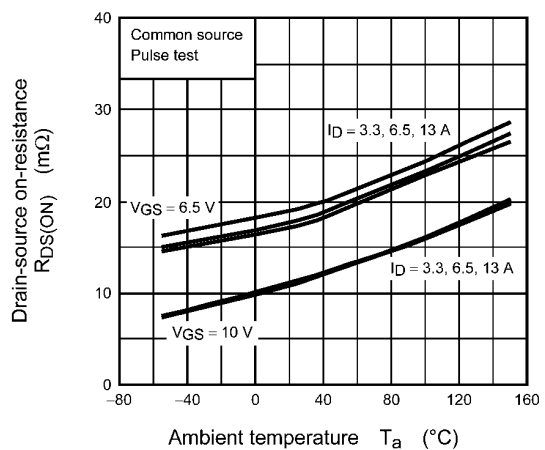
**Fig. 8.3  $I_D - V_{GS}$**



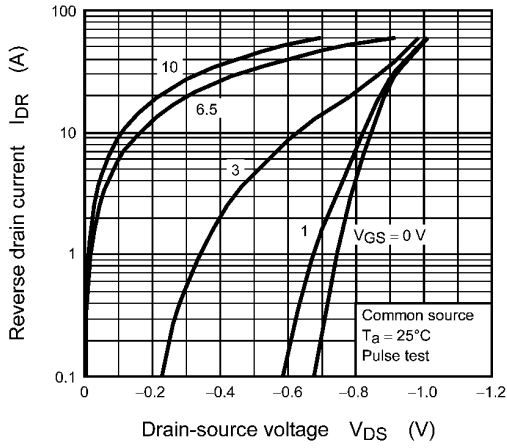
**Fig. 8.4  $V_{DS} - V_{GS}$**



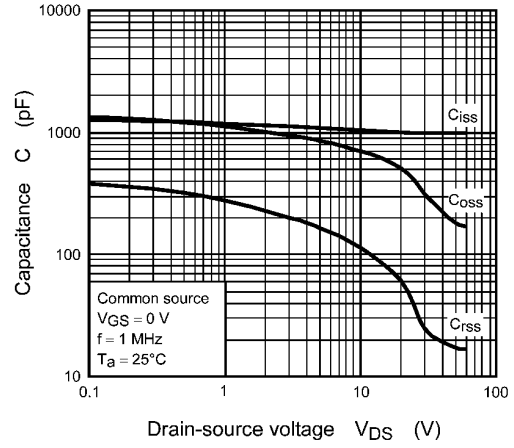
**Fig. 8.5  $R_{DS(ON)} - I_D$**



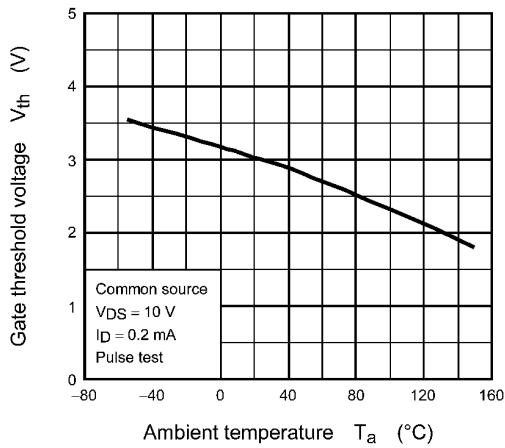
**Fig. 8.6  $R_{DS(ON)} - T_a$**



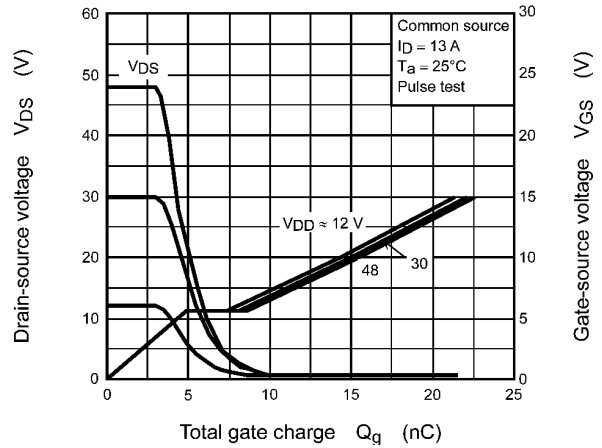
**Fig. 8.7  $I_{DR} - V_{DS}$**



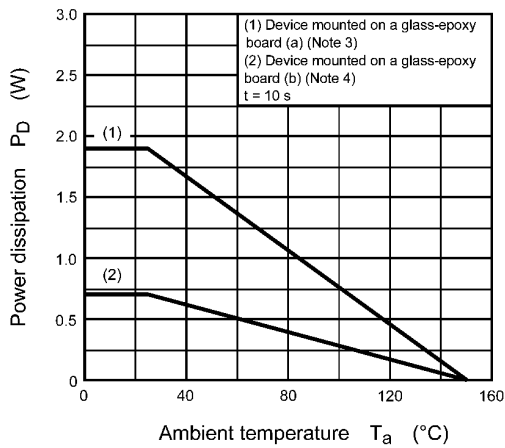
**Fig. 8.8 Capacitance -  $V_{DS}$**



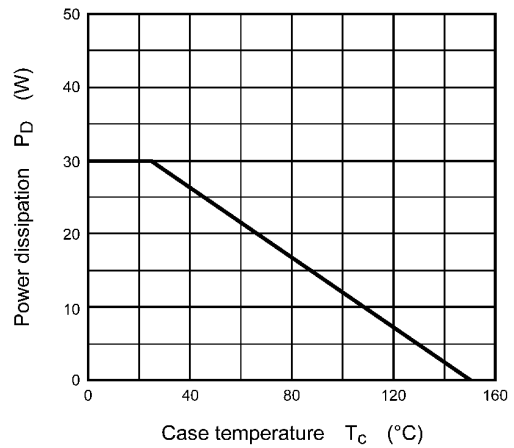
**Fig. 8.9  $V_{th} - T_a$**



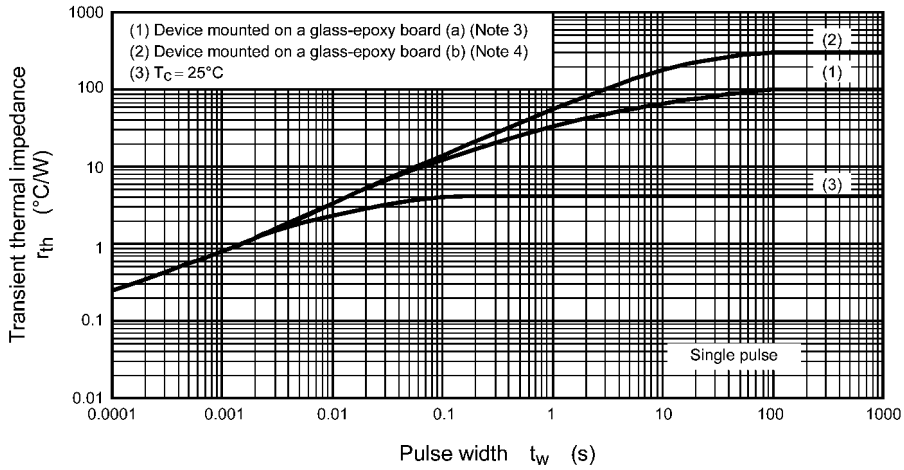
**Fig. 8.10 Dynamic Input/Output Characteristics**



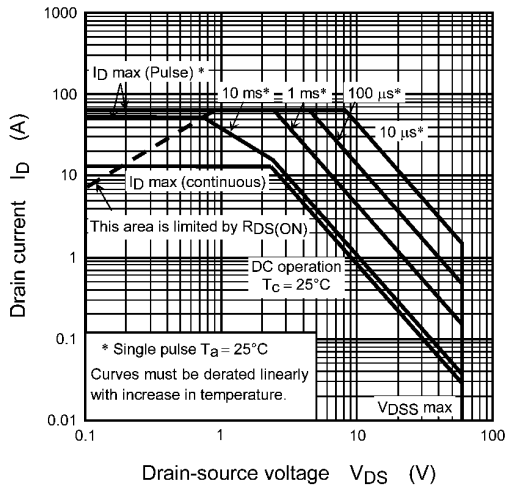
**Fig. 8.11  $P_D - T_a$   
 (Guaranteed Maximum)**



**Fig. 8.12  $P_D - T_c$   
 (Guaranteed Maximum)**



**Fig. 8.13  $r_{th} - t_w$**   
**(Guaranteed Maximum)**



**Fig. 8.14 Safe Operating Area**  
**(Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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