

TOSHIBA Field Effect Transistor Silicon P, N Channel MOS Type (U-MOV/U-MOSIV)

# TPCP8404

Portable Equipment Applications  
Motor Drive Applications

- Low drain-source ON-resistance : P Channel  $R_{DS(ON)} = 38 \text{ m}\Omega(\text{typ.})$   
( $V_{GS} = -10\text{V}$ )  
N Channel  $R_{DS(ON)} = 38 \text{ m}\Omega(\text{typ.})$   
( $V_{GS} = 10\text{V}$ )
- High forward transfer admittance : P Channel  $|Y_{fs}| = 7.3 \text{ S}(\text{typ.})$   
N Channel  $|Y_{fs}| = 8 \text{ S}(\text{typ.})$
- Low leakage current : P Channel  $I_{DSS} = -10 \mu\text{A}(\text{max})$  ( $V_{DS} = -30 \text{ V}$ )  
N Channel  $I_{DSS} = 10 \mu\text{A}(\text{max})$  ( $V_{DS} = 30 \text{ V}$ )
- Enhancement mode  
: P Channel  $V_{th} = -0.8 \text{ to } -2.0 \text{ V}$  ( $V_{DS} = -10 \text{ V}$ ,  $I_D = -1 \text{ mA}$ )  
N Channel  $V_{th} = 1.3 \text{ to } 2.5 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1 \text{ mA}$ )

## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

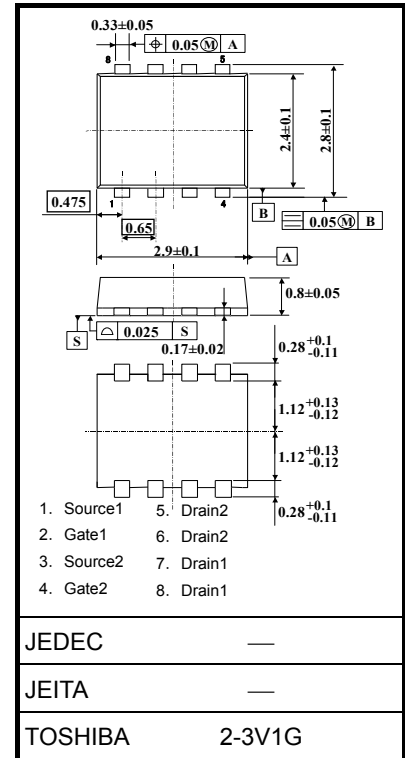
Characteristics		Symbol	Rating		Unit
Drain-source voltage		$V_{DSS}$	-30	30	V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )		$V_{DGR}$	-30	30	V
Gate-source voltage		$V_{GSS}$	$\pm 20$	$\pm 20$	V
Drain current	DC (Note 1)	$I_D$	-4	4	A
	Pulse (Note 1)	$I_{DP}$	-16	16	
Drain power dissipation ( $t = 5 \text{ s}$ ) (Note 2a)	Single-device operation (Note 3a)	$P_D(1)$	1.48	1.48	W
	Single-device value at dual operation (Note 3b)	$P_D(2)$	1.23	1.23	
Drain power dissipation ( $t = 5 \text{ s}$ ) (Note 2b)	Single-device operation (Note 3a)	$P_D(1)$	0.58	0.58	
	Single-device value at dual operation (Note 3b)	$P_D(2)$	0.36	0.36	
Single pulse avalanche energy (Note 4)		$E_{AS}$	2.6	2.6	mJ
Avalanche current		$I_{AR}$	-2	2	A
Repetitive avalanche energy Single-device value at dual operation (Note 2a, 3b, 5)		$E_{AR}$	0.009		mJ
Channel temperature		$T_{ch}$	150		$^\circ\text{C}$
Storage temperature range		$T_{stg}$	-55 to 150		$^\circ\text{C}$

Note: For Notes 1 to 5, refer to the next page.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

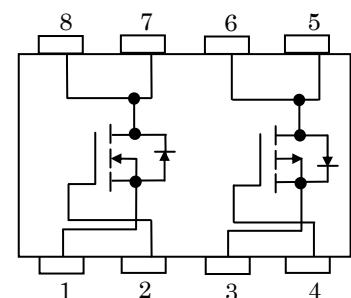
This transistor is an electrostatic-sensitive device. Handle with caution.

Unit: mm

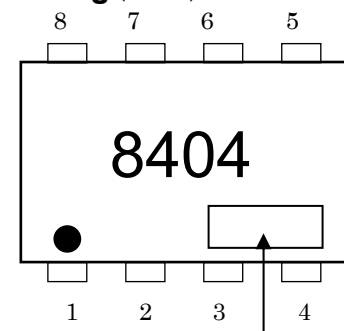


Weight: 0.017 g (typ.)

## Circuit Configuration



## Marking (Note 6)



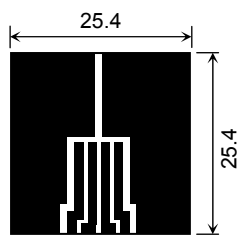
Lot No.

## Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 5 s) (Note 2a)	Single-device operation (Note 3a)	R <sub>th</sub> (ch-a) (1)	84.5	°C/W
	Single-device value at dual operation (Note 3b)	R <sub>th</sub> (ch-a) (2)	101.6	
Thermal resistance, channel to ambient (t = 5 s) (Note 2b)	Single-device operation (Note 3a)	R <sub>th</sub> (ch-a) (1)	215.5	°C/W
	Single-device value at dual operation (Note 3b)	R <sub>th</sub> (ch-a) (2)	347.2	

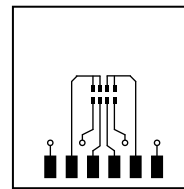
Note 1: The channel temperature should not exceed 150°C during use.

Note 2: (a) Device mounted on a glass-epoxy board (a)      (b) Device mounted on a glass-epoxy board (b)



(a)

FR-4  
25.4 × 25.4 × 0.8  
(Unit: mm)



(b)

FR-4  
25.4 × 25.4 × 0.8  
(Unit: mm)

- Note 3: a) The power dissipation and thermal resistance values shown are for a single device. (During single-device operation, power is only applied to one device.)  
 b) The power dissipation and thermal resistance values shown are for a single device. (During dual operation, power is evenly applied to both devices.)

Note 4: P Channel: V<sub>DD</sub> = -24 V, T<sub>ch</sub> = 25°C (initial), L = 0.5 mH, R<sub>G</sub> = 25 Ω, I<sub>AR</sub> = -2 A  
 N Channel: V<sub>DD</sub> = 24 V, T<sub>ch</sub> = 25°C (initial), L = 0.5 mH, R<sub>G</sub> = 25 Ω, I<sub>AR</sub> = 2 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: ● on the lower left of the marking indicates Pin 1.

※ Weekly code (3 digits):



Week of manufacture

(01 for the first week of the year, continuing up to 52 or 53)

Year of manufacture

(The last digit of the calendar year)

## P-ch

### Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 100$	nA
Drain cut-off current		$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-30	—	—	V
		$V_{(BR)DSX}$	$I_D = -10\text{ mA}, V_{GS} = 20\text{ V}$	-10	—	—	
Gate threshold voltage		$V_{th}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-0.8	—	-2.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -2.0\text{ A}$	—	58	80	m $\Omega$
			$V_{GS} = -10\text{ V}, I_D = -2.0\text{ A}$	—	38	50	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -2.0\text{ A}$	3.7	7.3	—	S
Input capacitance		$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	510	—	pF
Reverse transfer capacitance		$C_{rss}$		—	110	—	
Output capacitance		$C_{oss}$		—	170	—	
Switching time	Rise time	$t_r$	<p><math>I_D = -2\text{ A}</math> <math>V_{DD} \approx -15\text{ V}</math> <math>R_L = 7.5\Omega</math> <math>V_{OUT}</math> <math>47\Omega</math></p>	—	11	—	ns
	Turn-on time	$t_{on}$		—	20	—	
	Fall time	$t_f$		—	37	—	
	Turn-off time	$t_{off}$		Duty $\leq 1\%$ , $t_w = 10\ \mu\text{s}$	—	99	
Total gate charge (gate-source plus gate-drain)		$Q_g$	$V_{DD} \approx -24\text{ V}, V_{GS} = -10\text{ V}, I_D = -4\text{ A}$	—	13	—	nC
Gate-source charge 1		$Q_{gs1}$		—	1.7	—	
Gate-drain ("miller") charge		$Q_{gd}$		—	4.6	—	

### Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	$I_{DRP}$	—	—	—	-16	A
Forward voltage (diode)		$V_{DSF}$	$I_{DR} = -4\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.2	V

## N-ch

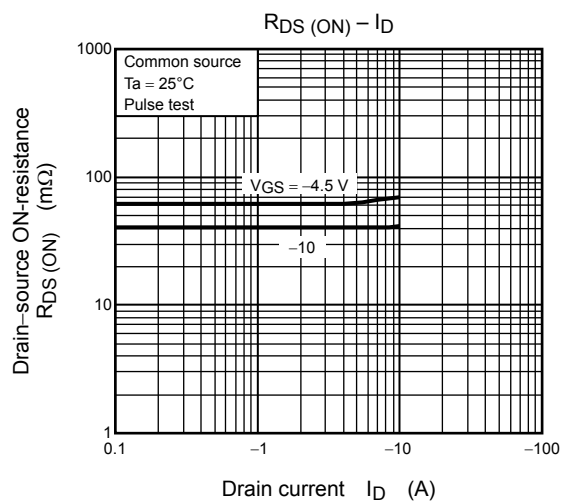
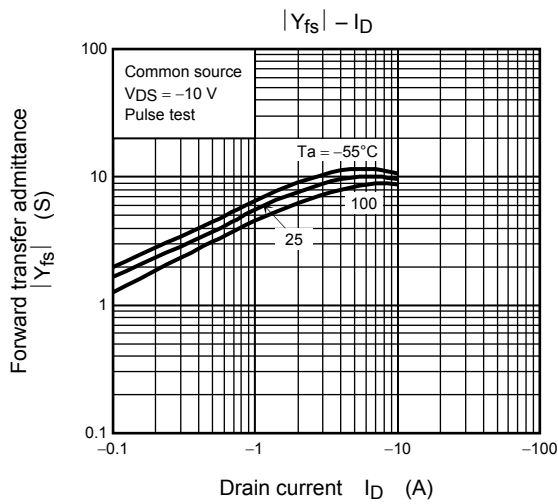
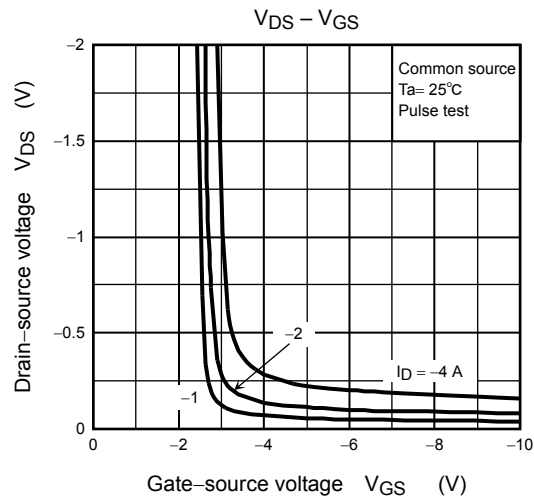
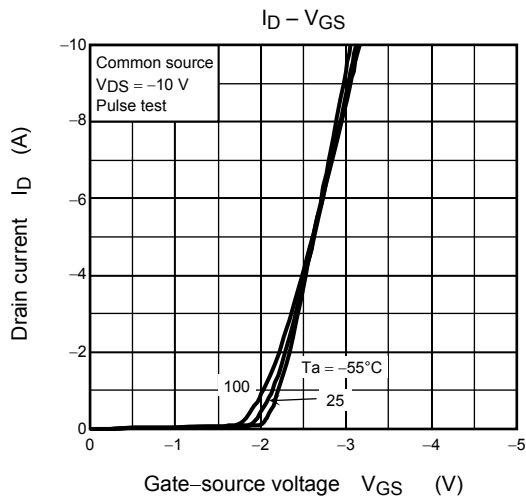
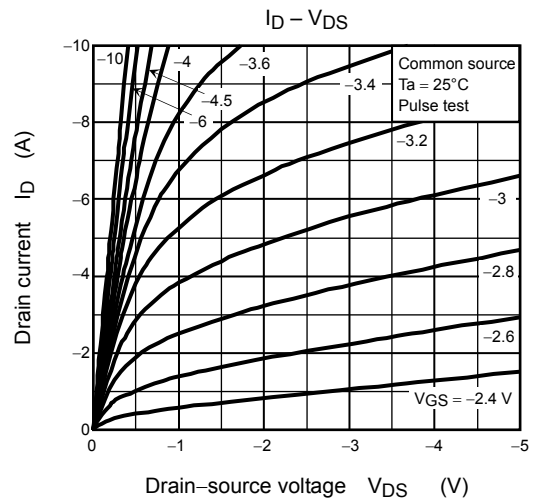
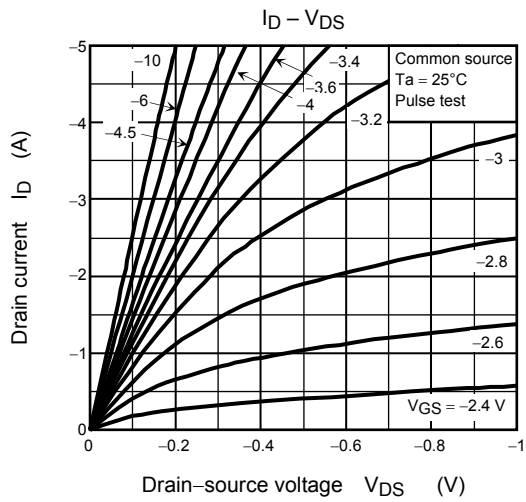
### Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 100$	nA
Drain cut-off current		$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	$\mu\text{A}$
Drain-source breakdown voltage		$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
		$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	10	—	—	
Gate threshold voltage		$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	1.3	—	2.5	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 2\text{ A}$	—	58	80	m $\Omega$
			$V_{GS} = 10\text{ V}, I_D = 2\text{ A}$	—	38	50	
Forward transfer admittance		$ Y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 2\text{ A}$	4	8	—	S
Input capacitance		$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	190	—	pF
Reverse transfer capacitance		$C_{rss}$		—	45	—	
Output capacitance		$C_{oss}$		—	60	—	
Switching time	Rise time	$t_r$		—	4.5	—	ns
	Turn-on time	$t_{on}$		—	9.0	—	
	Fall time	$t_f$		—	3.0	—	
	Turn-off time	$t_{off}$		Duty $\leq 1\%$ , $t_w = 10\ \mu\text{s}$	—	12	
Total gate charge (gate-source plus gate-drain)		$Q_g$	$V_{DD} \approx 24\text{ V}, V_{GS} = 10\text{ V}, I_D = 4\text{ A}$	—	4.6	—	nC
Gate-source charge 1		$Q_{gs1}$		—	0.7	—	
Gate-drain ("miller") charge		$Q_{gd}$		—	1.4	—	

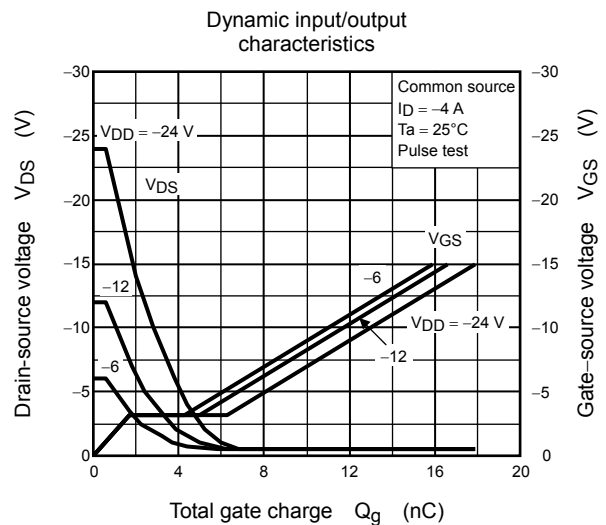
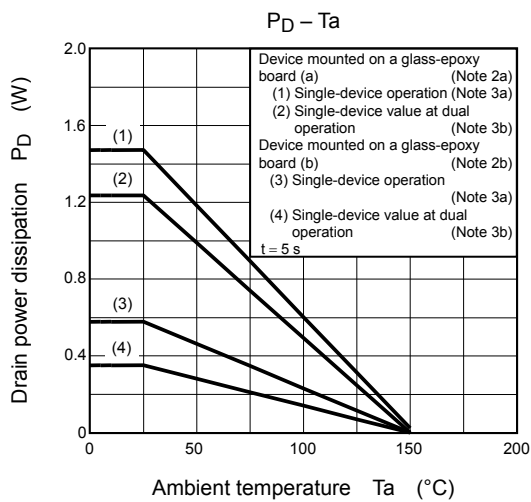
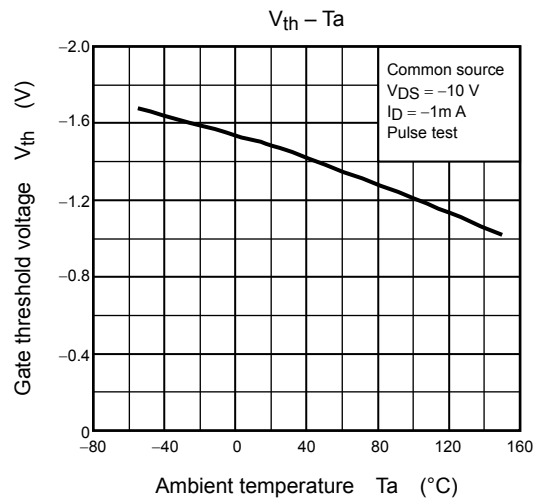
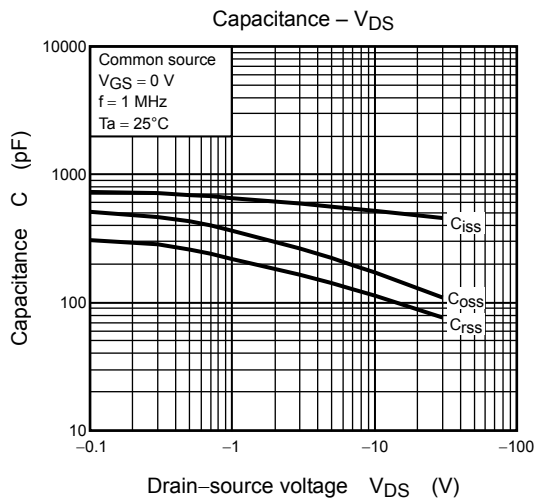
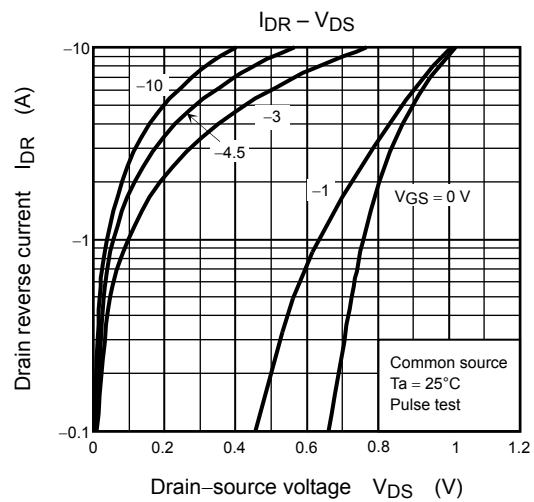
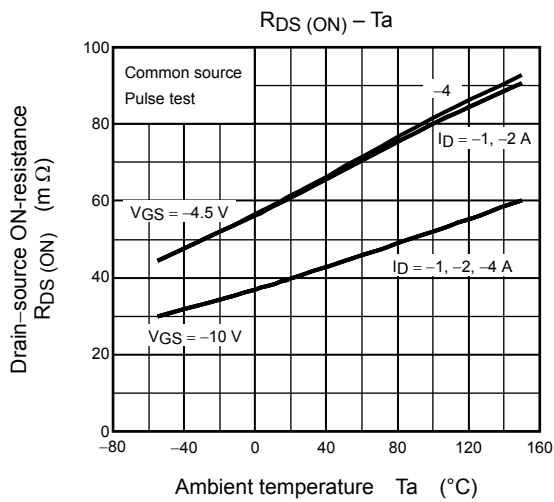
### Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	$I_{DRP}$	—	—	—	16	A
Forward voltage (diode)		$V_{DSF}$	$I_{DR} = 4\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V

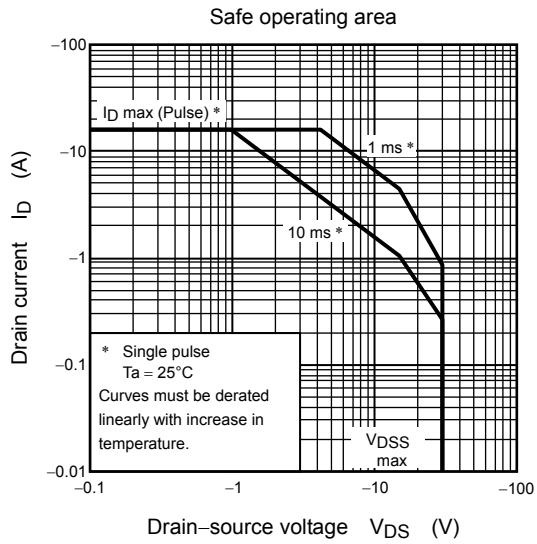
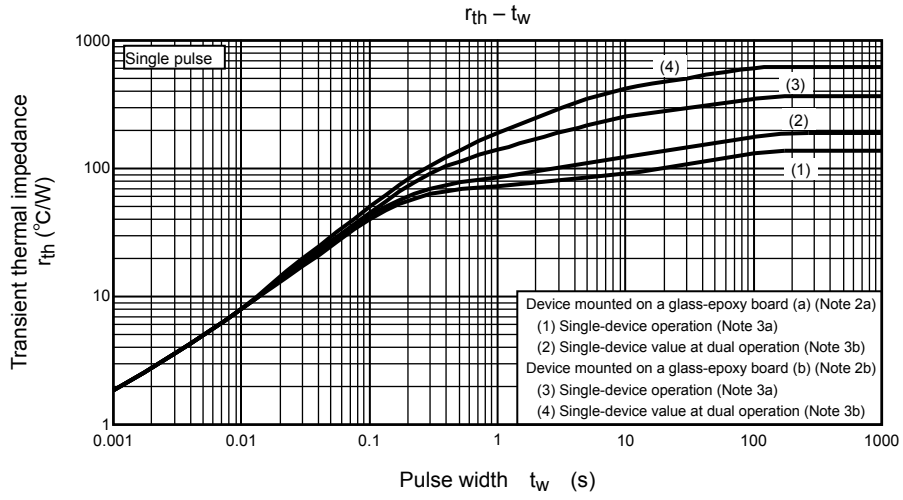
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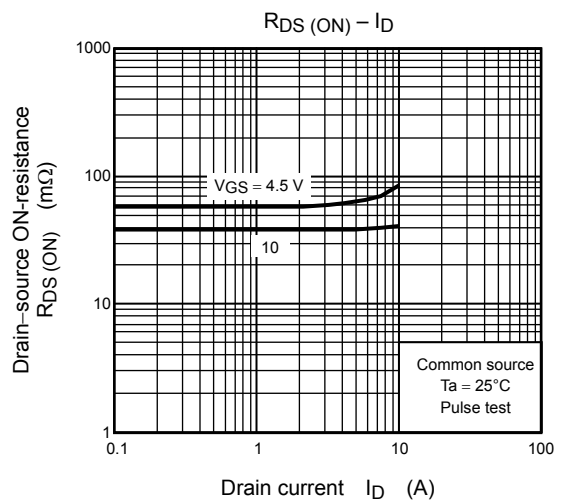
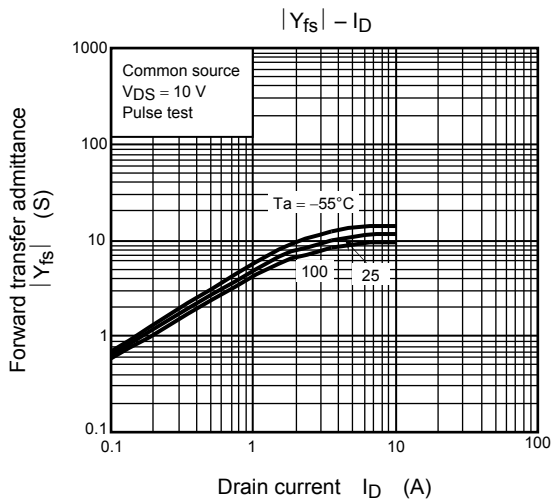
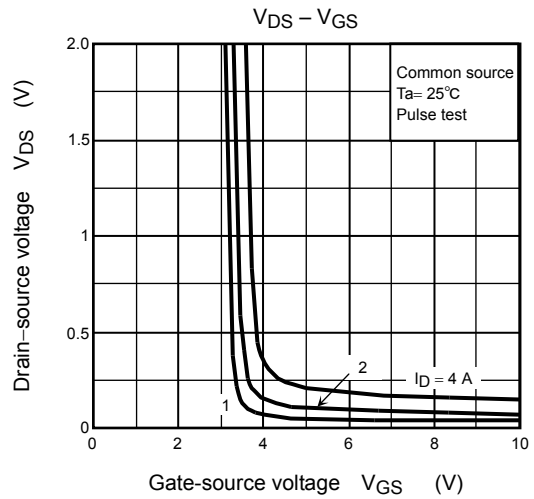
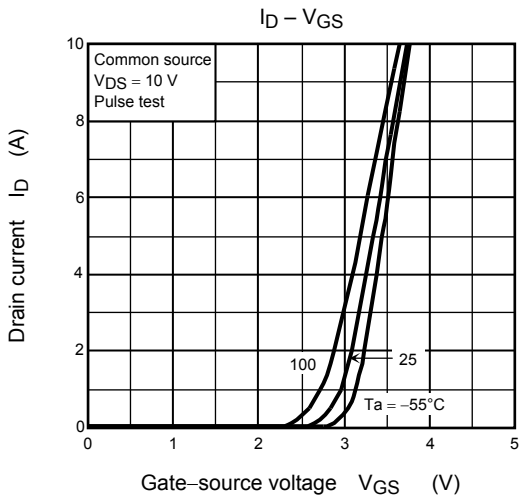
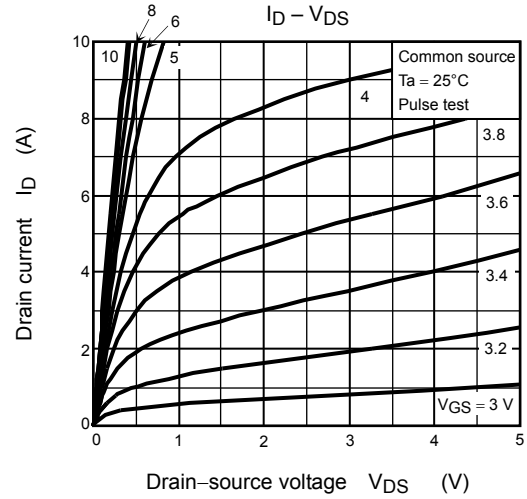
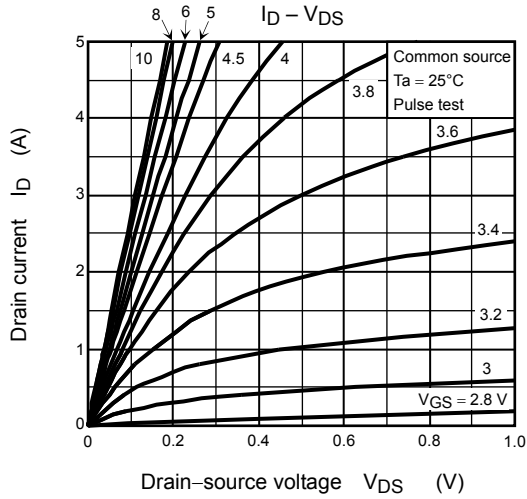
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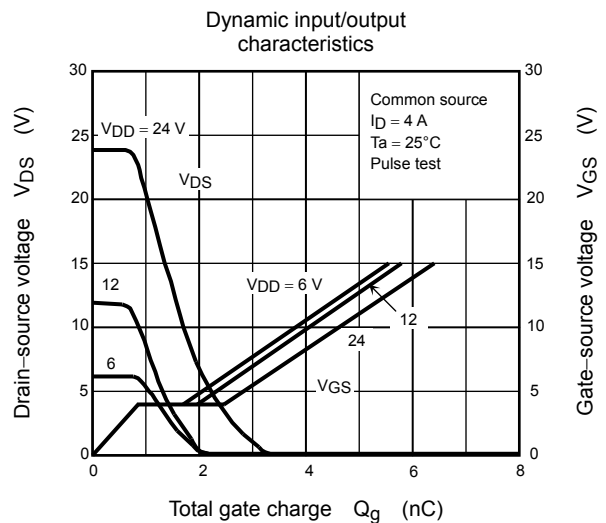
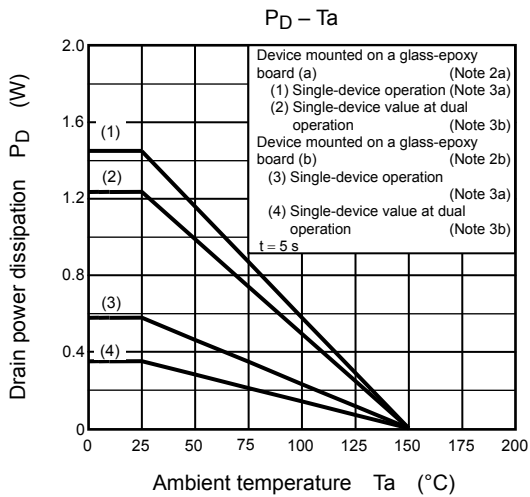
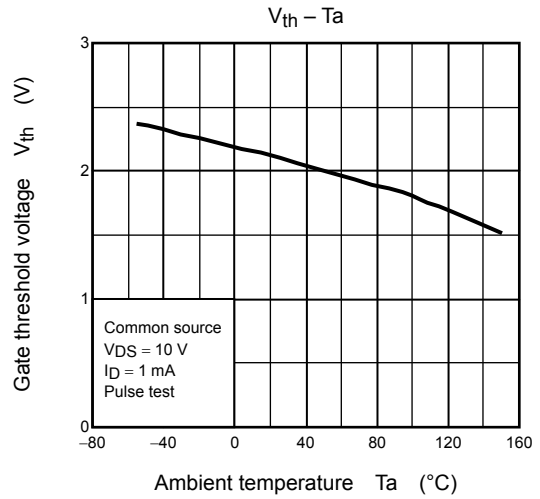
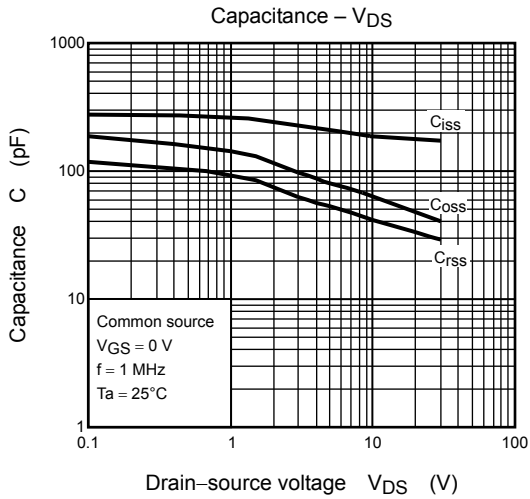
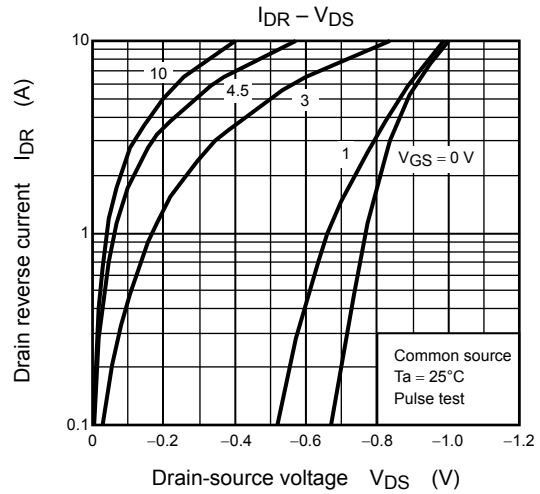
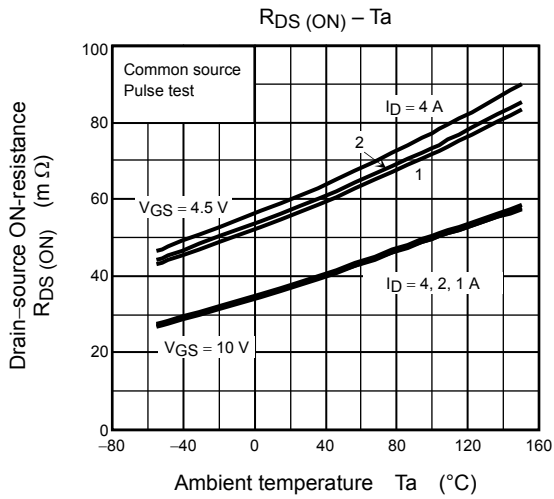
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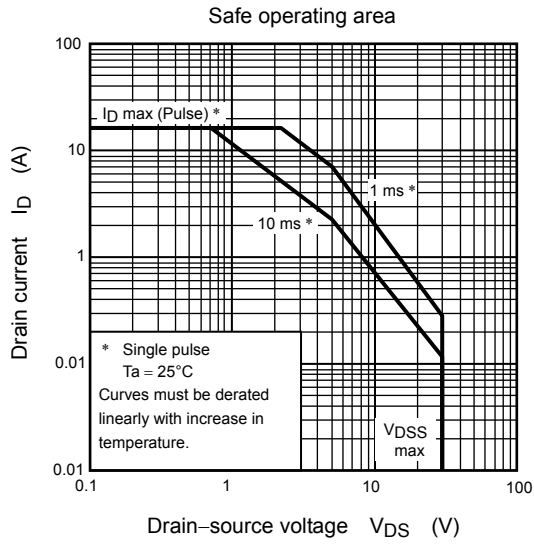
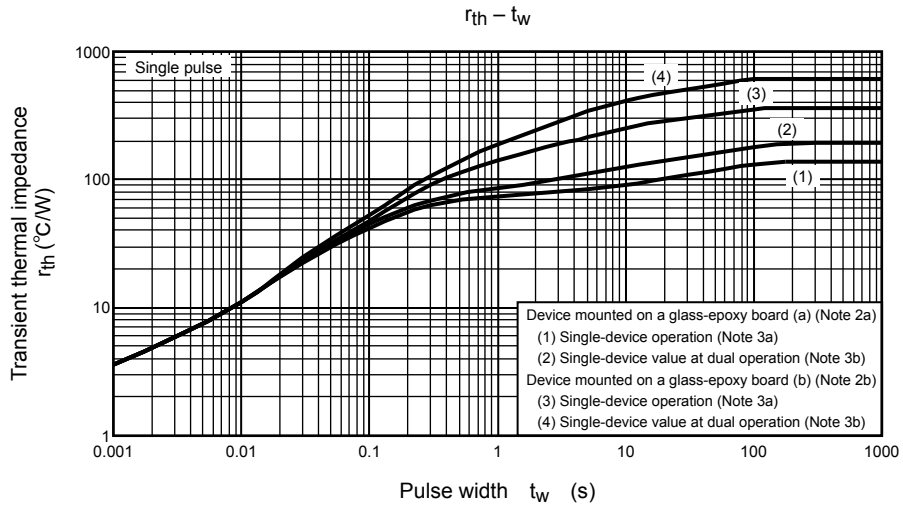
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N-ch



**N-ch**



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