

TPCA8121

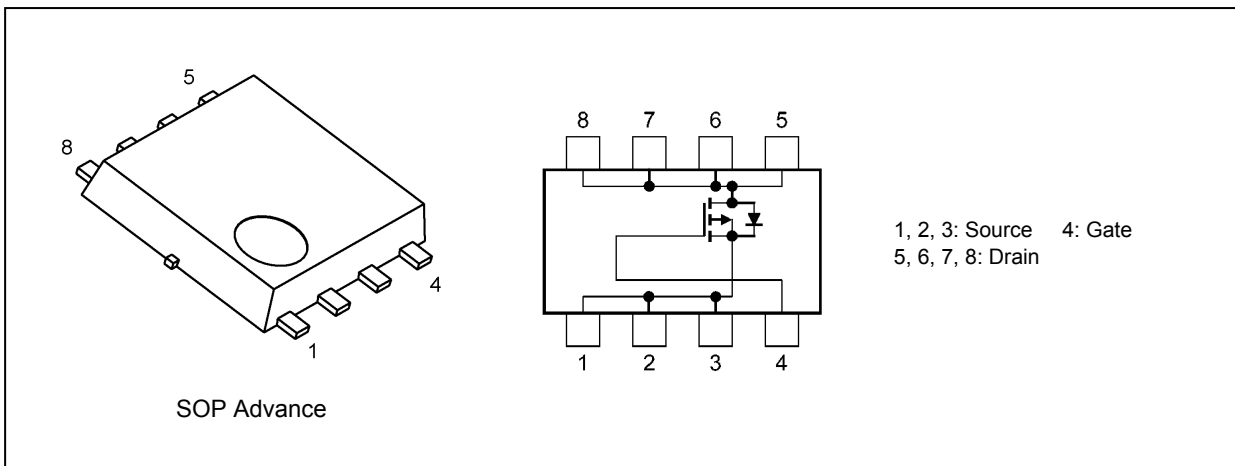
1. Applications

- Lithium-Ion Secondary Batteries
- Power Management Switches

2. Features

- (1) Small, thin package
- (2) Low drain-source on-resistance: $R_{DS(ON)} = 2.4 \text{ m}\Omega$ (typ.) ($V_{GS} = -10 \text{ V}$)
- (3) Low leakage current: $I_{DSS} = -10 \text{ }\mu\text{A}$ (max) ($V_{DS} = -30 \text{ V}$)
- (4) Enhancement mode: $V_{th} = -0.8$ to -2.0 V ($V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Rating | Unit |
|--|-----------|------------|------------------|
| Drain-source voltage | V_{DSS} | -30 | V |
| Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$) | V_{DGR} | -30 | |
| Gate-source voltage | V_{GSS} | -20/+10 | |
| Drain current (DC) (Note 1) | I_D | -45 | A |
| Drain current (pulsed) (Note 1) | I_{DP} | -135 | |
| Power dissipation ($T_c = 25^\circ\text{C}$) | P_D | 45 | W |
| Power dissipation ($t = 10 \text{ s}$) (Note 2) | P_D | 2.8 | W |
| Power dissipation ($t = 10 \text{ s}$) (Note 3) | P_D | 1.6 | W |
| Single-pulse avalanche energy (Note 4) | E_{AS} | 263 | mJ |
| Avalanche current | I_{AR} | -45 | A |
| Channel temperature (Note 5) | T_{ch} | 175 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | -55 to 150 | |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

| Characteristics | | | Symbol | Max | Unit |
|---------------------------------------|------------------------------|----------|----------------|------|--------------------|
| Channel-to-case thermal resistance | ($T_c = 25^\circ\text{C}$) | | $R_{th(ch-c)}$ | 2.78 | $^\circ\text{C/W}$ |
| Channel-to-ambient thermal resistance | ($t = 10\text{ s}$) | (Note 2) | $R_{th(ch-a)}$ | 44.6 | $^\circ\text{C/W}$ |
| Channel-to-ambient thermal resistance | ($t = 10\text{ s}$) | (Note 3) | $R_{th(ch-a)}$ | 78.1 | $^\circ\text{C/W}$ |

Note 1: Ensure that the channel temperature does not exceed 175°C .

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4: $V_{DD} = -24\text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 100\ \mu\text{H}$, $R_G = 25\ \Omega$, $I_{AR} = -45\text{ A}$

Note 5: Merely Channel temperature is guaranteed 175°C .

Storage temperature range is guaranteed as usual (-55 to 150°C).

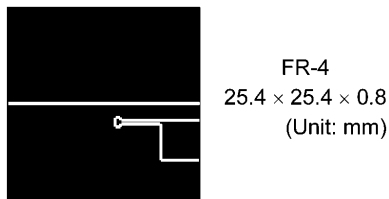


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

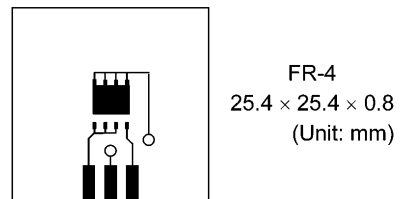


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

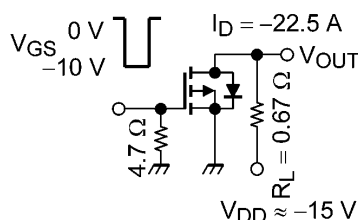
6.1. Static Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---------------|--|------|------|-----------|---------------|
| Gate leakage current | I_{GSS} | $V_{GS} = -20/+10\text{ V}, V_{DS} = 0\text{ V}$ | — | — | ± 100 | nA |
| Drain cut-off current | I_{DSS} | $V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$ | — | — | -10 | μA |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$ | -30 | — | — | V |
| Drain-source breakdown voltage (Note 6) | $V_{(BR)DSX}$ | $I_D = -10\text{ mA}, V_{GS} = 10\text{ V}$ | -21 | — | — | |
| Gate threshold voltage | V_{th} | $V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$ | -0.8 | — | -2.0 | |
| Drain-source on-resistance | $R_{DS(ON)}$ | $V_{GS} = -4.5\text{ V}, I_D = -22.5\text{ A}$ | — | 3.1 | 4.0 | m Ω |
| | | $V_{GS} = -10\text{ V}, I_D = -22.5\text{ A}$ | — | 2.4 | 3.0 | |

Note 6: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|--------------------------------|-----------|--|-----|------|-----|------|
| Input capacitance | C_{iss} | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | — | 7420 | — | pF |
| Reverse transfer capacitance | C_{rss} | | — | 1180 | — | |
| Output capacitance | C_{oss} | | — | 1440 | — | |
| Switching time (rise time) | t_r | See Figure 6.2.1. | — | 10 | — | ns |
| Switching time (turn-on time) | t_{on} | | — | 18 | — | |
| Switching time (fall time) | t_f | | — | 262 | — | |
| Switching time (turn-off time) | t_{off} | | — | 762 | — | |



Duty $\leq 1\%$, $t_w = 10\ \mu\text{s}$

Fig. 6.2.1 Switching Time Test Circuit

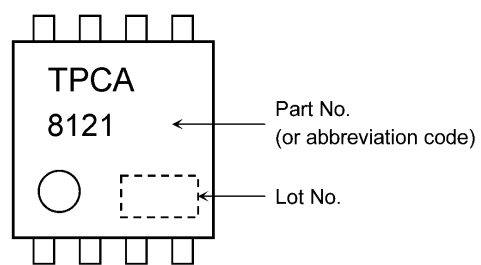
6.3. Gate Charge Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | Q_g | $V_{DD} \approx -24\text{ V}, V_{GS} = -10\text{ V}, I_D = -45\text{ A}$ | — | 190 | — | nC |
| Gate-source charge 1 | Q_{gs1} | | — | 23 | — | |
| Gate-drain charge | Q_{gd} | | — | 47 | — | |

6.4. Source-Drain Characteristics ($T_a = 25^\circ\text{C}$ unless otherwise specified)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|-----------|--|-----|------|------|------|
| Reverse drain current (pulsed) (Note 7) | I_{DRP} | — | — | — | -135 | A |
| Diode forward voltage | V_{DSF} | $I_{DR} = -45\text{ A}, V_{GS} = 0\text{ V}$ | — | — | 1.2 | V |

Note 7: Ensure that the channel temperature does not exceed 175°C .

7. Marking**Fig. 7.1 Marking**

8. Characteristics Curves (Note)

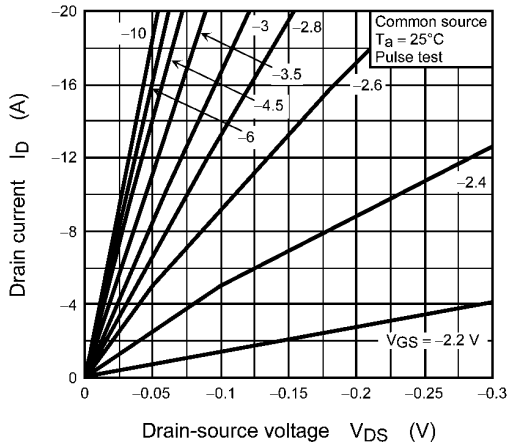


Fig. 8.1 $I_D - V_{DS}$

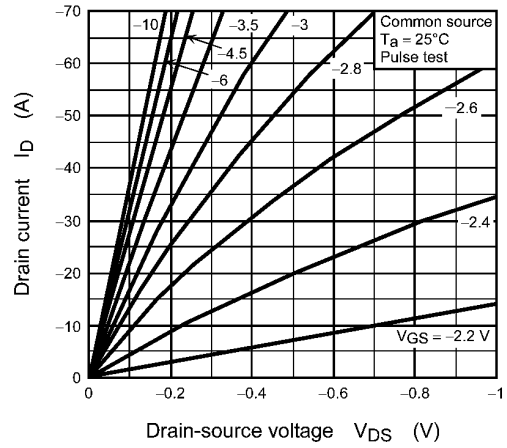


Fig. 8.2 $I_D - V_{DS}$

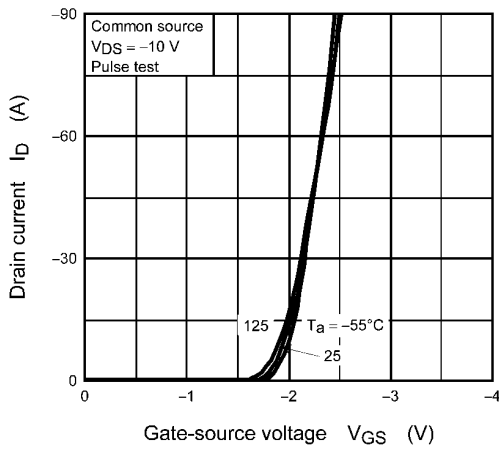


Fig. 8.3 $I_D - V_{GS}$

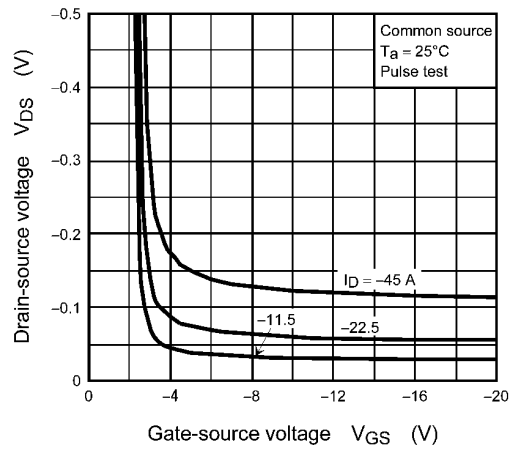


Fig. 8.4 $V_{DS} - V_{GS}$

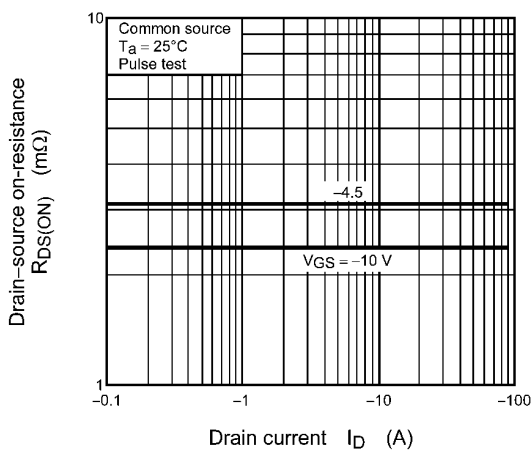


Fig. 8.5 $R_{DS(ON)} - I_D$

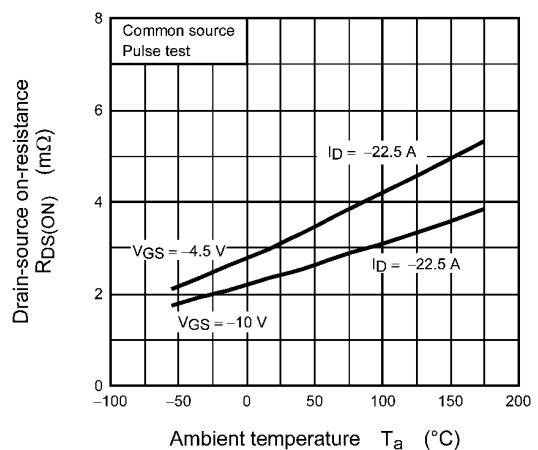


Fig. 8.6 $R_{DS(ON)} - T_a$

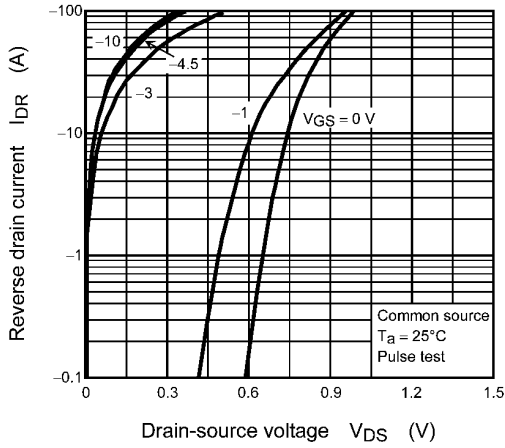


Fig. 8.7 I_{DR} - V_{DS}

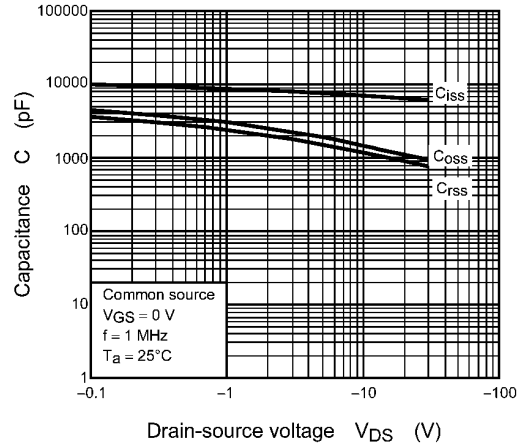


Fig. 8.8 Capacitance - V_{DS}

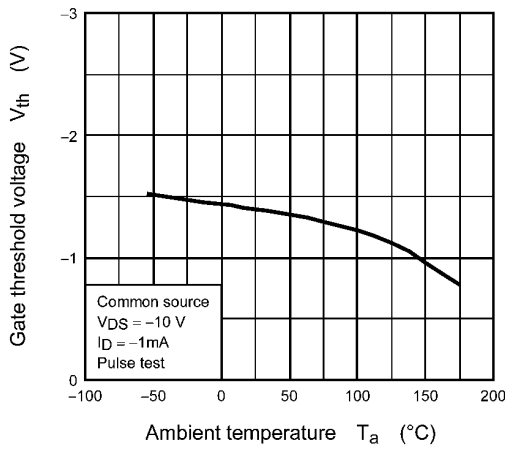


Fig. 8.9 V_{th} - T_a

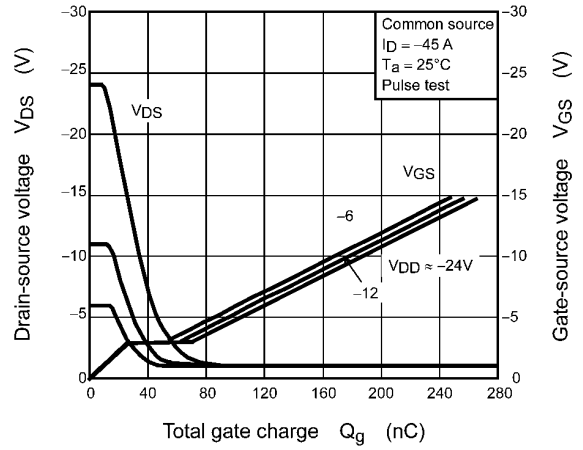
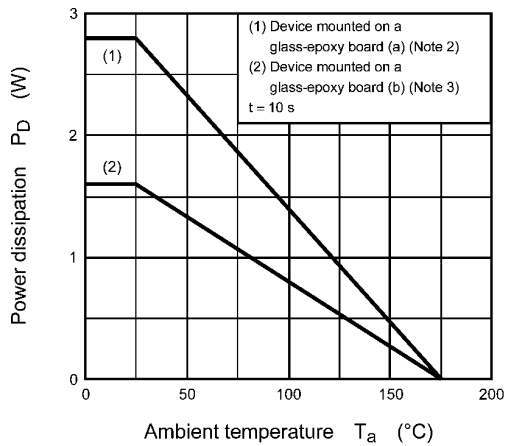
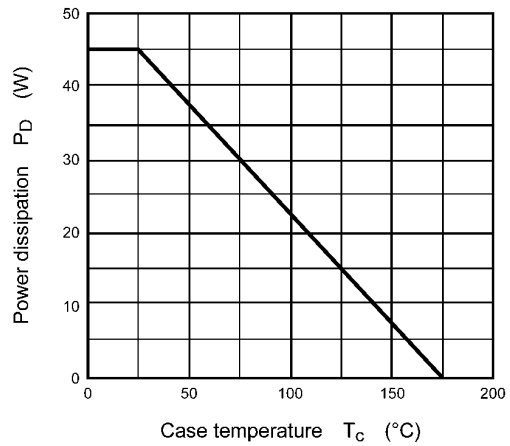


Fig. 8.10 Dynamic Input/Output Characteristics



**Fig. 8.11 P_D - T_a
(Guaranteed Maximum)**



**Fig. 8.12 P_D - T_c
(Guaranteed Maximum)**

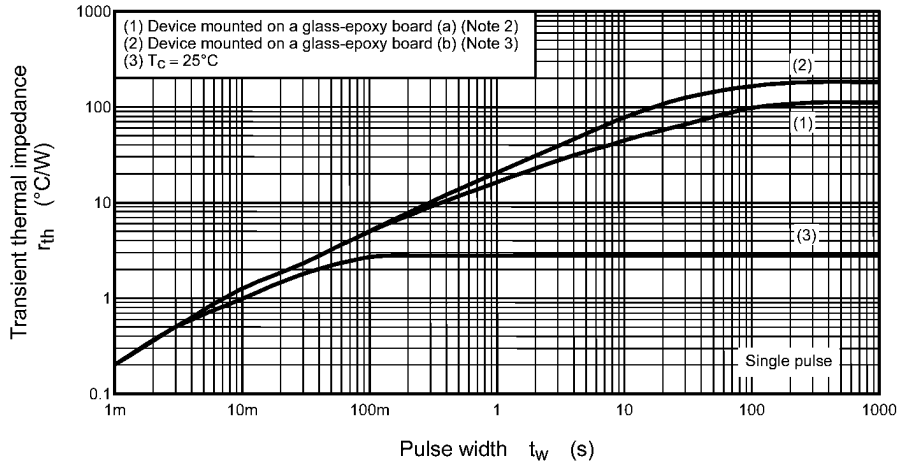


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

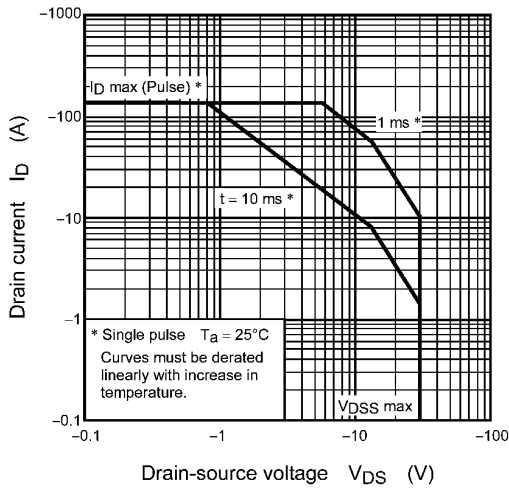


Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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