

MOSFETs Silicon N-Channel MOS (DTMOSIV)

# TK7Q60W

#### 1. Applications

· Switching Voltage Regulators

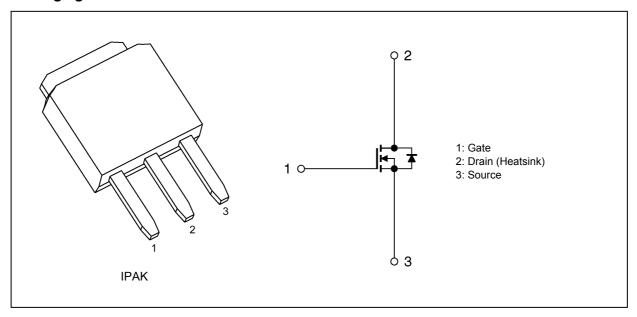
#### 2. Features

(1) Low drain-source on-resistance:  $R_{DS(ON)}$  = 0.5  $\Omega$  (typ.) by used to Super Junction Structure: DTMOS

(2) Easy to control Gate switching

(3) Enhancement mode:  $V_{th}$  = 2.7 to 3.7 V ( $V_{DS}$  = 10 V,  $I_{D}$  = 0.35 mA)

#### 3. Packaging and Internal Circuit



### 4. Absolute Maximum Ratings (Note) (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Rating	Unit	
Drain-source voltage		V <sub>DSS</sub>	600	V
Gate-source voltage		V <sub>GSS</sub>	±30	
Drain current (DC)	(Note 1)	I <sub>D</sub>	7.0	Α
Drain current (pulsed)	(Note 1)	I <sub>DP</sub>	28	
Power dissipation (T <sub>c</sub> = 25°C	)	P <sub>D</sub>	60	W
Single-pulse avalanche energy	(Note 2)	E <sub>AS</sub>	92	mJ
Avalanche current		I <sub>AR</sub>	1.8	Α
Reverse drain current (DC)	(Note 1)	I <sub>DR</sub>	7.0	
Reverse drain current (pulsed)	(Note 1)	I <sub>DRP</sub>	28	
Channel temperature		T <sub>ch</sub>	150	°C
Storage temperature		T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



#### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R <sub>th(ch-c)</sub>	2.09	°C/W
Channel-to-ambient thermal resistance	R <sub>th(ch-a)</sub>	125	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:  $V_{DD}$  = 90 V,  $T_{ch}$  = 25°C (initial), L = 49.9 mH,  $R_{G}$  = 25  $\Omega,$   $I_{AR}$  = 1.8 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

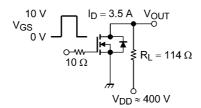
#### 6. Electrical Characteristics

## 6.1. Static Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I <sub>GSS</sub>	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	_	_	10	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	600	_	_	V
Gate threshold voltage	$V_{th}$	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.35 mA	2.7	_	3.7	
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.5 A	_	0.5	0.6	Ω

## 6.2. Dynamic Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 300 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	490	_	pF
Reverse transfer capacitance	C <sub>rss</sub>		_	1.7	_	
Output capacitance	C <sub>oss</sub>		_	13	_	
Effective output capacitance	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 to 400 V, V <sub>GS</sub> = 0 V	_	21	_	
Gate resistance	r <sub>g</sub>	V <sub>DS</sub> = OPEN, f = 1 MHz	_	7.0	_	Ω
Switching time (rise time)	t <sub>r</sub>	See Figure 6.2.1	_	18	_	ns
Switching time (turn-on time)	t <sub>on</sub>		_	40	_	
Switching time (fall time)	t <sub>f</sub>		_	7.0	_	
Switching time (turn-off time)	t <sub>off</sub>		_	55	_	
MOSFET dv/dt ruggedness	dv/dt	V <sub>DD</sub> = 0 to 400 V, I <sub>D</sub> = 3.5 A	25	_	_	V/ns



Duty  $\leq$  1%,  $t_W=10~\mu s$ 

Fig. 6.2.1 Switching Time Test Circuit

## 6.3. Gate Charge Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 7.0 \text{ A}$	_	15		nC
Gate-source charge 1	Q <sub>gs1</sub>			3.2	1	
Gate-drain charge	$Q_{gd}$		_	8.0	_	

## 6.4. Source-Drain Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	$V_{DSF}$	I <sub>DR</sub> = 7.0 A, V <sub>GS</sub> = 0 V	_	_	-1.7	V
Reverse recovery time	t <sub>rr</sub>	I <sub>DR</sub> = 3.5 A, V <sub>GS</sub> = 0 V	_	230	_	ns
Reverse recovery charge	$Q_{rr}$	-dI <sub>DR</sub> /dt = 100 A/μs	_	1.7	_	μС
Peak reverse recovery current	I <sub>rr</sub>		_	16	_	Α
Diode dv/dt ruggedness	dv/dt	$I_{DR} = 3.5 \text{ A}, V_{GS} = 0 \text{ V}, V_{DD} = 400 \text{ V}$	15	_		V/ns



## 7. Marking

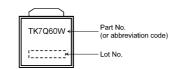
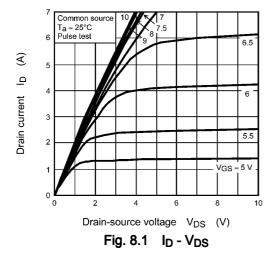
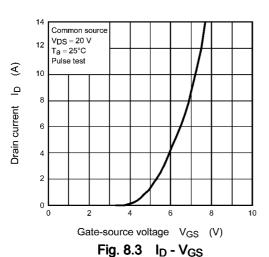
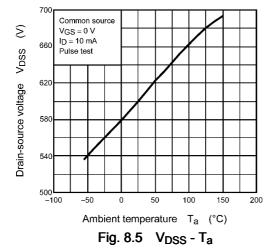


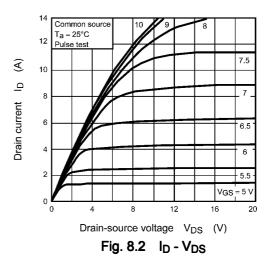
Fig. 7.1 Marking

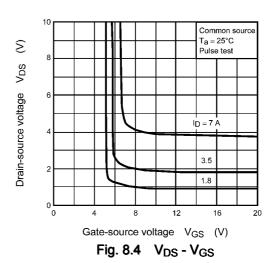
#### 8. Characteristics Curves (Note)











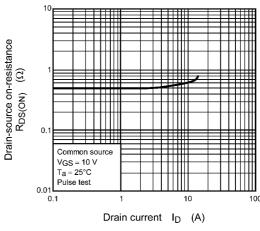


Fig. 8.6 R<sub>DS(ON)</sub> - I<sub>D</sub>

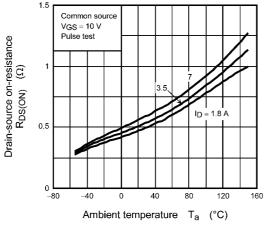


Fig. 8.7 R<sub>DS(ON)</sub> - T<sub>a</sub>

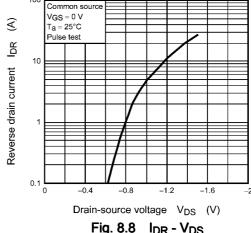


Fig. 8.8 IDR - VDS

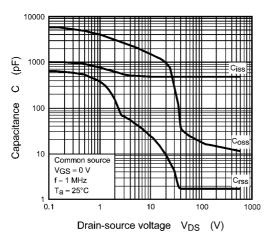


Fig. 8.9 C - V<sub>DS</sub>

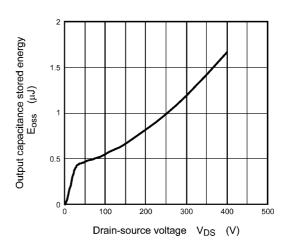


Fig. 8.10 E<sub>OSS</sub> - V<sub>DS</sub>

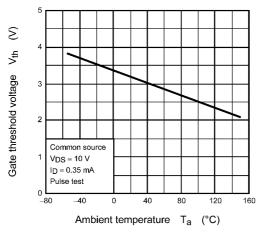


Fig. 8.11 V<sub>th</sub> - T<sub>a</sub>

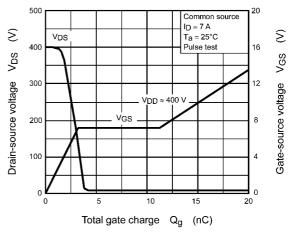


Fig. 8.12 Dynamic Input/Output Characteristics

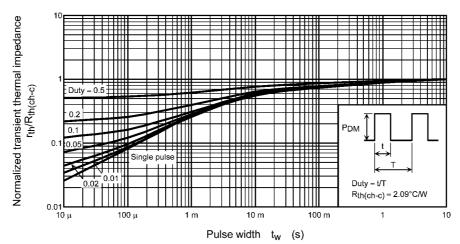


Fig. 8.13 r<sub>th</sub> - t<sub>w</sub> (Guaranteed Maximum)

80

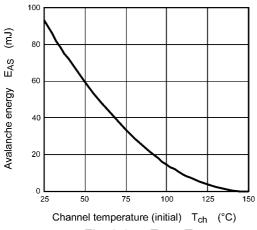


Fig. 8.14 E<sub>AS</sub> - T<sub>ch</sub> (Guaranteed Maximum)

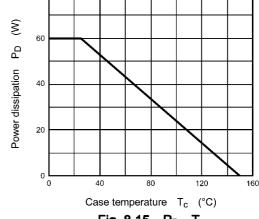
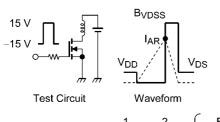


Fig. 8.15 P<sub>D</sub> - T<sub>c</sub> (Guaranteed Maximum)



 $R_G = 25 \Omega$ ,  $V_{DD} = 90 V$   $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left( \frac{BVDSS}{BVDSS - V_{DD}} \right)$ 

Fig. 8.16 Test Circuit/Waveform

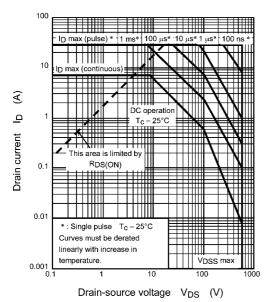


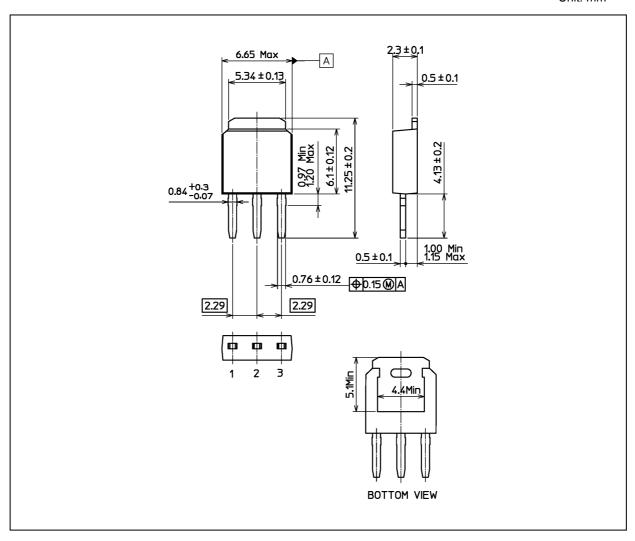
Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



## **Package Dimensions**

Unit: mm



Weight: 0.337 g (typ.)

	Package Name(s)
TOSHIBA: 2-7L1A	
Nickname: IPAK	



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