

MOSFETs Silicon N-Channel MOS (DTMOSIV)

TK39J60W

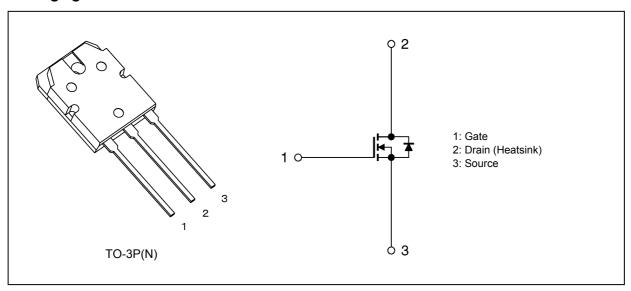
1. Applications

• Switching Voltage Regulators

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.055 Ω (typ.) by used to Super Junction Structure: DTMOS
- (2) Easy to control Gate switching
- (3) Enhancement mode: $V_{th} = 2.7$ to 3.7 V ($V_{DS} = 10$ V, $I_D = 1.9$ mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	±30	
Drain current (DC)	(Note 1)	I _D	38.8	Α
Drain current (pulsed)	(Note 1)	I _{DP}	155	
Power dissipation (7	Γ _c = 25°C)	P_{D}	270	W
Single-pulse avalanche energy	(Note 2)	E _{AS}	608	mJ
Avalanche current		I _{AR}	9.7	Α
Reverse drain current (DC)	(Note 1)	I _{DR}	38.8	
Reverse drain current (pulsed)	(Note 1)	I _{DRP}	155	
Channel temperature		T _{ch}	150	ç
Storage temperature		T _{stg}	-55 to 150	
Mounting torque		TOR	0.8	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance		0.463	°C/W
Channel-to-ambient thermal resistance		50	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 11.3 mH, R_{G} = 25 $\Omega,$ I_{AR} = 9.7 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



6. Electrical Characteristics

6.1. Static Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I _{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Drain cut-off current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V	_	_	10	
Drain-source breakdown voltage	V _{(BR)DSS}	I _D = 10 mA, V _{GS} = 0 V	600	_	_	V
Gate threshold voltage	V_{th}	V _{DS} = 10 V, I _D = 1.9 mA	2.7	_	3.7	
Drain-source on-resistance	R _{DS(ON)}	V _{GS} = 10 V, I _D = 19.4 A		0.055	0.065	Ω

6.2. Dynamic Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C _{iss}	$V_{DS} = 300 \text{ V}, V_{GS} = 0 \text{ V}, f = 100 \text{ kHz}$	_	4100	_	pF
Reverse transfer capacitance	C _{rss}		_	10	_	
Output capacitance	C _{oss}		_	90	_	
Effective output capacitance	C _{o(er)}	V _{DS} = 0 to 400 V, V _{GS} = 0 V	_	165	_	
Gate resistance	r _g	V _{DS} = OPEN, f = 1 MHz	_	2	_	Ω
Switching time (rise time)	t _r	See Figure 6.2.1	_	50	_	ns
Switching time (turn-on time)	t _{on}		_	80	_	
Switching time (fall time)	t _f		_	9	_	
Switching time (turn-off time)	t _{off}		_	200	_	
MOSFET dv/dt ruggedness	dv/dt	V _{DD} = 0 to 400 V, I _D = 9.7 A	50	_	_	V/ns

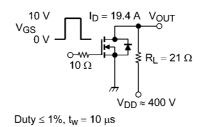


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 38.8 \text{ A}$	_	110		nC
Gate-source charge 1	Q _{gs1}		1	23		
Gate-drain charge	Q _{gd}		_	52	_	

6.4. Source-Drain Characteristics (T_a = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Diode forward voltage	V_{DSF}	I _{DR} = 38.8 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	I _{DR} = 19.4 A, V _{GS} = 0 V		450	_	ns
Reverse recovery charge	Q_{rr}]-dI _{DR} /dt = 50 A/μs	_	5	_	μС
Peak reverse recovery current	I _{rr}		_	21	_	Α
Diode dv/dt ruggedness	dv/dt	I _{DR} = 19.4 A, V _{GS} = 0 V, V _{DD} = 400 V	15		_	V/ns



7. Marking (Note)

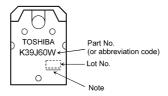


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS

compatibility of Product.

The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on

the restriction of the use of certain hazardous substances in electrical and electronic equipment.

8. Characteristics Curves (Note)

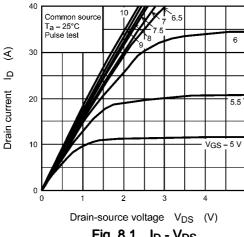


Fig. 8.1 I_D - V_{DS}

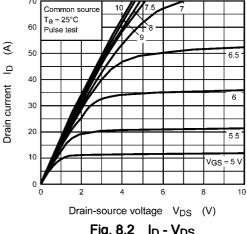


Fig. 8.2 I_D - V_{DS}

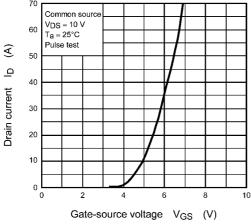


Fig. 8.3 ID - VGS

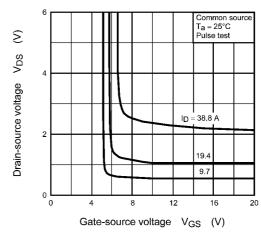


Fig. 8.4 V_{DS} - V_{GS}

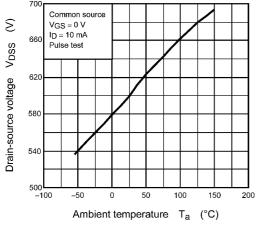


Fig. 8.5 V_{DSS} - T_a

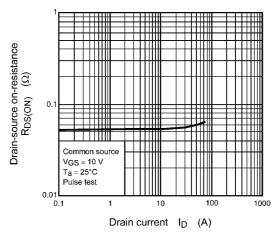


Fig. 8.6 R_{DS(ON)} - I_D

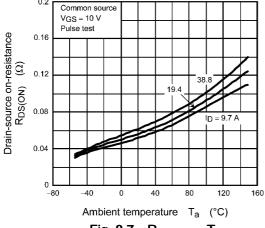


Fig. 8.7 R_{DS(ON)} - T_a

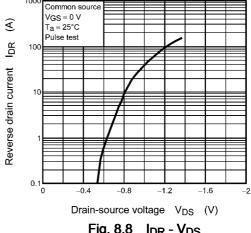


Fig. 8.8 IDR - VDS

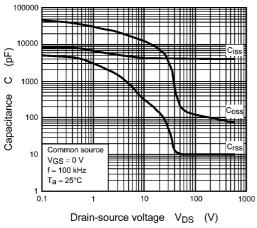


Fig. 8.9 $C - V_{DS}$

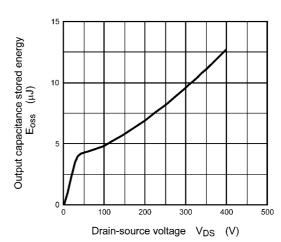


Fig. 8.10 Eoss - V_{DS}

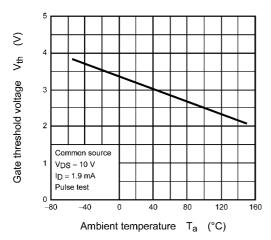


Fig. 8.11 V_{th} - T_a

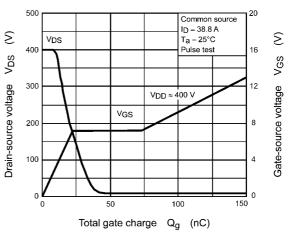


Fig. 8.12 Dynamic Input/Output Characteristics

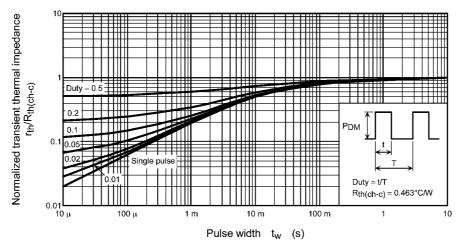


Fig. 8.13 r_{th} - t_w (Guaranteed Maximum)

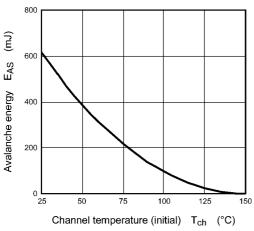


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)

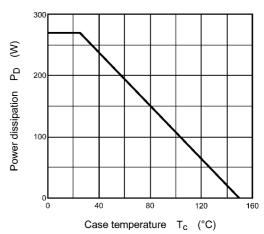


Fig. 8.15 P_D - T_c (Guaranteed Maximum)

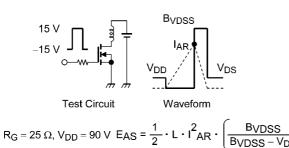


Fig. 8.16 Test Circuit/Waveform

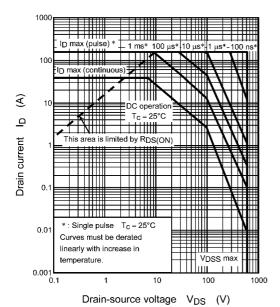


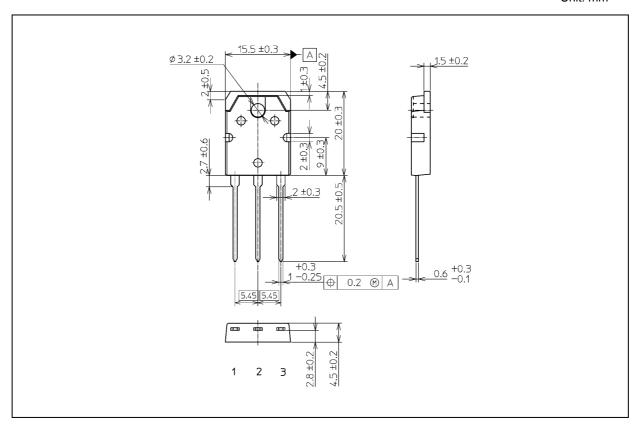
Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



Package Dimensions

Unit: mm



Weight: 4.6 g (typ.)

	Package Name(s)
JEITA: SC-65	
TOSHIBA: 2-16C1S	
Nickname: TO-3P(N)	



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