

# TC74HC4094AP, TC74HC4094AF

## 8-Bit Shift and Store Register (3-state)

The TC74HC4094A is a high speed CMOS 8-BIT SHIFT AND STROBE REGISTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

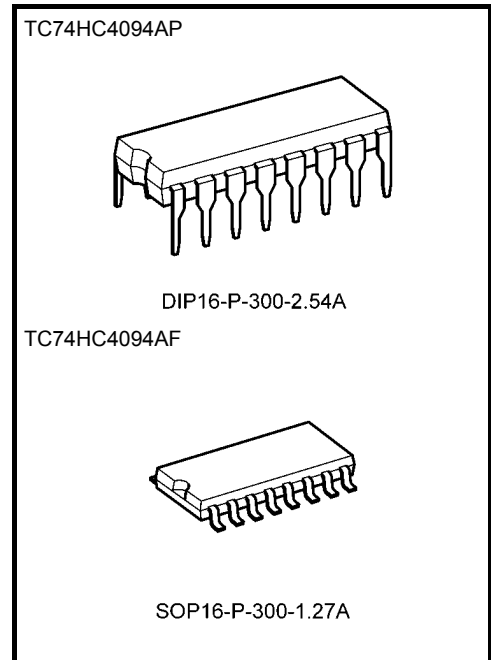
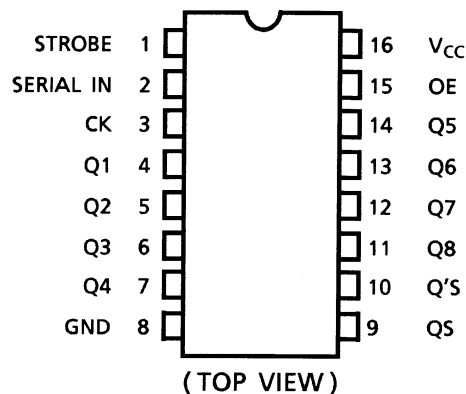
It consists of an 8-bit shift register and an 8-bit latch with 3-state output buffers. Data is shifted serially through the shift register on the positive going transition of the CK input. The output of the last stage (Q<sub>s</sub>) can be used to cascade several devices. Data on the Q<sub>s</sub> output is transferred to a second output (Q'<sub>s</sub>) on the following negative transition of the CK input. The data in each stage of the shift register is provided to a corresponding latch, on the negative going transition of the STROBE input. When STROBE is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is set high.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

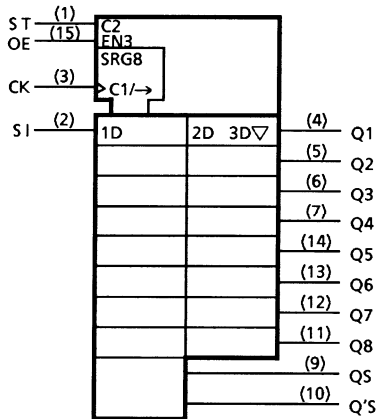
- High speed:  $f_{max} = 73 \text{ MHz (typ.) at } V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \mu\text{A (max) at } T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (min)}$
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{OH}| = I_{OL} = 4 \text{ mA (min)}$
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} \text{ (opr)} = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 4094B

### Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

## IEC Logic Symbol



## Truth Table

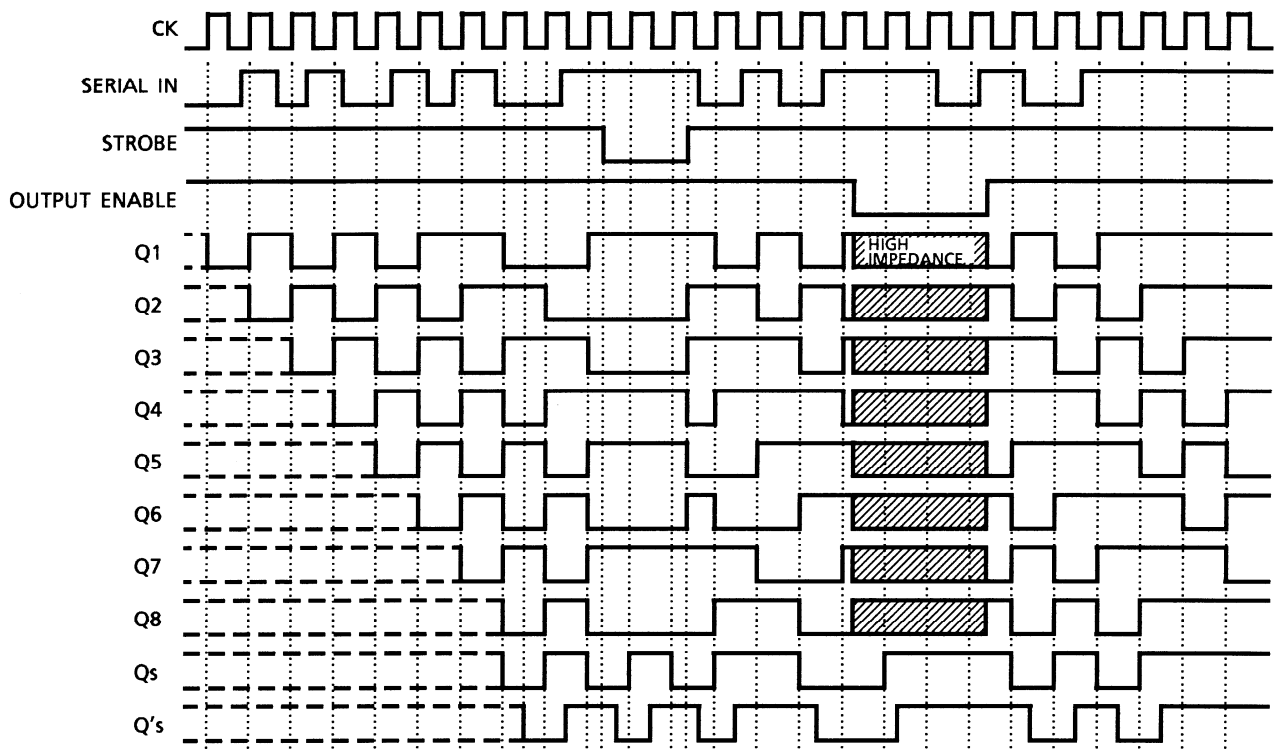
CK	OE	ST	SI	Para. Out		Seri. Out	
				Q1	Qn	Qs	Q's
	H	H	L	L	Qn - 1	Q7	NC
	H	H	H	H	Qn - 1	Q7	NC
	H	L	*	NC	NC	Q7	NC
	L	*	*	Z	Z	Q7	NC
	H	*	*	NC	NC	NC	Qs
	L	*	*	Z	Z	NC	Qs

X: Don't care

NC: No change

Z: High impedance

## Timing Chart





## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit	
				Min	Typ.	Max	Min	Max		
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	1.50	—	V	
			4.5	3.15	—	—	3.15	—		
			6.0	4.20	—	—	4.20	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	—	0.50	V	
			4.5	—	—	1.35	—	1.35		
			6.0	—	—	1.80	—	1.80		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
				6.0	5.68	5.80	—	5.63	—	
				6.0	—	—	—	—	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			$I_{OL} = 4 \text{ mA}$ $I_{OL} = 5.2 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
				6.0	—	0.18	0.26	—	0.33	
				6.0	—	—	—	—	—	
3-state output off-state current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	6.0	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu\text{A}$	
Input leakage current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	6.0	—	—	4.0	—	40.0	$\mu\text{A}$	

### Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_W$ (H) $t_W$ (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width (STROBE)	$t_W$ (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (SERIAL)	$t_s$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time (STROBE)	$t_s$	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum hold time (SERIAL)	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum hold time (STROBE)	$t_h$	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

### AC Characteristics ( $C_L = 15$ pF, $V_{CC} = 5$ V, $T_a = 25^\circ\text{C}$ , input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$	—	—	4	8	ns
	$t_{THL}$					
Propagation delay time (CK-Qn)	$t_{pLH}$	—	—	22	35	ns
	$t_{pHL}$					
Propagation delay time (CK-QS, Q'S)	$t_{pLH}$	—	—	16	25	ns
	$t_{pHL}$					
Propagation delay time (STROBE-Qn)	$t_{pLH}$	—	—	16	27	ns
	$t_{pHL}$					
3-state output enable time	$t_{pZL}$	$R_L = 1$ k $\Omega$	—	13	25	ns
	$t_{pZH}$					
Maximum clock frequency	$f_{max}$	—	33	73	—	MHz

## AC Characteristics ( $C_L = 50 \text{ pF}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ.	Max	Min	Max	
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (CK-Qn)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	92	200	—	250	ns
			4.5	—	26	40	—	50	
			6.0	—	20	34	—	43	
Propagation delay time (CK-QS, Q'S)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	65	150	—	190	ns
			4.5	—	19	30	—	38	
			6.0	—	15	26	—	32	
Propagation delay time (STROBE-Qn)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	75	160	—	200	ns
			4.5	—	20	32	—	40	
			6.0	—	16	27	—	34	
3-state output enable time	$t_{pZL}$ $t_{pZH}$	$R_L = 1 \text{ k}\Omega$	2.0	—	58	150	—	190	ns
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
3-state output disable time	$t_{pLZ}$ $t_{pHZ}$	$R_L = 1 \text{ k}\Omega$	2.0	—	35	150	—	190	ns
			4.5	—	16	30	—	38	
			6.0	—	13	26	—	32	
Maximum clock frequency	$f_{max}$	—	2.0	6	16	—	5	—	MHz
			4.5	30	66	—	24	—	
			6.0	35	80	—	28	—	
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF	
Bus input capacitance	$C_{OUT}$	—	—	10	—	—	—	pF	
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	140	—	—	—	pF	

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

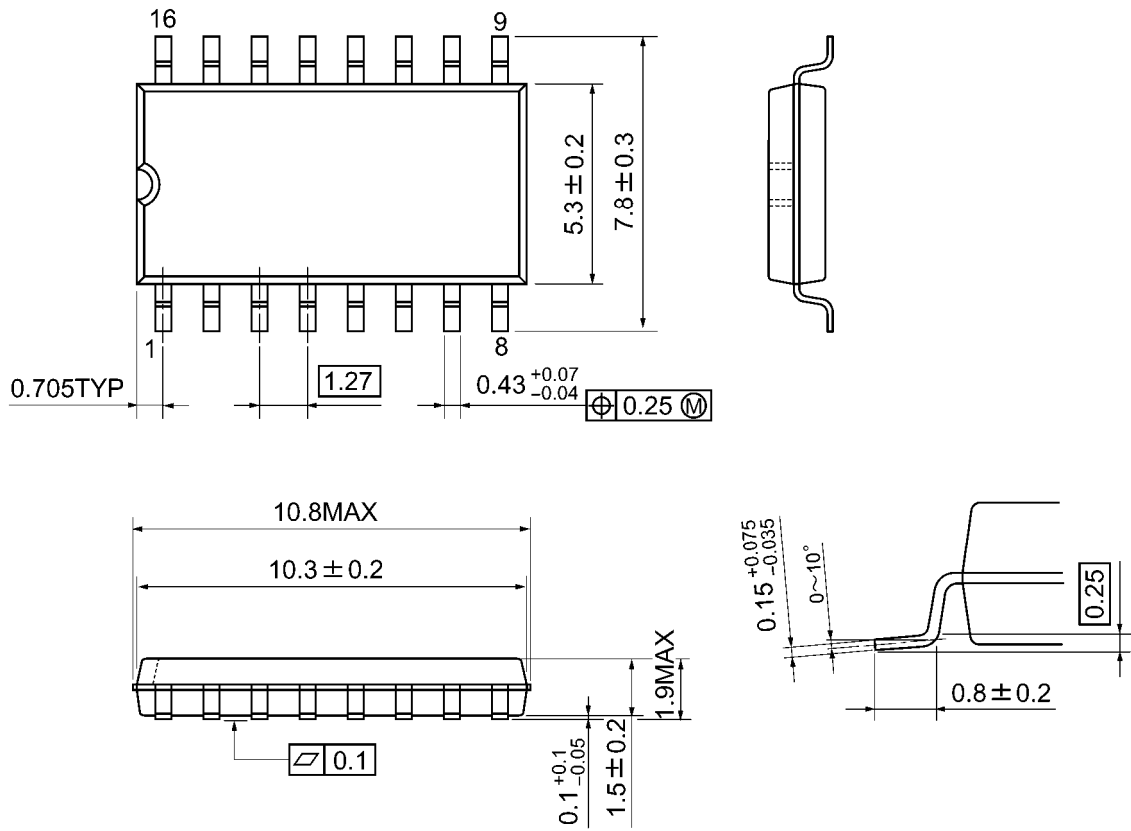


Weight: 1.00 g (typ.)

**Package Dimensions**

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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