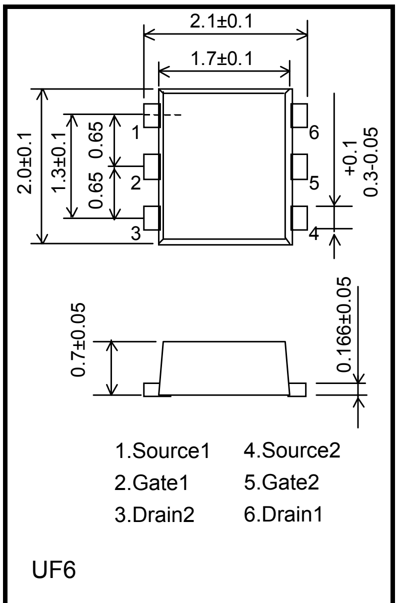
TOSHIBA Field-Effect Transistor Silicon N / P Channel MOS Type

# SSM6L40TU

○ Power Management Switch Applications
○ High-Speed Switching Applications

- N-ch: 4.0-V drive
  P-ch: 4.0 -V drive
- N-ch, P-ch, 2-in-1
- Low ON-resistance Q1 N-ch: $R_{on}$ = 182 mΩ (max) (@$V_{GS}$ = 4 V)
  $R_{on}$ = 122 mΩ (max) (@$V_{GS}$ = 10 V)
  Q2 P-ch: $R_{on}$ = 403 mΩ (max) (@$V_{GS}$ = -4 V)
  $R_{on}$ = 226 mΩ (max) (@$V_{GS}$ = -10 V)

Unit: mm




| | |
|---|---|
| JEDEC | ― |
| JEITA | ― |
| TOSHIBA | 2-2T1B |

Weight: 7.0 mg (typ.)

### Q1 Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 30 | V |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC | $I_D$ | 1.6 | A |
| | Pulse | $I_{DP}$ | 3.2 | |

### Q2 Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | −30 | V |
| Gate-source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC | $I_D$ | −1.4 | A |
| | Pulse | $I_{DP}$ | −2.8 | |

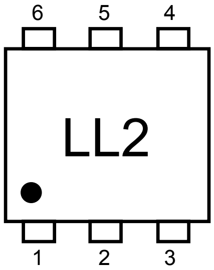
### Absolute Maximum Ratings (Ta = 25 °C) (Q1, Q2 Common)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Drain power dissipation | $P_D$(Note 1) | 500 | mW |
| Channel temperature | $T_{ch}$ | 150 | °C |
| Storage temperature range | $T_{stg}$ | −55 to 150 | °C |

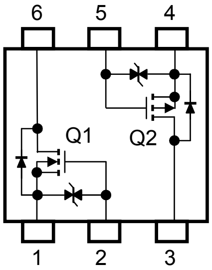
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note1: Mounted on an FR4 board. (total dissipation)
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 645 $mm^2$ )

### Marking




### Equivalent Circuit (top view)



## Q1 Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 30 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = 1 mA, $V_{GS}$ = -20 V | 15 | — | — | |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ =30 V, $V_{GS}$ = 0 V | — | — | 1 | μA |
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 V | — | — | ±1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 5 V, $I_D$ = 1 mA | 1.0 | — | 2.6 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 5 V, $I_D$ = 1A (Note 2) | 1.9 | 3.7 | — | S |
| Drain-source ON-resistance | | $R_{DS\ (ON)}$ | $I_D$ = 1 A, $V_{GS}$ = 10 V (Note 2) | — | 96 | 122 | mΩ |
| | | | $I_D$ = 0.5 A, $V_{GS}$ = 4 V (Note 2) | — | 130 | 182 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 180 | — | pF |
| Output capacitance | | $C_{oss}$ | | — | 34 | — | |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 27 | — | |
| Total Gate Charge | | $Q_g$ | $V_{DS}$ = 15 V, $I_D$ = 1.6 A<br>$V_{GS}$ = 10 V | — | 5.1 | — | nC |
| Gate–Source Charge | | $Q_{gs}$ | | — | 3.9 | — | |
| Gate–Drain Charge | | $Q_{gd}$ | | — | 1.2 | — | |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 15 V, $I_D$ = 0.5 A<br>$V_{GS}$ = 0 to 4 V, $R_G$ = 10 Ω | — | 9.5 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 9.0 | — | |
| Drain-source forward voltage | | $V_{DSF}$ | $I_D$ = -1.6 A, $V_{GS}$ = 0 V (Note 2) | — | -0.8 | -1.2 | V |

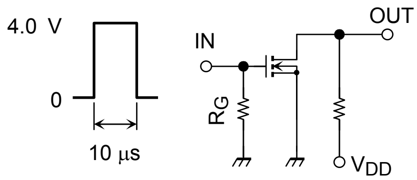
## Q2 Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = -1 mA, $V_{GS}$ = 0 V | -30 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = -1 mA, $V_{GS}$ = +20 V | -15 | — | — | |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = -30 V, $V_{GS}$ = 0 V | — | — | -10 | μA |
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 V | — | — | ±1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = -5 V, $I_D$ = -1 mA | -0.8 | — | -2.0 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = -5 V, $I_D$ = -1 A (Note 2) | 1.0 | 2.0 | — | S |
| Drain-source ON-resistance | | $R_{DS\ (ON)}$ | $I_D$ = -1.0 A, $V_{GS}$ = -10 V (Note 2) | — | 175 | 226 | mΩ |
| | | | $I_D$ = -0.5 A, $V_{GS}$ = -4.0 V (Note 2) | — | 290 | 403 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = -15 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 120 | — | pF |
| Output capacitance | | $C_{oss}$ | | — | 32 | — | |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 21 | — | |
| Total Gate Charge | | $Q_g$ | $V_{DS}$ = -15 V, $I_D$ = -1.4 A<br>$V_{GS}$ = -10 V | — | 2.9 | — | nC |
| Gate–Source Charge | | $Q_{gs}$ | | — | 2.2 | — | |
| Gate–Drain Charge | | $Q_{gd}$ | | — | 0.7 | — | |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = -15 V, $I_D$ = -1 A,<br>$V_{GS}$ = 0 to -4 V, $R_G$ = 10 Ω | — | 12 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 8.5 | — | |
| Drain-source forward voltage | | $V_{DSF}$ | $I_D$ = 1.4 A, $V_{GS}$ = 0 V (Note 2) | — | 0.87 | 1.2 | V |

Note 2: Pulse test

## Q1 Switching Time Test Circuit

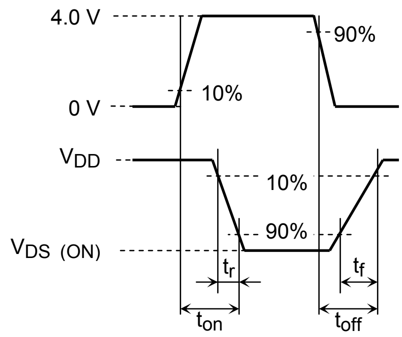
**(a) Test Circuit**




$V_{DD}$ = 15 V
$R_G$ = 10 Ω
D.U. ≤ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

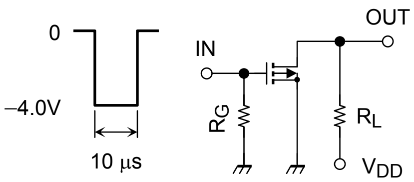
**(b) $V_{IN}$**

**(c) $V_{OUT}$**




## Q2 Switching Time Test Circuit

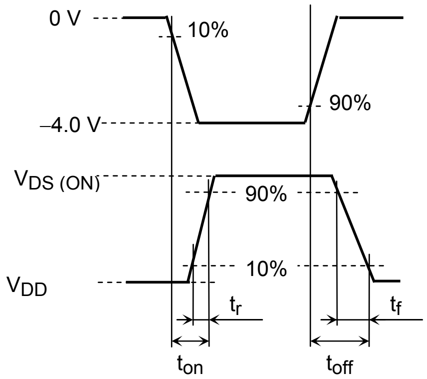
**(a) Test Circuit**




$V_{DD}$ =− 15 V
$R_G$ = 10 Ω
D.U. ≤ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

**(b) $V_{IN}$**

**(c) $V_{OUT}$**




## Q1 Usage Considerations

Let $V_{th}$ be the voltage applied between gate and source that causes the drain current ($I_D$) to below (1 mA for the Q1 of the SSM6L40TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th}$, and $V_{GS(off)}$ must be lower than $V_{th}$. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

Take this into consideration when using the device.

## Q2 Usage Considerations

Let $V_{th}$ be the voltage applied between gate and source that causes the drain current ($I_D$) to below (−1 mA for the Q2 of the SSM6L40TU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than $V_{th}$, and $V_{GS(off)}$ must be lower than $V_{th}$. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

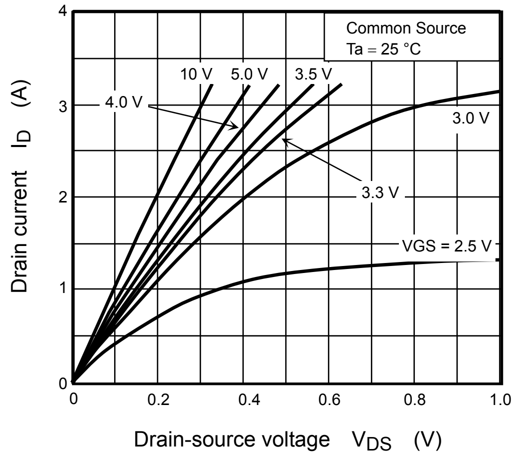
Take this into consideration when using the device.

## Handling Precaution

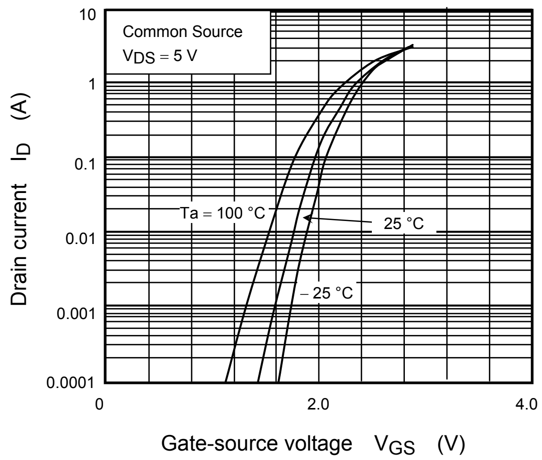
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

## Q1 (N-ch MOSFET)

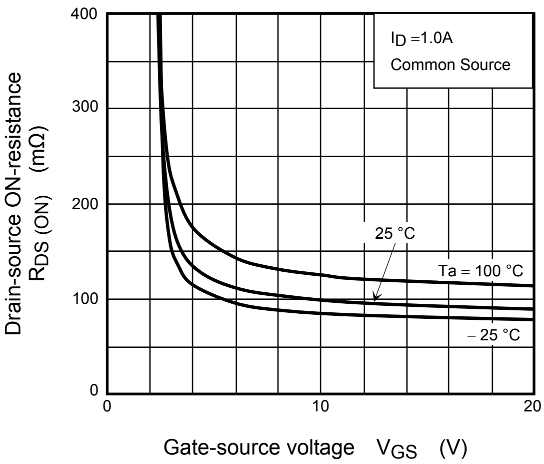
$I_D$ – $V_{DS}$



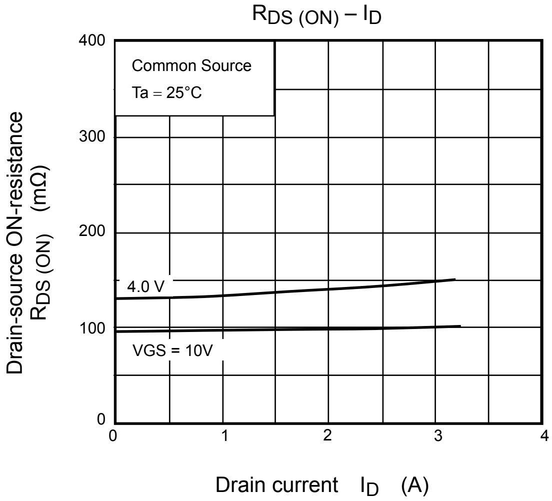

$I_D$ – $V_{GS}$



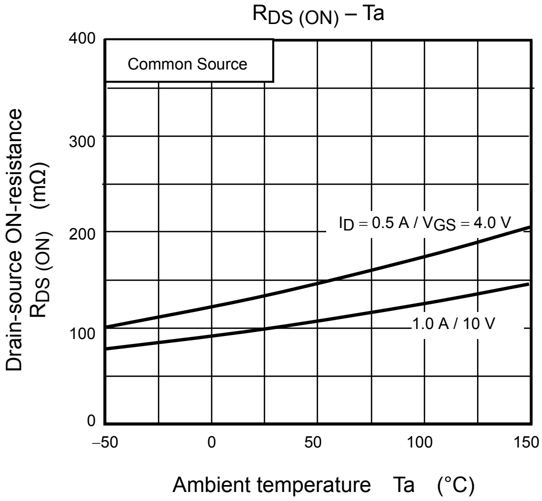

$R_{DS (ON)}$ – $V_{GS}$



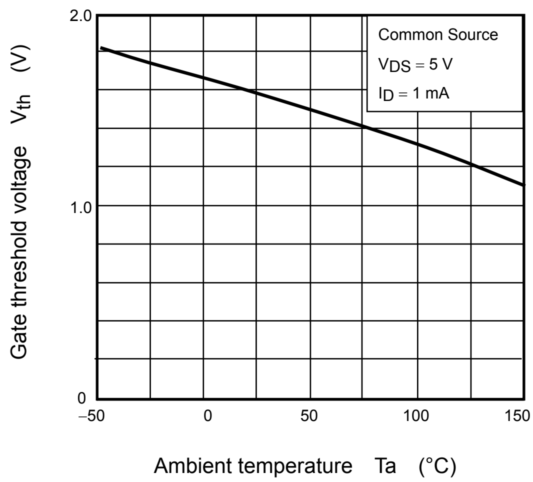

$R_{DS (ON)}$ – $I_D$



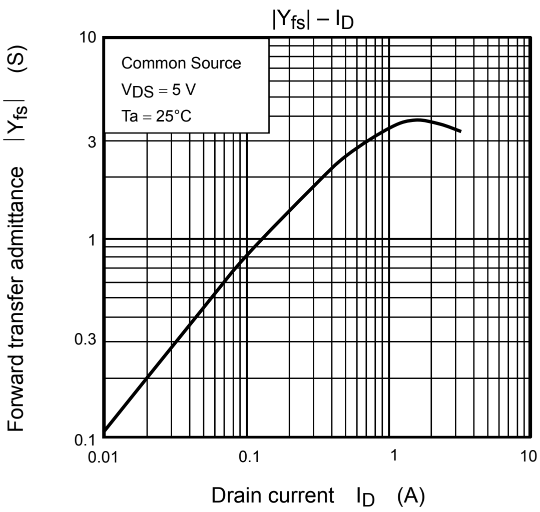

$R_{DS (ON)}$ – Ta

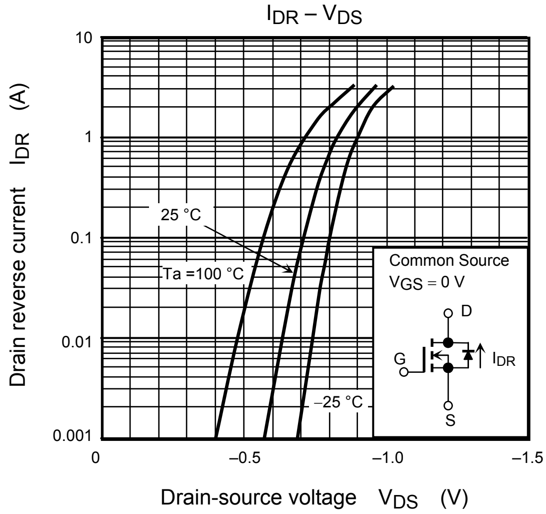


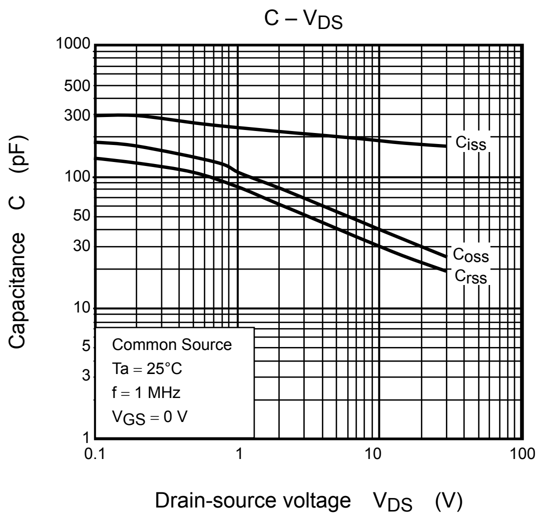

$V_{th}$ – Ta

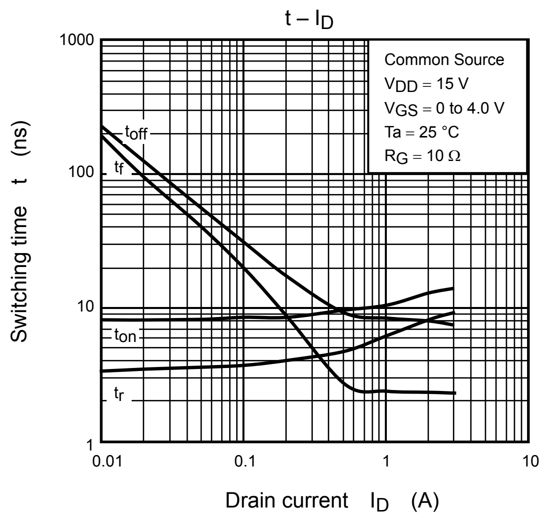


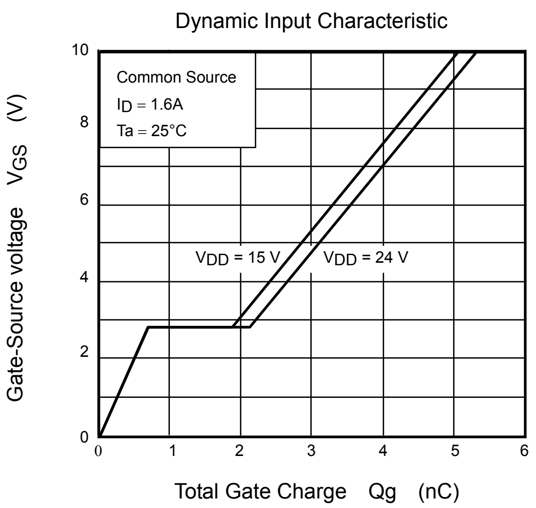
## Q1 (N-ch MOSFET)



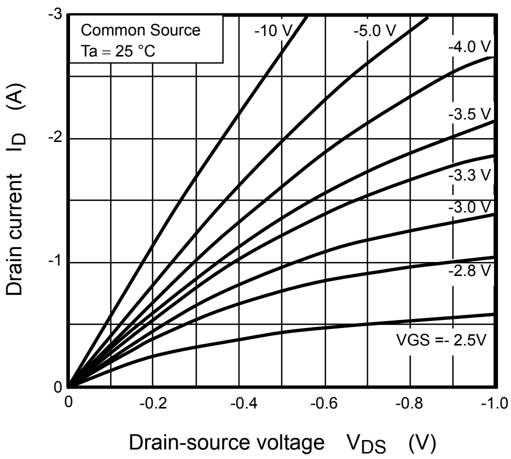



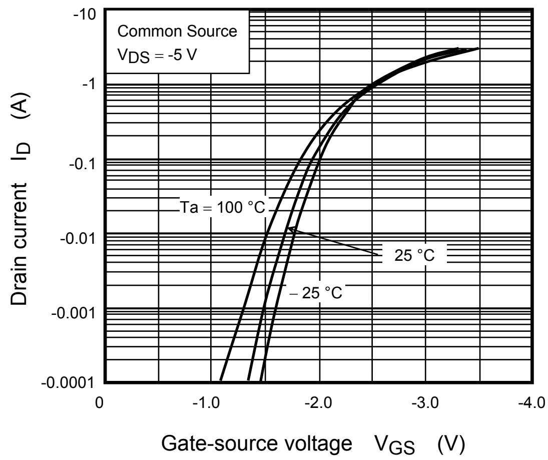



## Q2 (P-ch MOSFET)

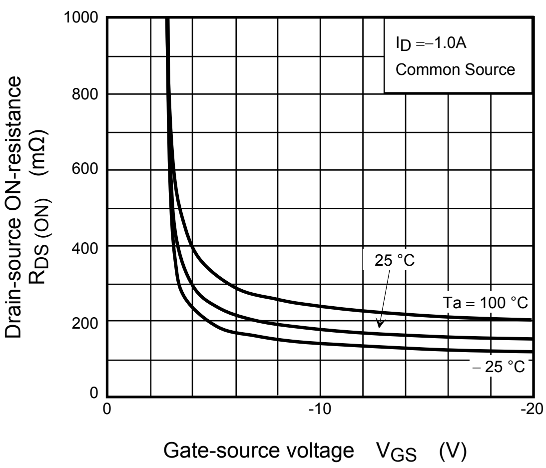
$I_D$ – $V_{DS}$



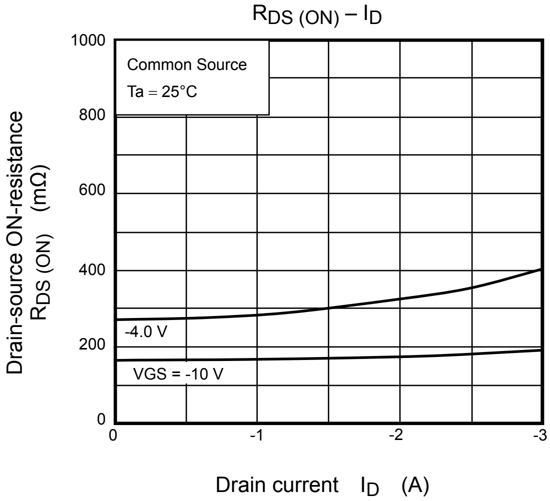

$I_D$ – $V_{GS}$



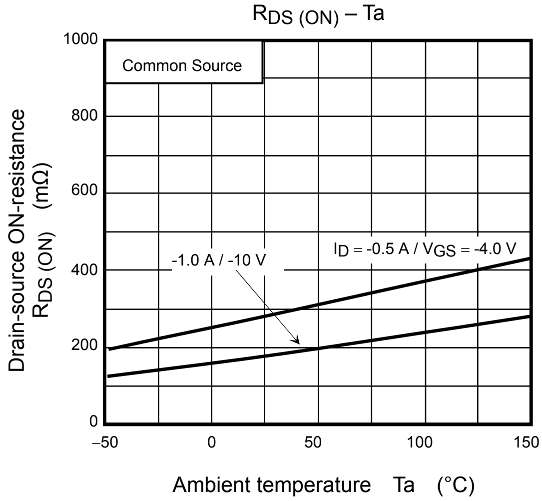

$R_{DS\ (ON)}$ – $V_{GS}$



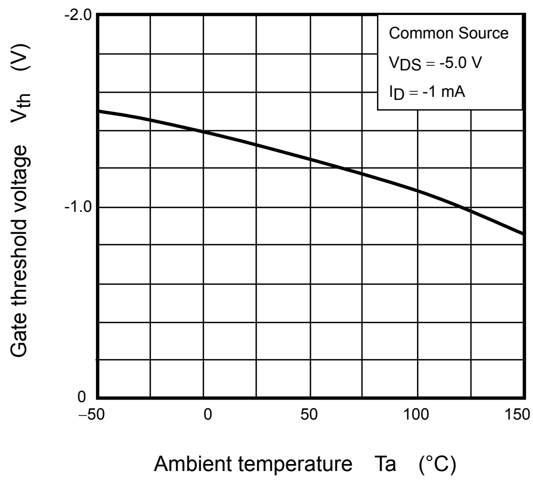

$R_{DS\ (ON)}$ – $I_D$



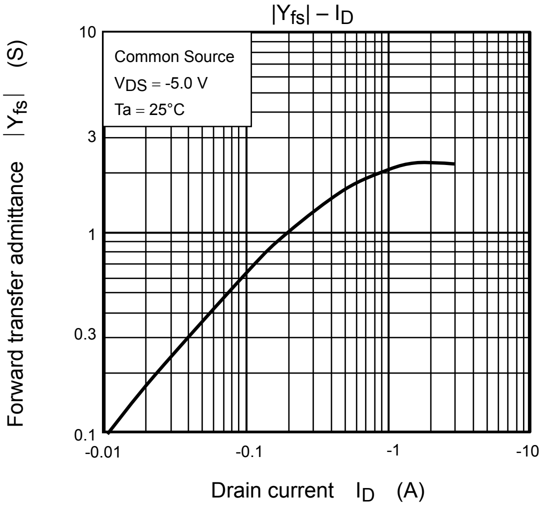

$R_{DS\ (ON)}$ – Ta

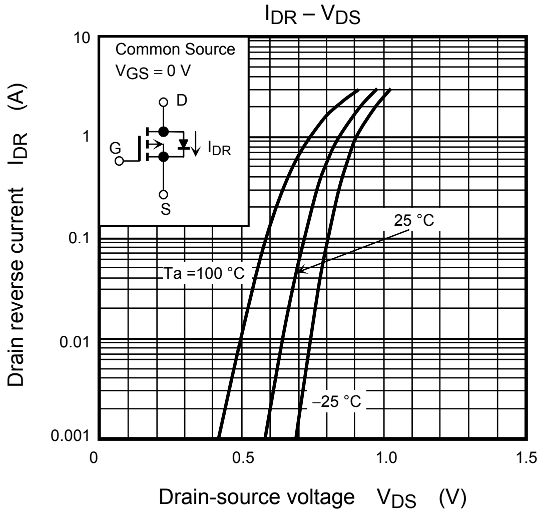


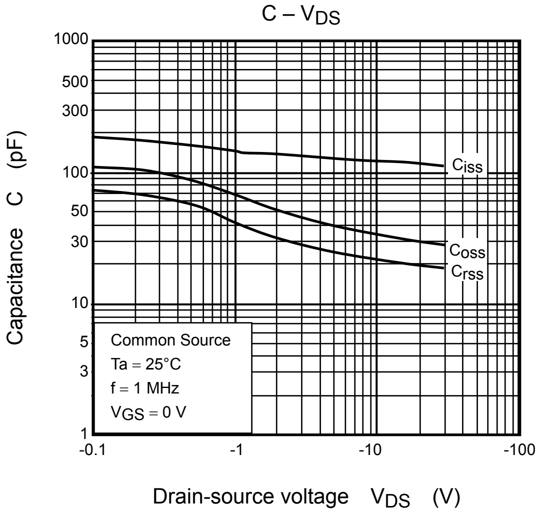

$V_{th}$ – Ta

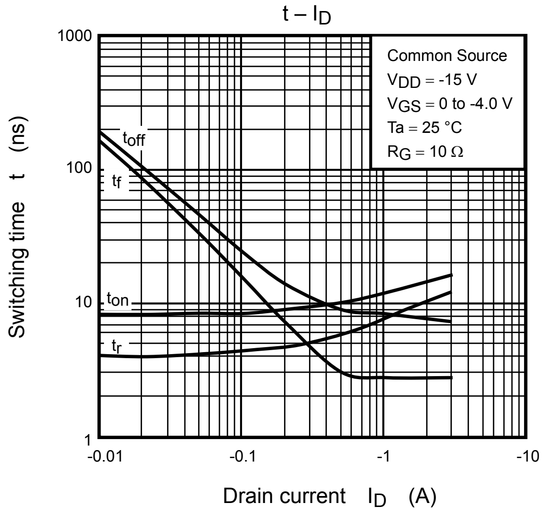


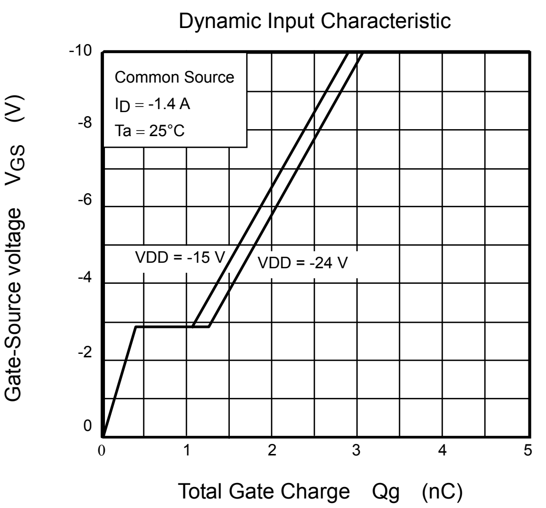
## Q2 (P-ch MOSFET)



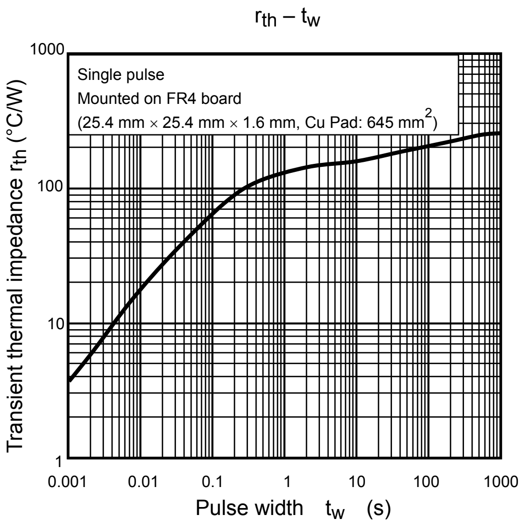



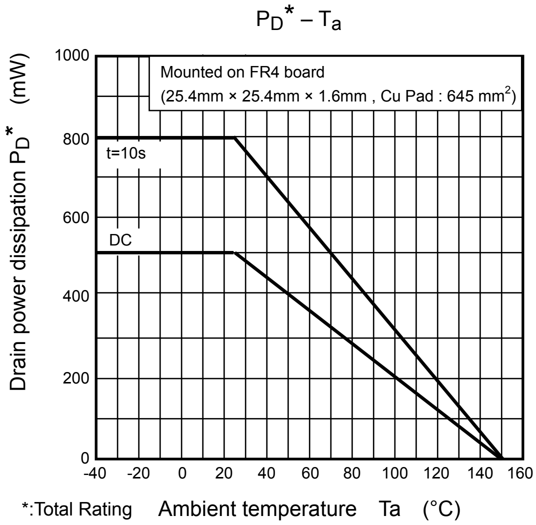



## Q1, Q2 Common


$r_{th}$ – $t_w$
Single pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)
Transient thermal impedance $r_{th}$ (°C/W)
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width $t_w$ (s)


$P_D$* – $T_a$
Mounted on FR4 board
(25.4mm × 25.4mm × 1.6mm , Cu Pad : 645 mm²)
t=10s
DC
Drain power dissipation $P_D$* (mW)
1000
800
600
400
200
0
-40
-20
0
20
40
60
80
100
120
140
160
*:Total Rating
Ambient temperature Ta (°C)

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