

TOSHIBA Field-Effect Transistor Silicon P / N Channel MOS Type

SSM6L13TU

Power Management Switch Applications

High-Speed Switching Applications

- 1.8-V drive
- N-ch, P-ch 2-in-1
- Low ON-resistance: Nch $R_{DS(ON)} = 235 \text{ m}\Omega$ (max) (@ $V_{GS} = 1.8 \text{ V}$)
- $R_{DS(ON)} = 178 \text{ m}\Omega$ (max) (@ $V_{GS} = 2.5 \text{ V}$)
- : Pch $R_{DS(ON)} = 460 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.8 \text{ V}$)
- $R_{DS(ON)} = 306 \text{ m}\Omega$ (max) (@ $V_{GS} = -2.5 \text{ V}$)

Q1 Absolute Maximum Ratings (Ta = 25 °C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	20	V
Gate-source voltage		V_{GSS}	± 12	V
Drain current	DC	I_D	0.8	A
	Pulse	I_{DP}	1.6	

Q2 Absolute Maximum Ratings (Ta = 25 °C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DS}	-20	V
Gate-source voltage		V_{GSS}	± 8	V
Drain current	DC	I_D	-0.8	A
	Pulse	I_{DP}	-1.6	

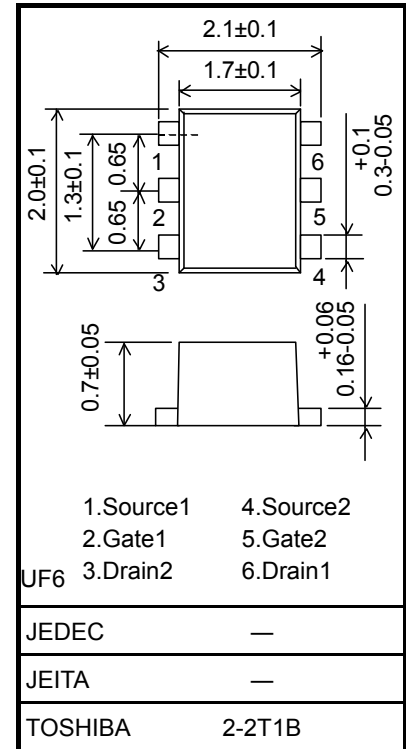
Absolute Maximum Ratings (Q1, Q2 Common) (Ta = 25 °C)

Characteristic	Symbol	Rating	Unit
Power dissipation	P_D (Note 1)	500	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

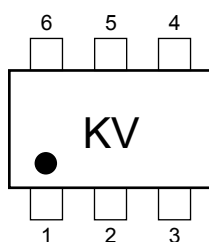
Note 1: Mounted on an FR4 board (total dissipation)
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

Unit: mm

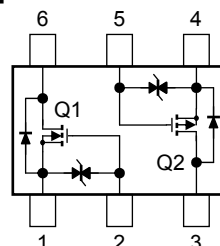


Weight: 7 mg (typ.)

Marking



Equivalent Circuit (top view)



Q1 Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit	
Drain-source breakdown voltage	$V_{(BR) DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	20	—	—	V	
	$V_{(BR) DSX}$	$I_D = 1 \text{ mA}, V_{GS} = -12 \text{ V}$	10	—	—		
Drain cutoff current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0$	—	—	1	μA	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$	—	—	± 1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.4	—	1.0	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 0.6 \text{ A}$ (Note 2)	2.3	3.75	—	S	
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 0.6 \text{ A}, V_{GS} = 4.0 \text{ V}$ (Note 2)	—	116	143	m Ω	
		$I_D = 0.4 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note 2)	—	134	178		
		$I_D = 0.2 \text{ A}, V_{GS} = 1.8 \text{ V}$ (Note 2)	—	160	235		
Input capacitance	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	268	—	pF	
Output capacitance	C_{oss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	44	—	pF	
Reverse transfer capacitance	C_{rss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	34	—	pF	
Switching time	Turn-on time	t_{on}	$V_{DD} = 10 \text{ V}, I_D = 0.25 \text{ A},$ $V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 4.7 \Omega$	—	9	—	ns
	Turn-off time	t_{off}		—	16	—	
Drain-source forward voltage	V_{DSF}	$I_D = -0.8 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	—	-0.8	-1.15	V	

Note 2 : Pulse test

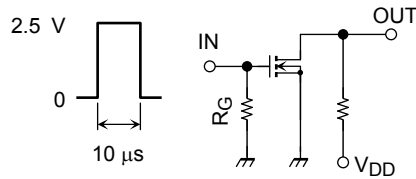
Q2 Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit	
Drain-source breakdown voltage	$V_{(BR) DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-20	—	—	V	
	$V_{(BR) DSX}$	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-12	—	—		
Drain cutoff current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	—	—	-10	μA	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$	—	—	± 1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -0.6 \text{ A}$ (Note 2)	1.5	2.5	—	S	
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -0.6 \text{ A}, V_{GS} = -4.0 \text{ V}$ (Note 2)	—	175	234	m Ω	
		$I_D = -0.4 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 2)	—	230	306		
		$I_D = -0.1 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 2)	—	300	460		
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	250	—	pF	
Output capacitance	C_{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	45	—	pF	
Reverse transfer capacitance	C_{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	35	—	pF	
Switching time	Turn-on time	t_{on}	$V_{DD} = -10 \text{ V}, I_D = -0.25 \text{ A},$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}, R_G = 4.7 \Omega$	—	12	—	ns
	Turn-off time	t_{off}		—	18	—	
Drain-source forward voltage	V_{DSF}	$I_D = 0.8 \text{ A}, V_{GS} = 0 \text{ V}$ (Note 2)	—	0.85	1.2	V	

Note 2: Pulse test

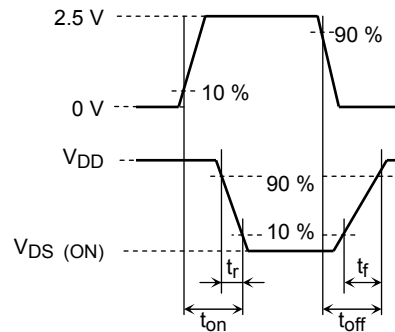
Q1 Switching Time Test Circuit

(a) Test Circuit

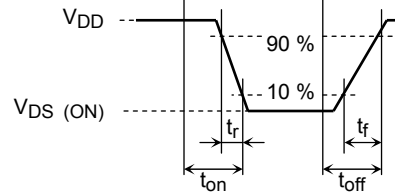


$V_{DD} = 10\text{ V}$
 $R_G = 4.7\ \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
 Common Source
 $T_a = 25\text{ }^\circ\text{C}$

(b) V_{IN}

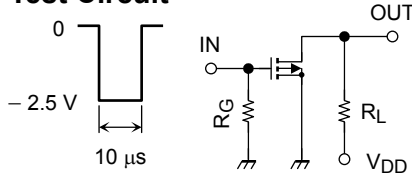


(c) V_{OUT}



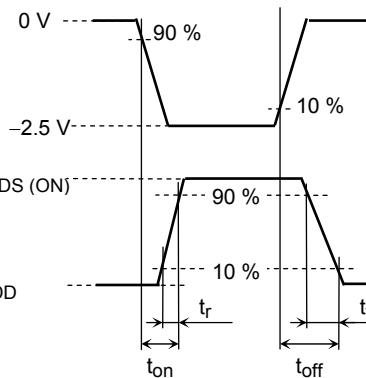
Q2 Switching Time Test Circuit

(a) Test Circuit

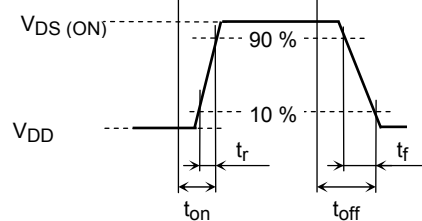


$V_{DD} = -10\text{ V}$
 $R_G = 4.7\ \Omega$
 Duty $\leq 1\%$
 V_{IN} : $t_r, t_f < 5\text{ ns}$
 Common Source
 $T_a = 25\text{ }^\circ\text{C}$

(b) V_{IN}



(c) V_{OUT}



Q1 Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = 1\text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} , and $V_{GS(OFF)}$ requires a lower voltage than V_{th} .

(The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

Take this into consideration when using the device.

Q2 Precaution

V_{th} can be expressed as the voltage between gate and source when the low operating current value is $I_D = -1\text{ mA}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires a higher voltage than V_{th} , and $V_{GS(OFF)}$ requires a lower voltage than V_{th} .

(The relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$.)

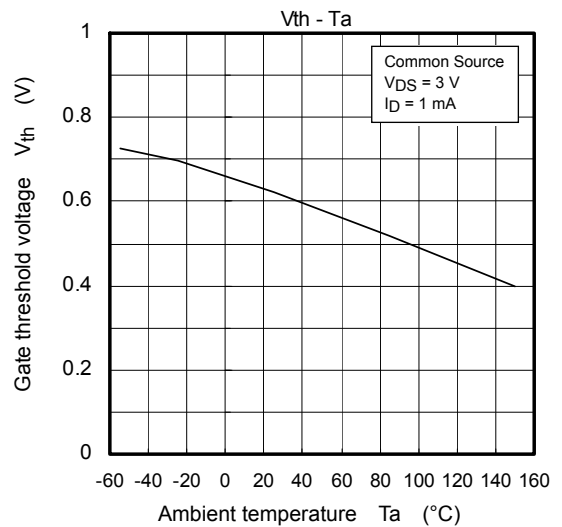
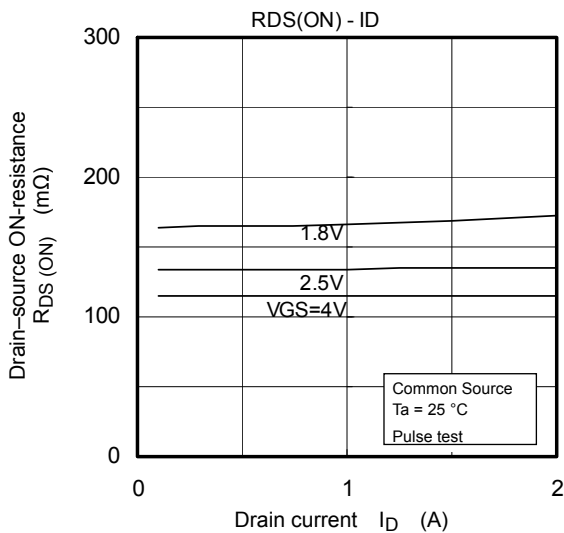
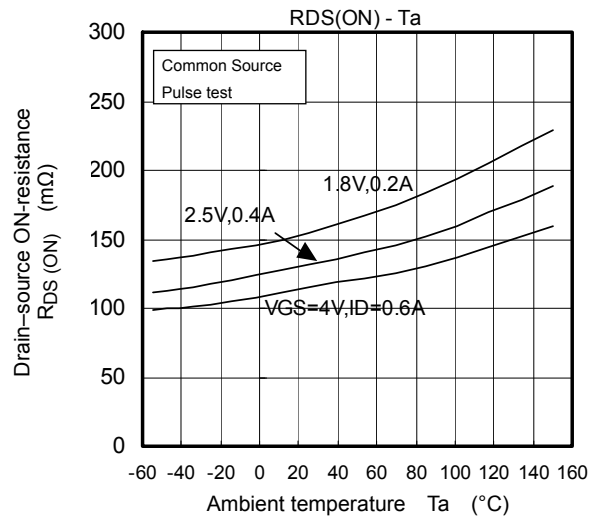
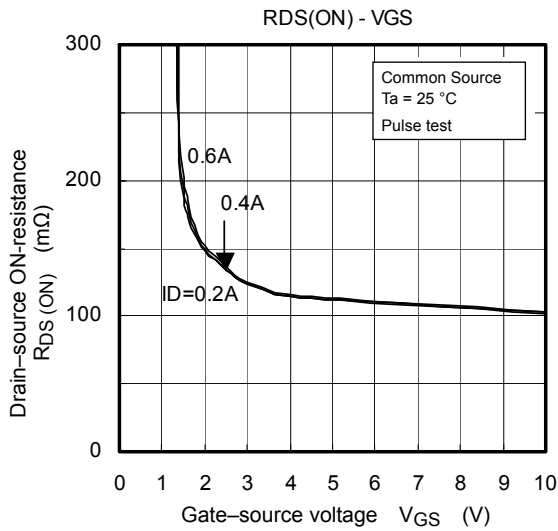
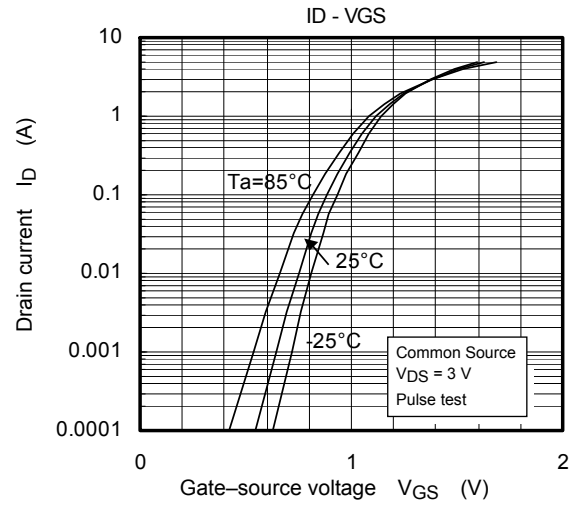
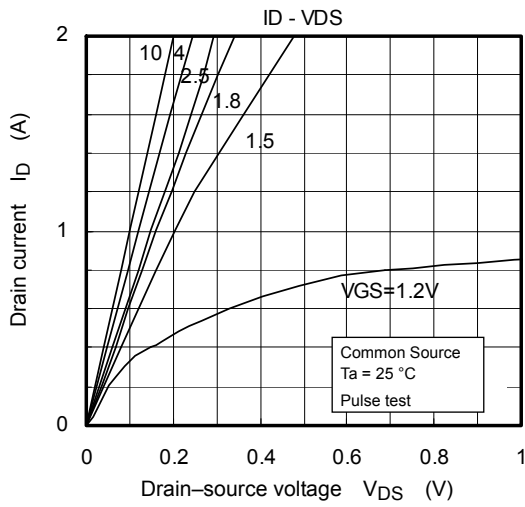
Take this into consideration when using the device.

Handling Precaution

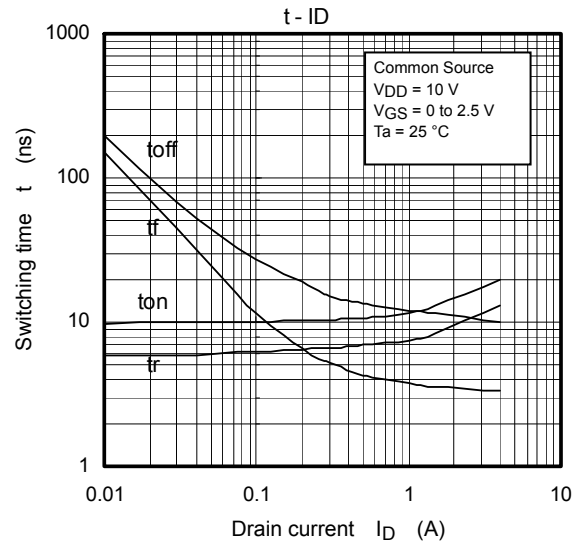
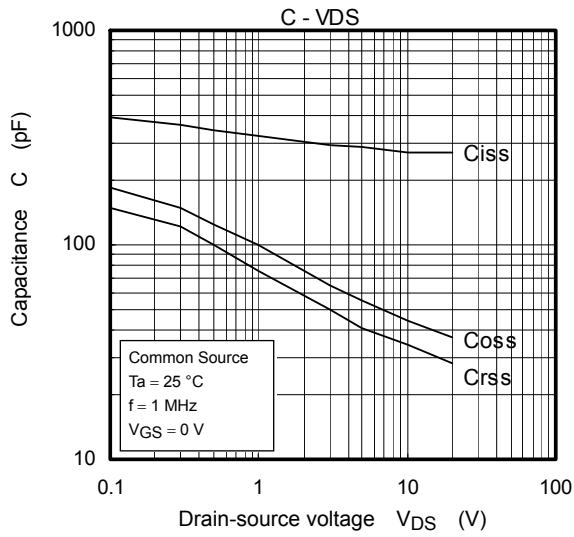
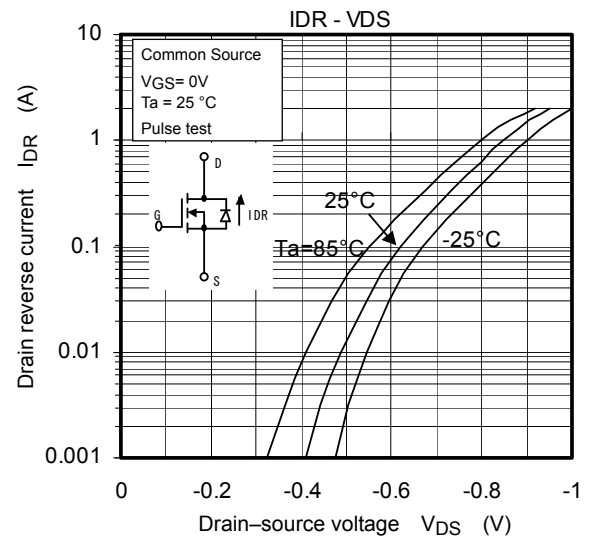
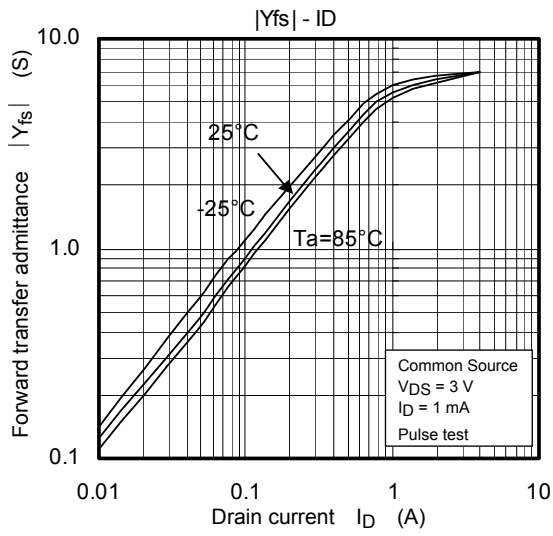
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance $R_{th(ch-a)}$ and Power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

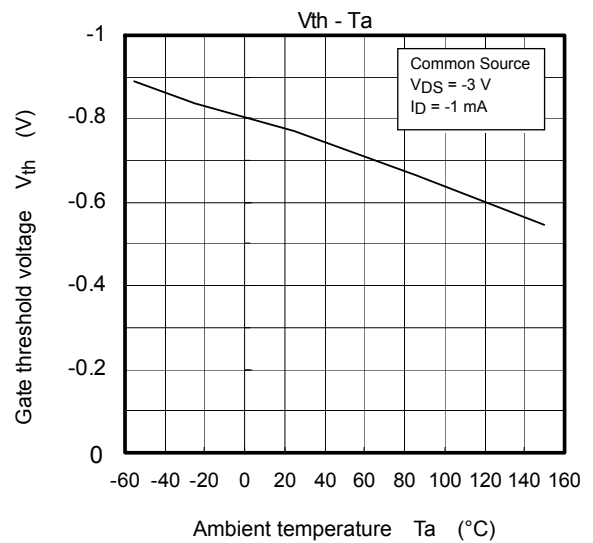
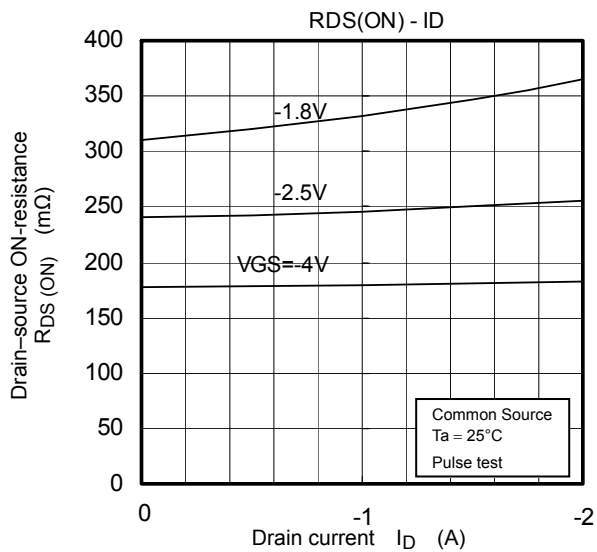
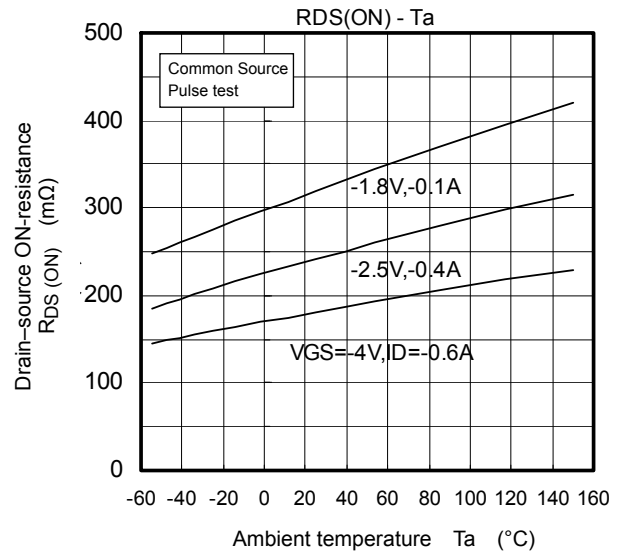
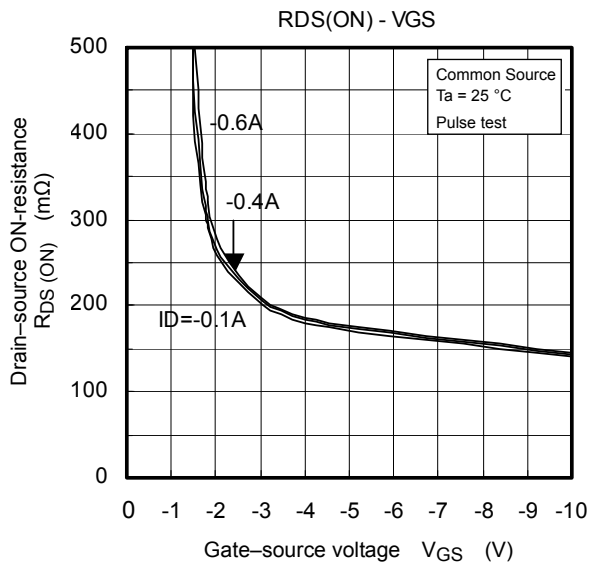
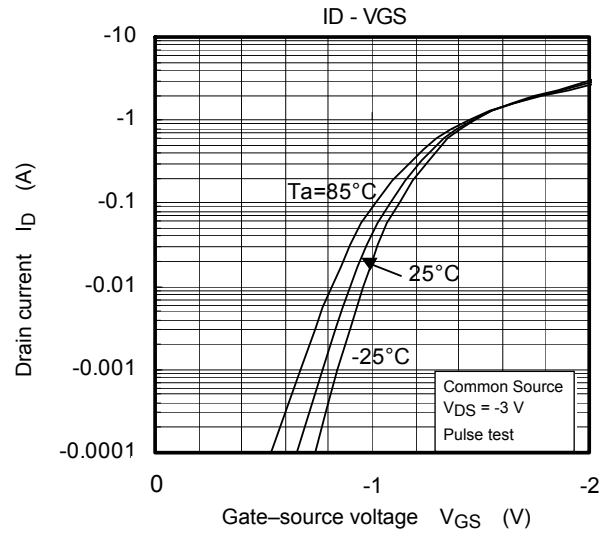
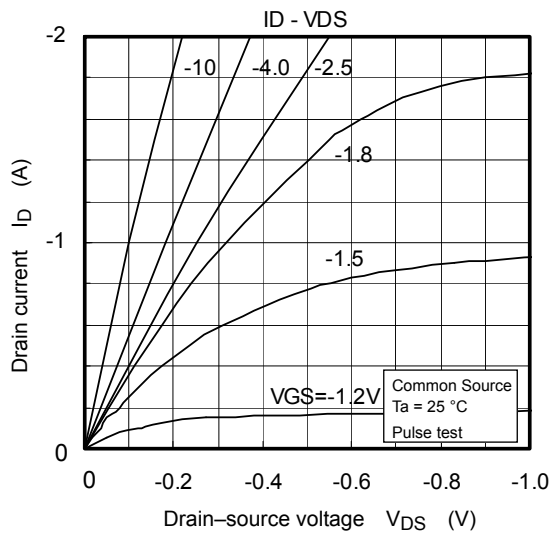
Q1 Data



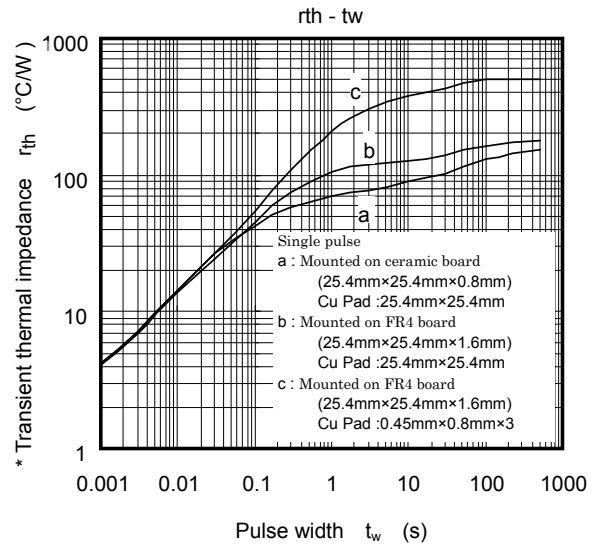
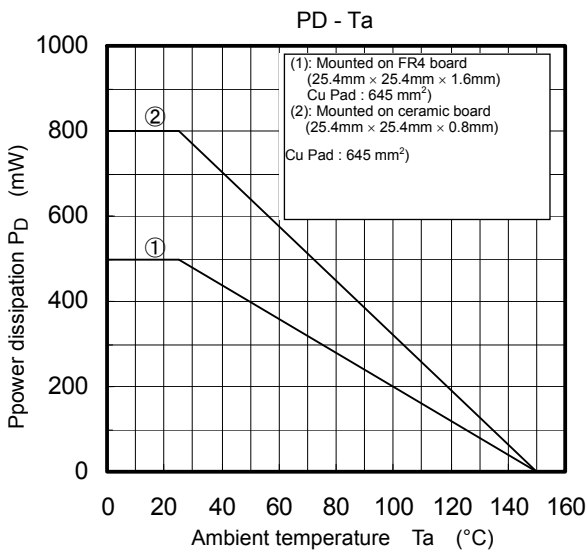
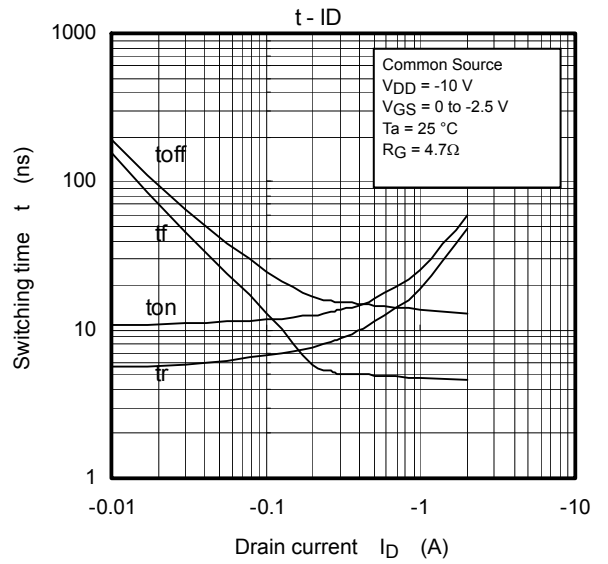
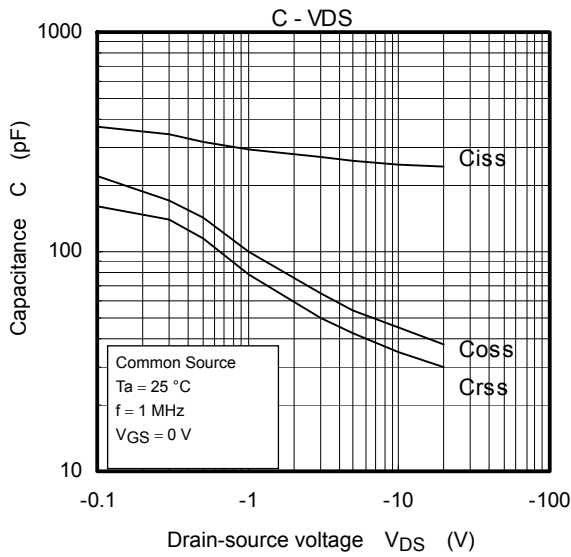
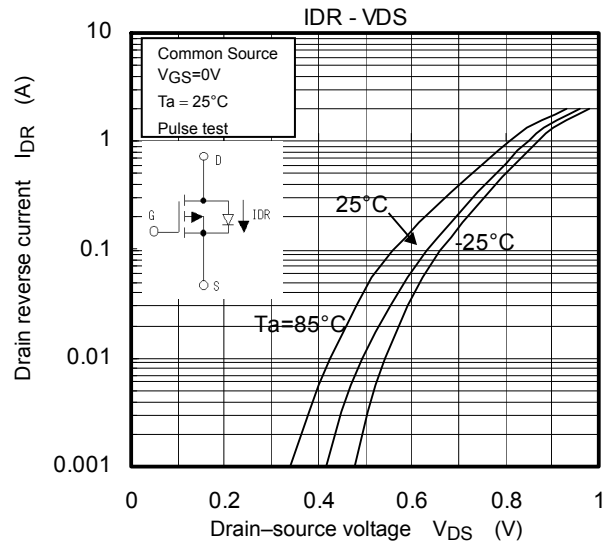
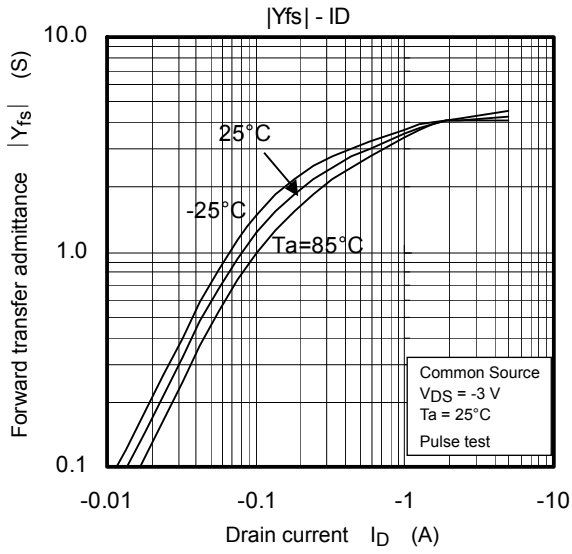
Q1 Data



Q2 Data



Q2 Data



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