

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSIII)

# SSM6K24FE

## High Speed Switching Applications

- Optimum for high-density mounting in small packages
- Low on-resistance:  $R_{on} = 145m\Omega$  (max) (@ $V_{GS} = 4.5 V$ )  
 $R_{on} = 180m\Omega$  (max) (@ $V_{GS} = 2.5 V$ )

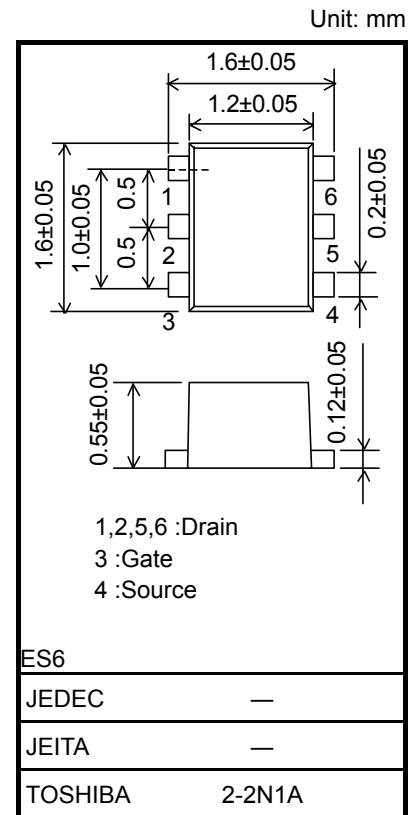
## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DS}$	30	V
Gate-Source voltage		$V_{GSS}$	$\pm 12$	V
Drain current	DC	$I_D$	0.5	A
	Pulse	$I_{DP}$	1.5	
Drain power dissipation		$P_D$ (Note 1)	500	mW
Channel temperature		$T_{ch}$	150	°C
Storage temperature range		$T_{stg}$	-55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

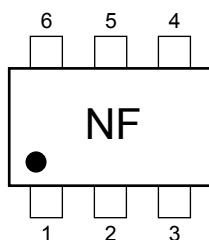
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Mounted on FR4 board.  
 (25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm<sup>2</sup>)

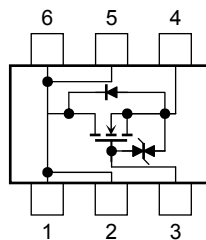


Weight: 3.0 mg (typ.)

## Marking



## Equivalent Circuit (top view)



## Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

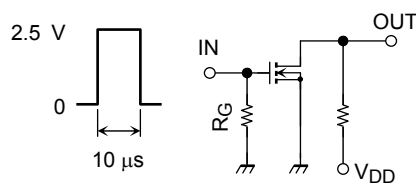
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1\text{ mA}, V_{GS} = 0$	30	—	—	V
	$V_{(BR)DSX}$	$I_D = 1\text{ mA}, V_{GS} = -12\text{ V}$	18	—	—	
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0$	—	—	1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.5	—	1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 0.25\text{ A}$ (Note2)	1.0	2.0	—	S
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = 0.50\text{ A}, V_{GS} = 4.5\text{ V}$ (Note2)	—	120	145	m $\Omega$
		$I_D = 0.25\text{ A}, V_{GS} = 2.5\text{ V}$ (Note2)	—	140	180	
Input capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	245	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	33	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	41	—	pF
Switching time	Turn-on time	$V_{DD} = 10\text{ V}, I_D = 0.25\text{ A},$ $V_{GS} = 0 \sim 2.5\text{ V}, R_G = 4.7\ \Omega$	—	9	—	ns
	Turn-off time		—	15	—	

Note2: Pulse test

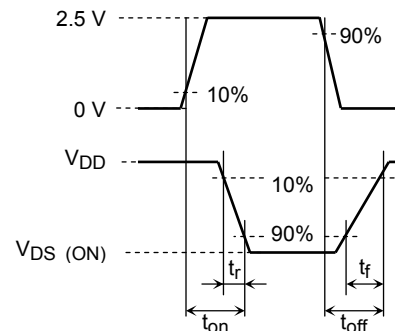
## Switching Time Test Circuit

### (a) Test Circuit



$V_{DD} = 10\text{ V}$   
 $R_G = 4.7\ \Omega$   
 D.U.  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

### (b) $V_{IN}$



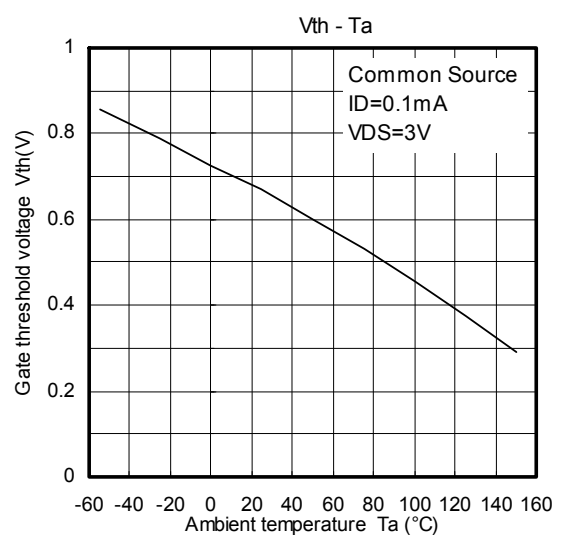
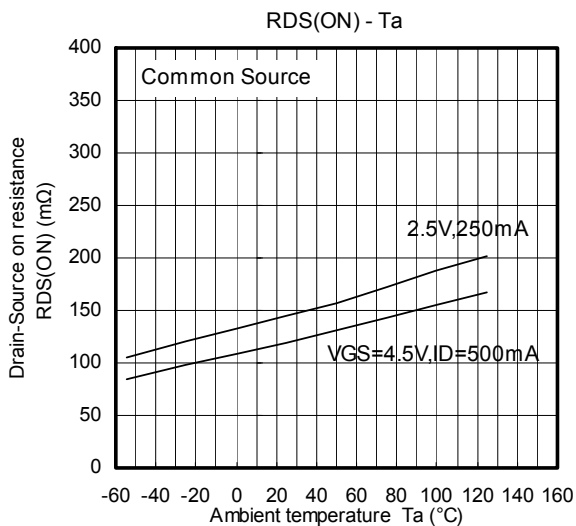
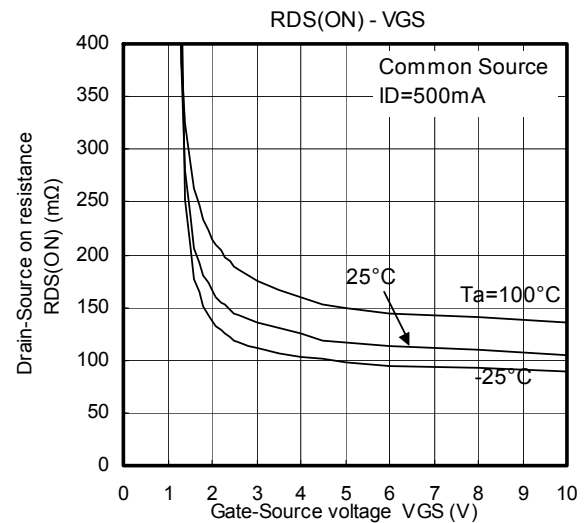
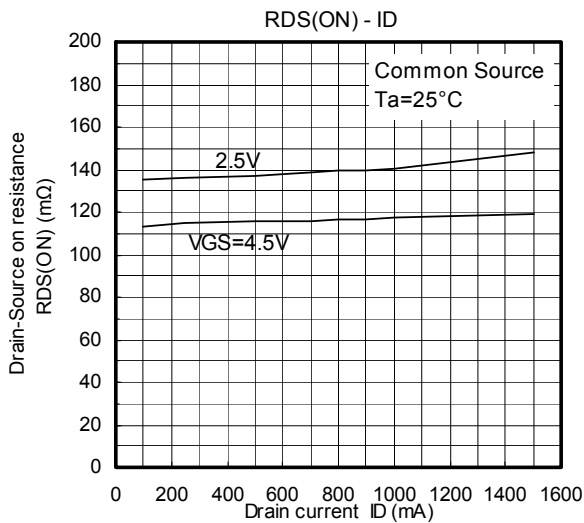
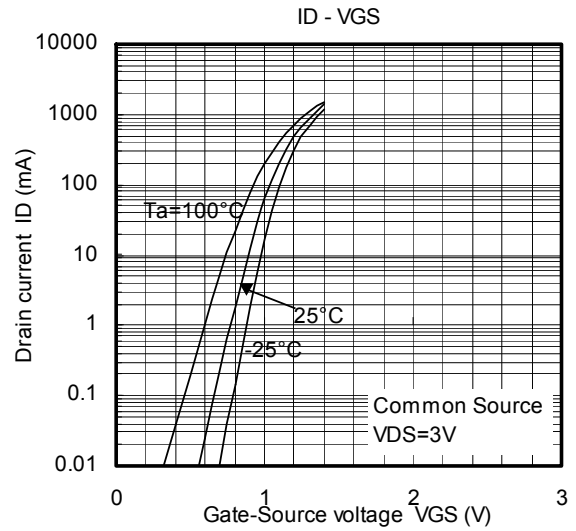
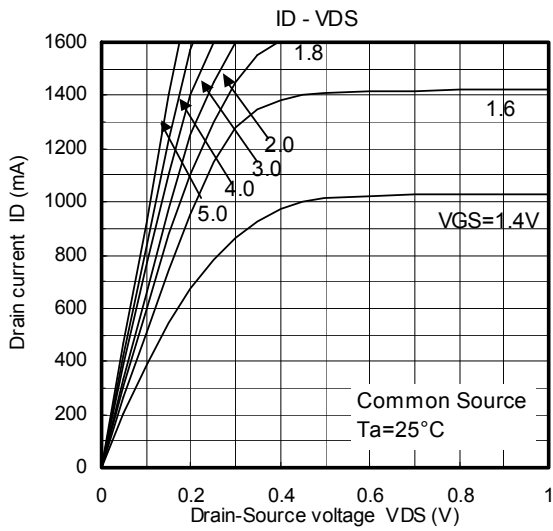
### (c) $V_{OUT}$

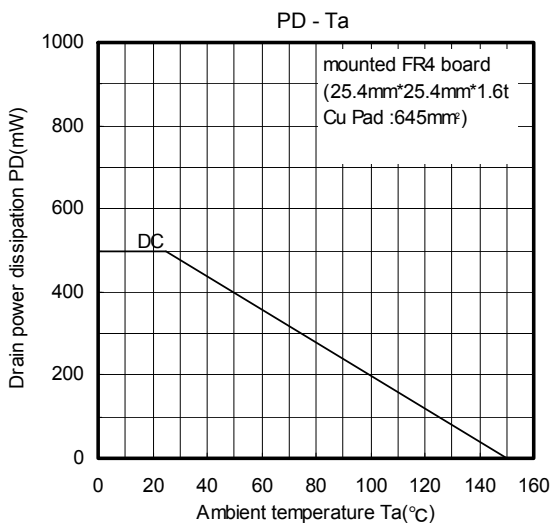
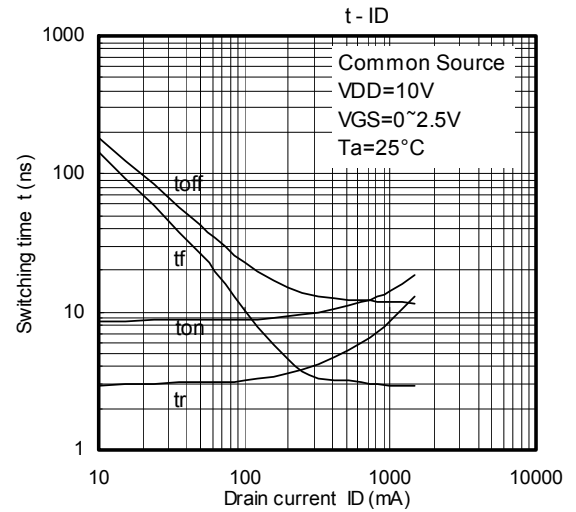
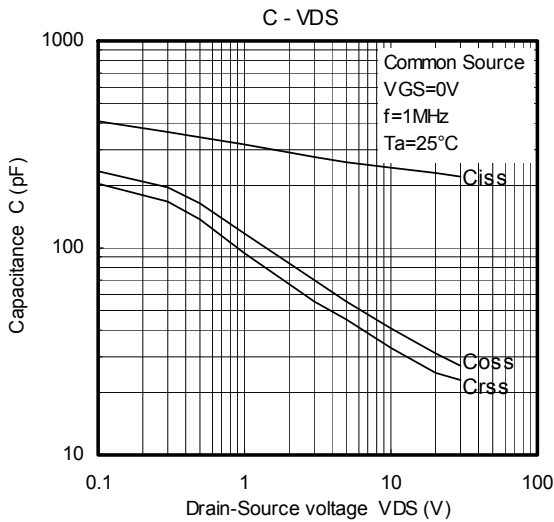
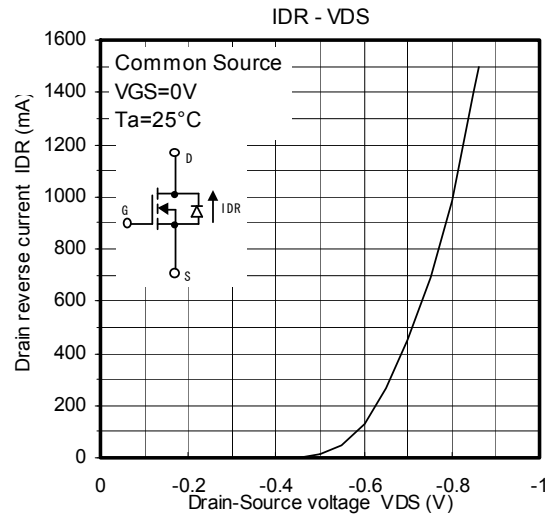
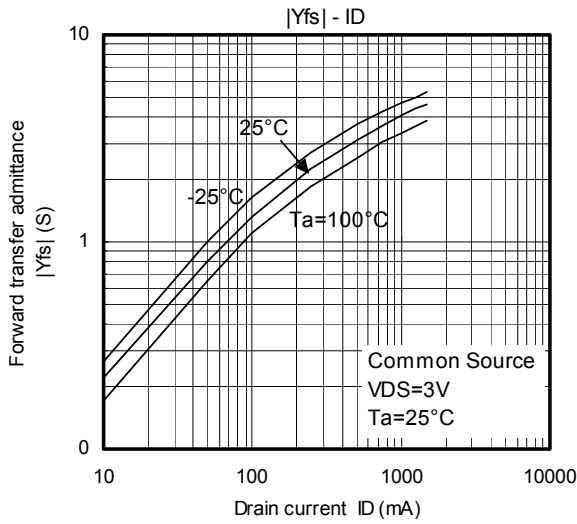
## Precaution

$V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D = 100\ \mu\text{A}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires a lower voltage than  $V_{th}$ .

(The relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ )

Please take this into consideration when using the device.





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