TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

# SSM6J412TU

## O Power Management Switch Applications

Unit: mm

• 1.5-V drive

• Low ON-resistance:  $R_{DS(ON)}$  = 99.6 m $\Omega$  (max) (@V<sub>GS</sub> = -1.5 V)

 $R_{DS(ON)} = 67.8 \text{ m}\Omega \text{ (max) (@V_{GS} = -1.8 V)}$ 

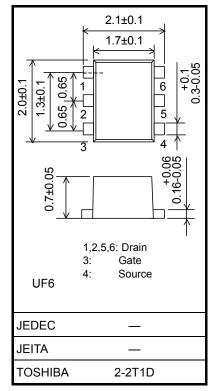
 $R_{DS(ON)} = 51.4 \text{ m}\Omega \text{ (max) (@V_{GS} = -2.5 V)}$ 

 $R_{DS(ON)} = 42.7 \text{ m}\Omega \text{ (max) (@V_{GS} = -4.5 V)}$ 

## **Absolute Maximum Ratings (Ta = 25°C)**

Characteristic		Symbol	Rating	Unit	
Drain-source voltage		$V_{DSS}$	-20	V	
Gate-source voltage		$V_{GSS}$	± 8	V	
Drain current	DC	ΙD	-4.0	А	
	Pulse	I <sub>DP</sub> (Note 1)	-16.0		
Power dissipation		P <sub>D</sub> (Note 2)	1	W	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



Weight: 7.0mg (typ.)

Please design the appropriate reliability upon reviewing the

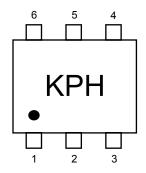
Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pw  $\leq$  10 $\mu$ s, Duty.  $\leq$  1%

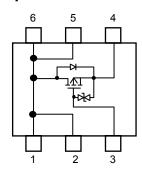
Note 2: Mounted on a FR4 board.

 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$ 

#### Marking (Top View)



## **Equivalent Circuit**



### **Electrical Characteristics (Ta = 25°C)**

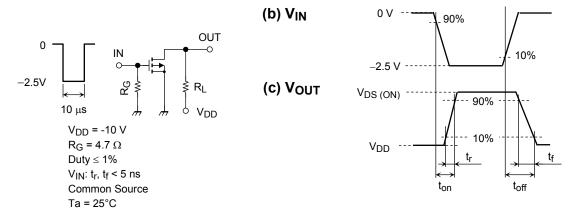
Chara	cteristic	Symbol	Test Conditions		Min	Тур.	Max	Unit
Drain source breakdown voltage	V <sub>(BR)DSS</sub>	$I_D = -1 \text{ mA}, V_{GS} = 0 \text{ V}$		-20	_	_	٧	
Drain-source breakdown voltage		V (BR) DSX	I <sub>D</sub> = -1 mA, V <sub>GS</sub> = 5 V	(Note 4)	-15	_	_	V
Drain cut-off curre	nt	I <sub>DSS</sub>	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V		_	_	-1	μΑ
Gate leakage curre	ent	I <sub>GSS</sub>	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	±1	μΑ
Gate threshold vol	tage	V <sub>th</sub>	$V_{DS} = -3 \text{ V}, I_{D} = -1 \text{ mA}$		-0.3	_	-1.0	V
Forward transfer a	dmittance	Y <sub>fs</sub>	V <sub>DS</sub> = -3 V, I <sub>D</sub> = -1.0 A	(Note 3)	4.5	9.1	_	S
Drain-source ON-resistance	R <sub>DS</sub> (ON)	I <sub>D</sub> = -3.0 A, V <sub>GS</sub> = -4.5 V	(Note 3)	_	36.9	42.7	mΩ	
		I <sub>D</sub> = -2.5 A, V <sub>GS</sub> = -2.5 V	(Note 3)	_	42.8	51.4		
		I <sub>D</sub> = -1.5 A, V <sub>GS</sub> = -1.8 V	(Note 3)	_	50.6	67.8		
		I <sub>D</sub> = -0.5 A, V <sub>GS</sub> = -1.5 V	(Note 3)	_	58.6	99.6		
Input capacitance		C <sub>iss</sub>	V 40.V.V 0.V		_	840	_	
Output capacitance		Coss	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$		_	118	_	pF
Reverse transfer capacitance		C <sub>rss</sub>	11 - 1 WITZ		_	99	_	
Switching time	Turn-on time	ton	$V_{DD}$ = -10 V, $I_{D}$ = -2.0 A $V_{GS}$ = 0 to -2.5 V, $R_{G}$ = 4.7 $\Omega$		_	32	_	20
	Turn-off time	t <sub>off</sub>			_	107	—	ns
Total gate charge		Qg	V 10 V I 4 0 A		_	12.8	—	
Gate-source charge		Q <sub>gs1</sub>	$V_{DD} = -10 \text{ V}, I_D = -4.0 \text{ A},$ $V_{GS} = -4.5 \text{ V}$		_	1.4	_	nC
Gate-drain charge		Q <sub>gd</sub>	v GS4.5 v		_	3.0	_	
Drain-source forward voltage		V <sub>DSF</sub>	I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 0 V	(Note 3)	_	0.88	1.2	V

Note 3: Pulse test

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

## **Switching Time Test Circuit**

#### (a) Test Circuit



## **Notice on Usage**

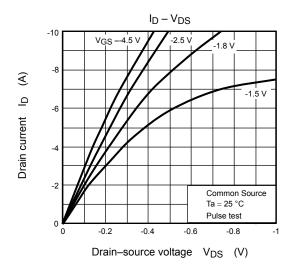
 $V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D$  = -1 mA for this product. For normal switching operation,  $V_{GS}$  (on) requires a higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires a lower voltage than  $V_{th}$ . (The relationship can be established as follows:  $V_{GS}$  (off) <  $V_{th}$  <  $V_{GS}$  (on).)

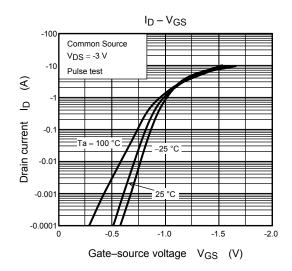
Take this into consideration when using the device.

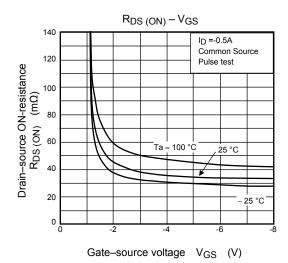
#### **Handling Precaution**

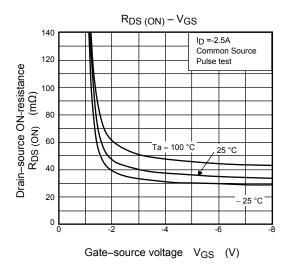
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

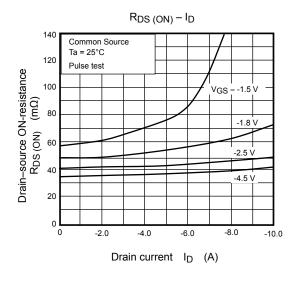
Thermal resistance  $R_{th (ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

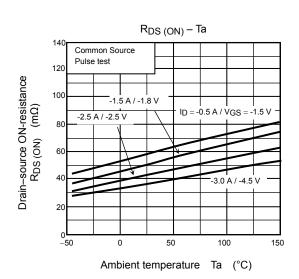


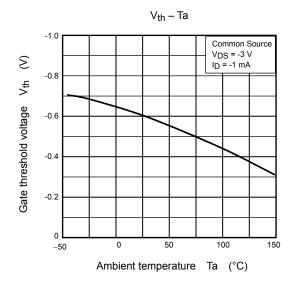


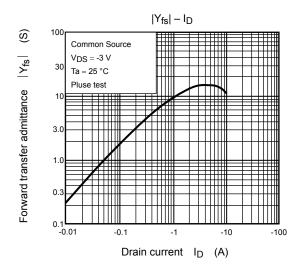


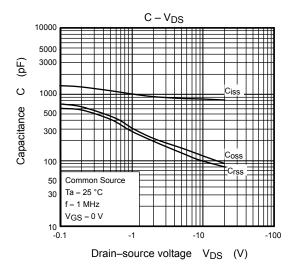


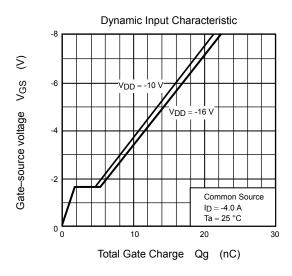


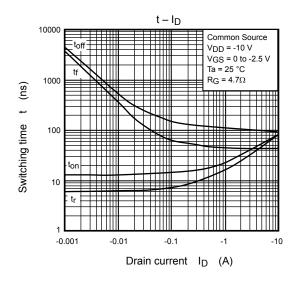


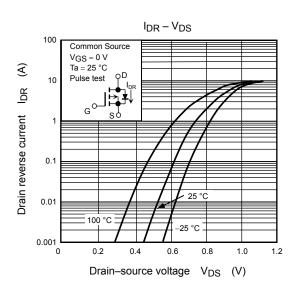


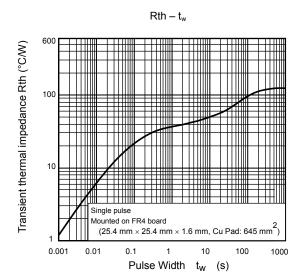


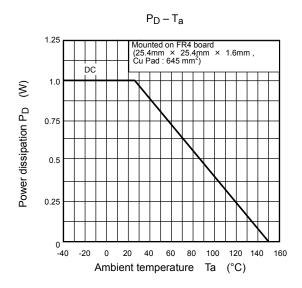












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