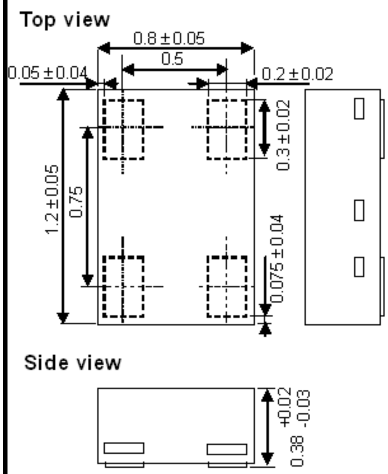
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSⅢ)

SSM4K27CT

○ Switching Applications

Unit: mm

- Small package
- Low on-resistance: $R_{DS(ON)}$ = 205 mΩ (max) (@V_{GS} = 4.0 V)
  $R_{DS(ON)}$ = 260 mΩ (max) (@V_{GS} = 2.5 V)
  $R_{DS(ON)}$ = 390 mΩ (max) (@V_{GS} = 1.8 V)



CST4

JEDEC	―
JEITA	―
TOSHIBA	2-1M1A

Weight: 1.1 mg (typ.)

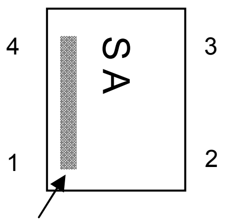
Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	20	V
Gate-Source voltage		V_{GSS}	±12	V
Drain current	DC	I_D	0.5	A
	Pulse	I_{DP}	1.0	
Power dissipation		P_D (Note 1)	400	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

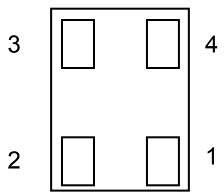
Note 1: Mounted on FR4 board.
(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm^2)

Marking (top view)



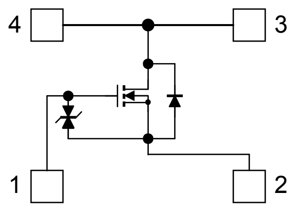
Polarity marking

Electrode Layout (bottom view)



1 Gate
2 Source
3 Drain
4 Drain

Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

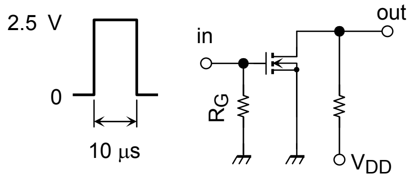
Electrical Characteristics (Ta=25°C)

Characteristics		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0	–	–	±1	μA
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = 1 mA, V_{GS} = 0	20	–	–	V
		$V_{(BR)DSX}$	I_D = 1 mA, V_{GS} = -12 V	10	–	–	
Drain cut-off current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	–	–	10	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.5	–	1.1	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 0.25 A (Note2)	0.8	1.6	–	S
Drain-Source on-resistance		$R_{DS(ON)}$	I_D = 0.25 A, V_{GS} = 4 V (Note2)	—	175	205	mΩ
			I_D = 0.25 A, V_{GS} = 2.5 V (Note2)	—	200	260	
			I_D = 0.10 A, V_{GS} = 1.8 V (Note2)	—	250	390	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	–	174	–	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	–	25	–	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0, f = 1 MHz	–	31	–	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 0.25 A,	–	10	–	ns
	Turn-off time	t_{off}	V_{GS} = 0~2.5 V, R_G = 4.7 Ω	–	12	–	

Note2: Pulse test

Switching Time Test Circuit

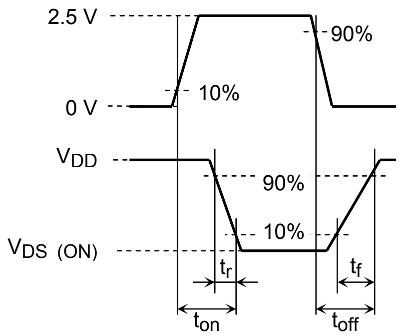
(a) Test Circuit



V_{DD} = 10 V
R_G = 4.7 Ω
Duty ≦ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

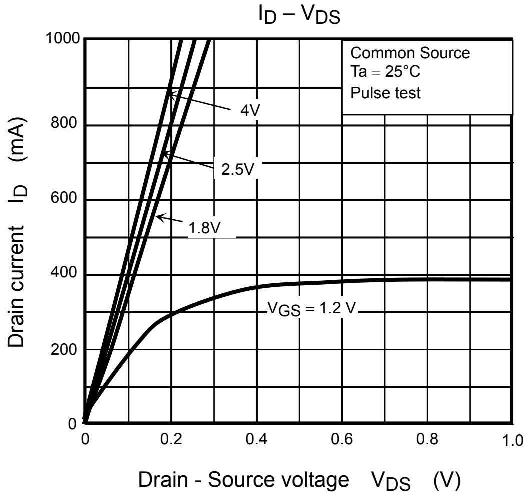
(c) V_{OUT}

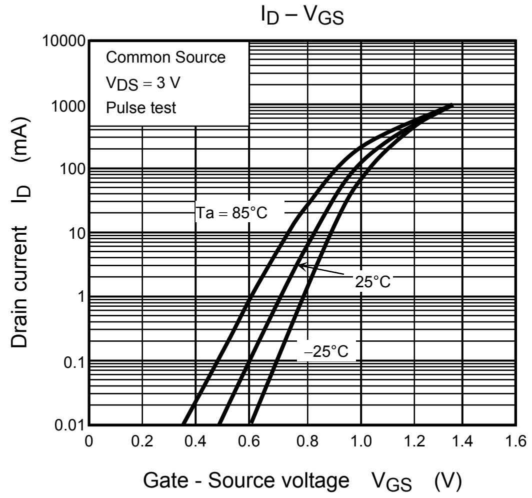


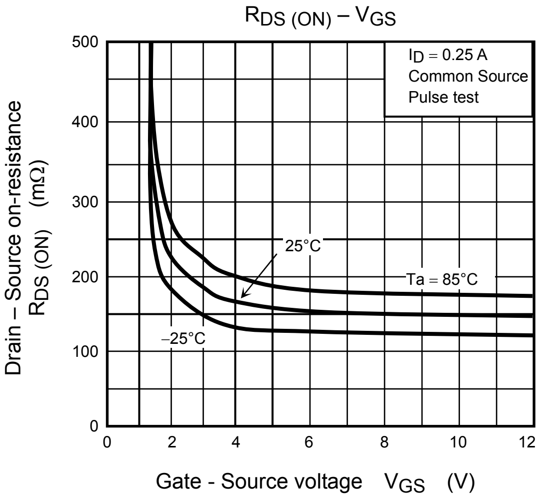
Precaution

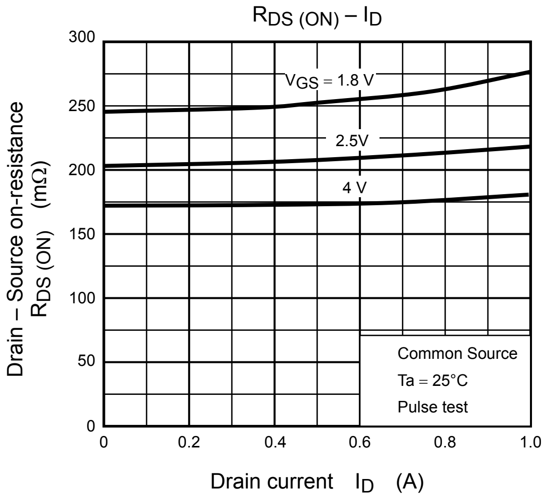
V_{th} can be expressed as the voltage between the gate and source when the low operating current value is I_D = 1 mA for this product. For normal switching operation, $V_{GS(on)}$ requires a higher voltage than V_{th} and $V_{GS(off)}$ requires a lower voltage than V_{th}. (The relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$.)

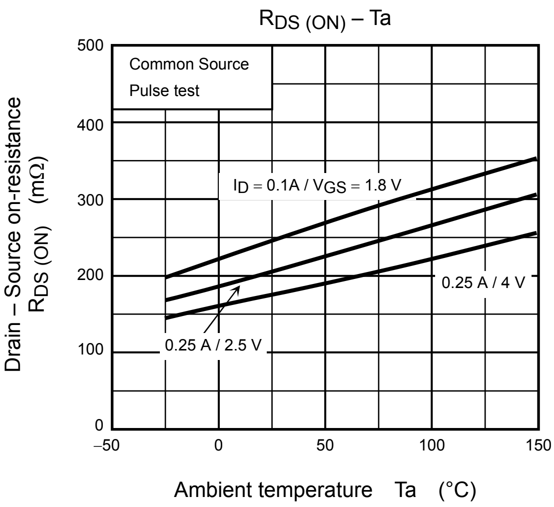
Be sure to take this into consideration when using the device.

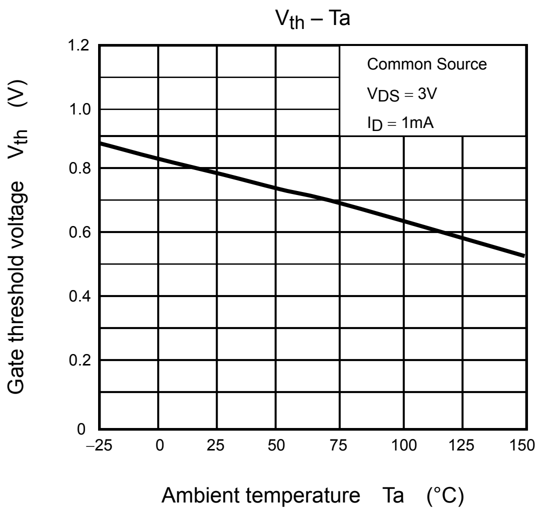

ID – VDS
Common Source
Ta = 25°C
Pulse test
4V
2.5V
1.8V
VGS = 1.2 V
Drain current ID (mA)
Drain - Source voltage VDS (V)

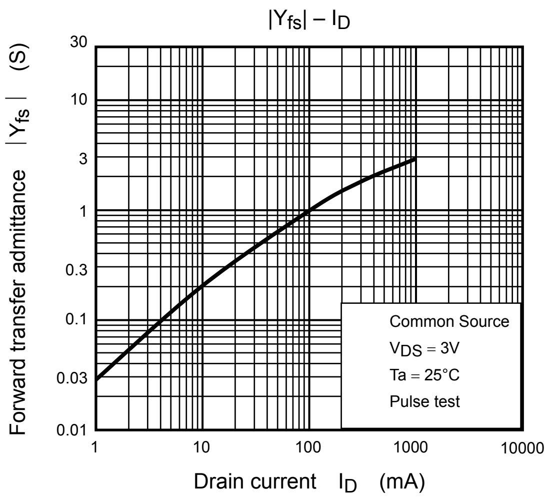

ID – VGS
Common Source
VDS = 3 V
Pulse test
Ta = 85°C
25°C
–25°C
Drain current ID (mA)
Gate - Source voltage VGS (V)

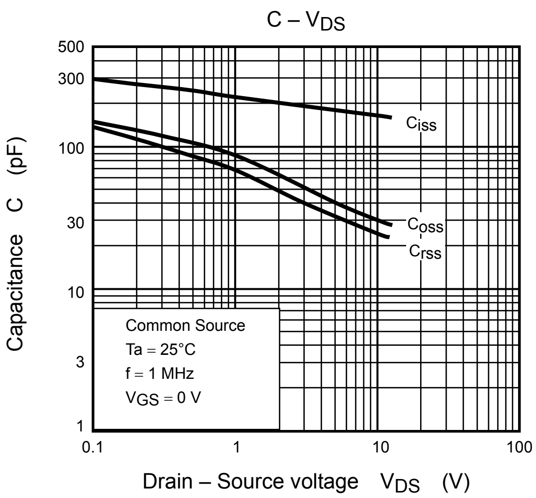

RDS (ON) – VGS
ID = 0.25 A
Common Source
Pulse test
25°C
Ta = 85°C
–25°C
Drain – Source on-resistance RDS (ON) (mΩ)
Gate - Source voltage VGS (V)

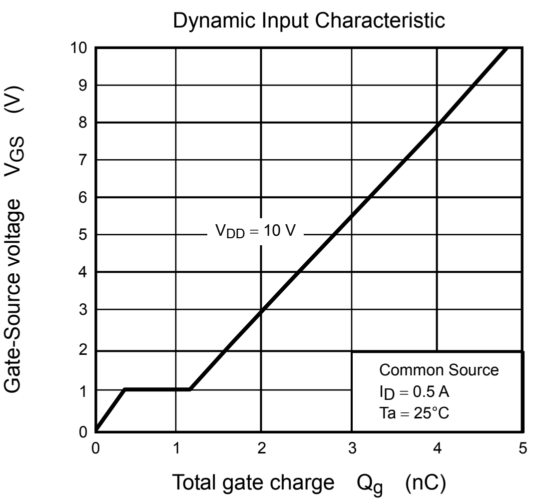

RDS (ON) – ID
VGS = 1.8 V
2.5V
4 V
Common Source
Ta = 25°C
Pulse test
Drain – Source on-resistance RDS (ON) (mΩ)
Drain current ID (A)

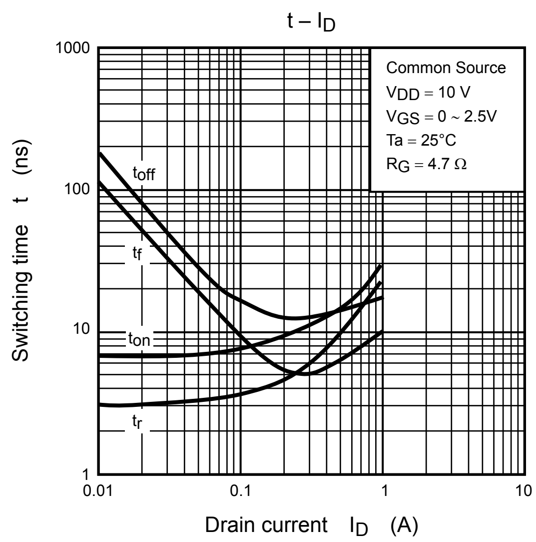

RDS (ON) – Ta
Common Source
Pulse test
ID = 0.1A / VGS = 1.8 V
0.25 A / 4 V
0.25 A / 2.5 V
Drain – Source on-resistance RDS (ON) (mΩ)
Ambient temperature Ta (°C)

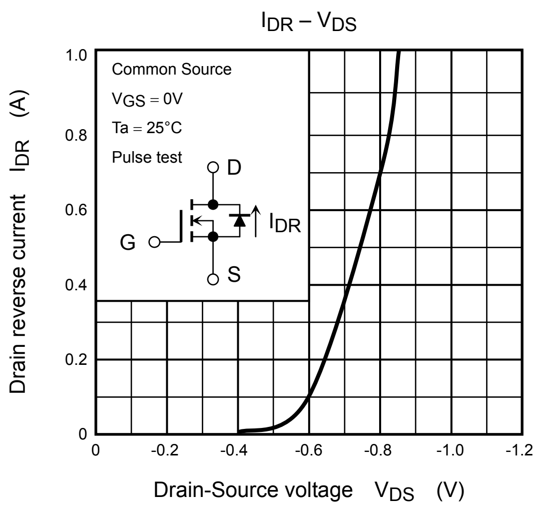

Vth – Ta
Common Source
VDS = 3V
ID = 1mA
Gate threshold voltage Vth (V)
Ambient temperature Ta (°C)

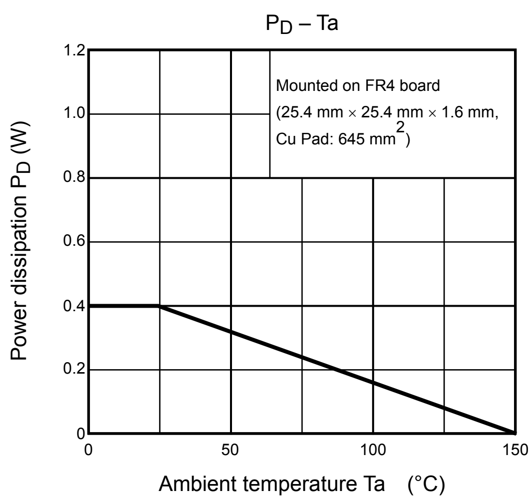

|Yfs| – ID
Forward transfer admittance |Yfs| (S)
Drain current ID (mA)
Common Source
VDS = 3V
Ta = 25°C
Pulse test


C – VDS
Capacitance C (pF)
Drain – Source voltage VDS (V)
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V


Dynamic Input Characteristic
Gate-Source voltage VGS (V)
Total gate charge Qg (nC)
VDD = 10 V
Common Source
ID = 0.5 A
Ta = 25°C


t – ID
Switching time t (ns)
Drain current ID (A)
Common Source
VDD = 10 V
VGS = 0 ~ 2.5V
Ta = 25°C
RG = 4.7 Ω
toff
tf
ton
tr


IDR – VDS
Drain reverse current IDR (A)
Drain-Source voltage VDS (V)
Common Source
VGS = 0V
Ta = 25°C
Pulse test
D
G
S
IDR


PD – Ta
Power dissipation PD (W)
Ambient temperature Ta (°C)
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 mm,
Cu Pad: 645 mm2)

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