

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCT9541AFT, TC74VHCT9541AFK

Octal Universal Schmitt Buffer with 3-State Outputs

The TC74VHCT9541A is an ultra-high-speed octal Schmitt buffer fabricated using silicon-gate CMOS technology. The TC74VHCT9541A combines low power consumption of CMOS with Schottky TTL speeds.

The input voltage are compatible with TTL output voltage.

This device may be used as a level converter for interfacing 3.3 V to 5 V system.

The outputs can be put in the high-impedance state by placing a logic HIGH on the Enable (\overline{G}) input. The CONT input determines the logical inversion of data. A logic LOW on the CONT input configures the TC74VHCT9541A as an inverter; a logic HIGH on the CONT input configures the TC74VHCT9541A as a buffer.

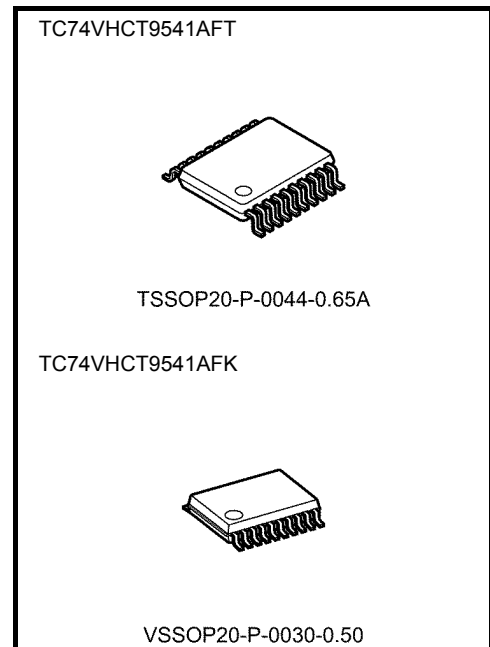
All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCT9541A is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output (Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state

Features

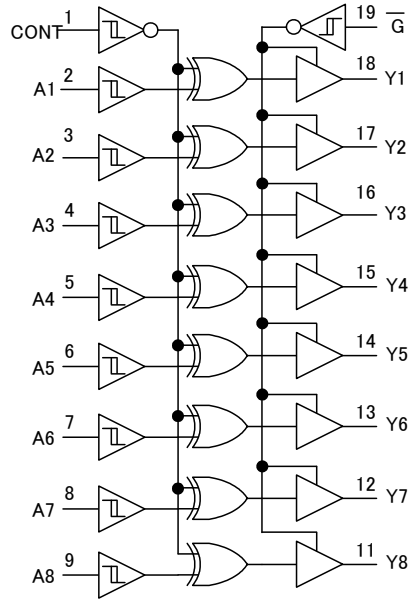
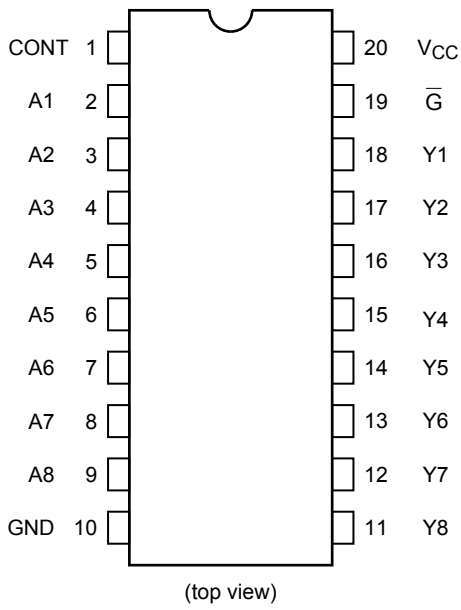
- High speed: $t_{pd} = 6.5\text{ns}$ (typ.) at $V_{CC} = 5\text{V}$
- Low power dissipation: $I_{CC} = 4\ \mu\text{A}$ (max) at $T_a = 25^\circ\text{C}$
- Compatible with TTL inputs
 - $V_{IL} = 0.5\text{V}$ (max)
 - $V_{IH} = 2.1\text{V}$ (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Input terminals are at the opposite side of Output terminals



Weight

TSSOP20-P-0044-0.65A : 0.08 g (typ.)
 VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Pin Assignment



Truth Table

Inputs			Outputs
\overline{G}	CONT	A _n	Y _n
H	X	X	Z
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to 7.0 (Note 2)	V
		-0.5 to $V_{CC} + 0.5$ (Note 3)	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20 (Note 4)	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to 5.5 (Note 2)	V
		0 to V_{CC} (Note 3)	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in off-state

Note 3: High or low state.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit	
				V _{CC} (V)	Min	Typ	Max	Min		Max
Positive threshold voltage	V _P	—		4.5	—	—	1.90	—	1.90	V
				5.5	—	—	2.10	—	2.10	
Negative threshold voltage	V _N	—		4.5	0.50	—	—	0.50	—	V
				5.5	0.60	—	—	0.60	—	
Hysteresis voltage	V _H	—		4.5	0.40	—	1.40	0.40	1.40	V
				5.5	0.40	—	1.50	0.40	1.50	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	4.5	4.4	4.5	—	4.4	—	V
			I _{OH} = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	4.5	—	0.0	0.1	—	0.1	V
			I _{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.25	—	±2.5	μA
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I _{CC(T)}	Per input: V _{IN} = 3.4 V Other input: V _{CC} or GND		5.5	—	—	1.35	—	1.50	mA
Output leakage current	I _{OPD}	V _{OUT} = 5.5 V		0	—	—	0.5	—	5.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (An-Yn)	t _{pLH}	—	5.0 ± 0.5	15	—	6.5	8.5	1.0	10.0	ns
	t _{pHL}			50	—	8.6	11.5	1.0	13.0	
Propagation delay time (CONT-Yn)	t _{pLH}	—	5.0 ± 0.5	15	—	8.2	10.5	1.0	12.0	ns
	t _{pHL}			50	—	10.8	14.5	1.0	17.0	
3-state output enable time	t _{pZL}	R _L = 1 kΩ	5.0 ± 0.5	15	—	6.9	8.5	1.0	10.0	ns
	t _{pZH}			50	—	9.1	12.5	1.0	14.5	
3-state output disable time	t _{pLZ} t _{pHZ}	R _L = 1 kΩ	5.0 ± 0.5	50	—	7.4	11.5	1.0	13.0	ns
Output to output skew	t _{osHL} t _{osLH}	(Note 1)	5.0 ± 0.5	50	—	—	1.0	—	1.0	ns
Input capacitance	C _{IN}	—	—	—	—	4	10	—	10	pF
Output capacitance	C _{OUT}	—	—	—	—	9	—	—	—	pF
Power dissipation capacitance (Note 2)	C _{PD}	f _{IN} = 1 MHz	—	—	—	16	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

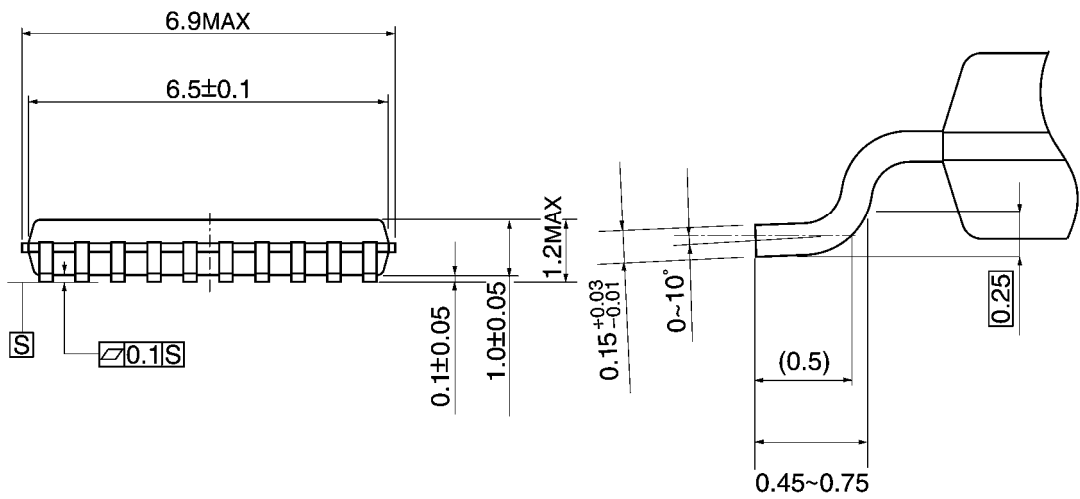
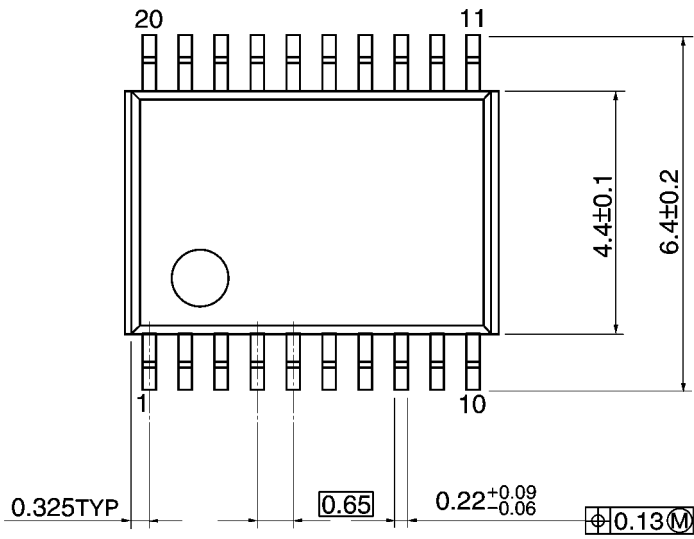
Noise Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Unit	
			V _{CC} (V)	Typ.		Limit
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	1.0	1.5	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.3	-1.5	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	2.1	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	0.5	V

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

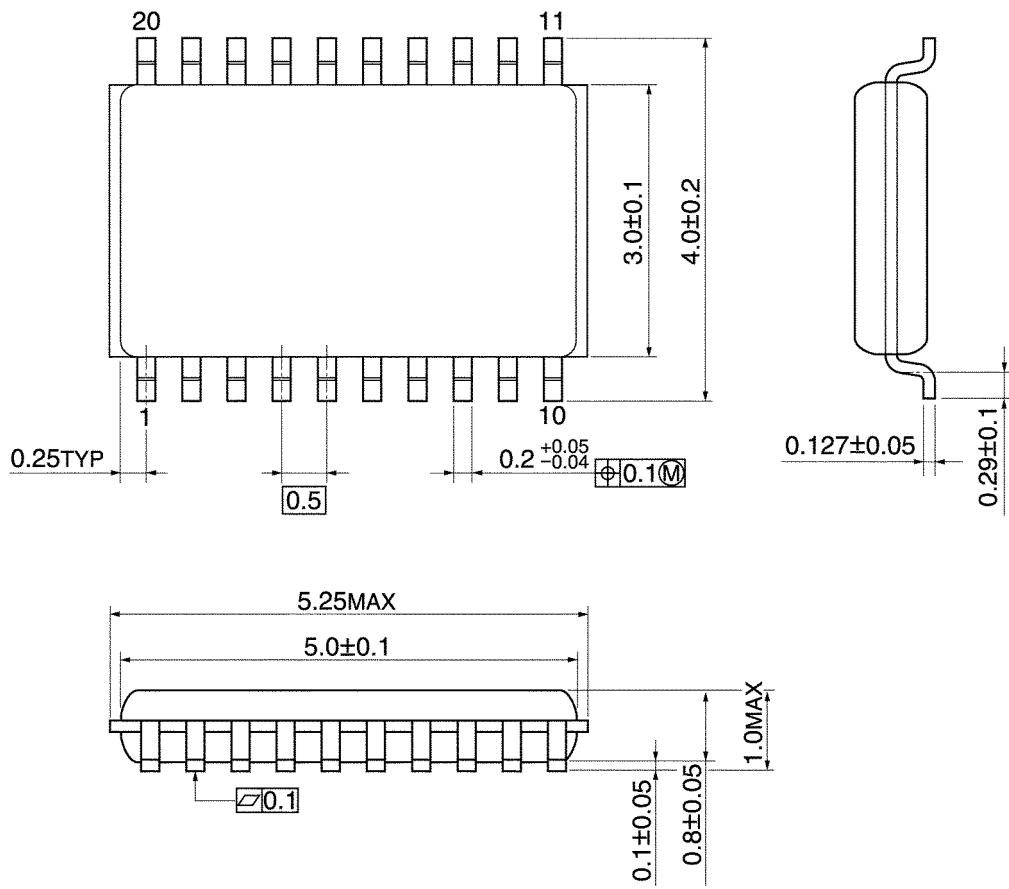


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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