TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC9595FT,TC74VHC9595FK

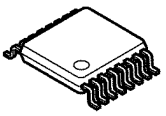
8-Bit Shift Register/Latch

The TC74VHC9595 is an advanced high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C^2MOS technology.
TC74VHC9595 combines low power consumption of CMOS with Schottky TTL speeds.
Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation.
This register can be used in serial-to-parallel conversion, data receivers, etc.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9595 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

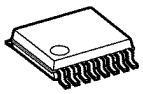
Additionally, all the inputs have a newly developed protection circuit without a diode returned to VCC. This enables the inputs to be tolerant of up to 5.5 volts even when power supply is down. The input power-down protection capability makes the TC74VHC9595 ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.
A variant of the TC 74HC/VHC/AHC/LV595, the TC74VHC9595 contains negative-edge-triggered flip-flops to improve timing margins that are affected by long wires or slowly changing clocks when multiple parts are cascaded together.

TC74VHC9595FT



TSSOP16-P-0044-0.65A

TC74VHC9595FK



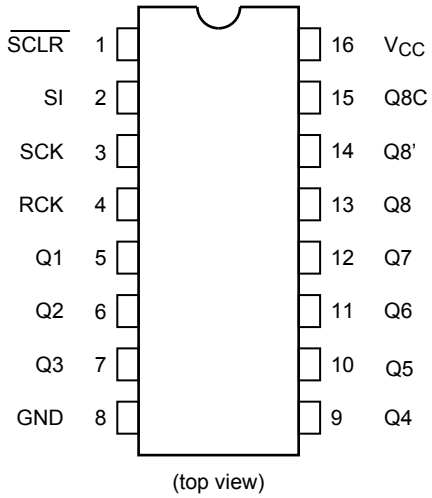
VSSOP16-P-0030-0.50

Weight
TSSOP16-P-0044-0.65A : 0.06 g (typ.)
VSSOP16-P-0030-0.50 : 0.02 g (typ.)

Features

- High speed: f_{max} = 224MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 V to 5.5 V

Pin Assignment



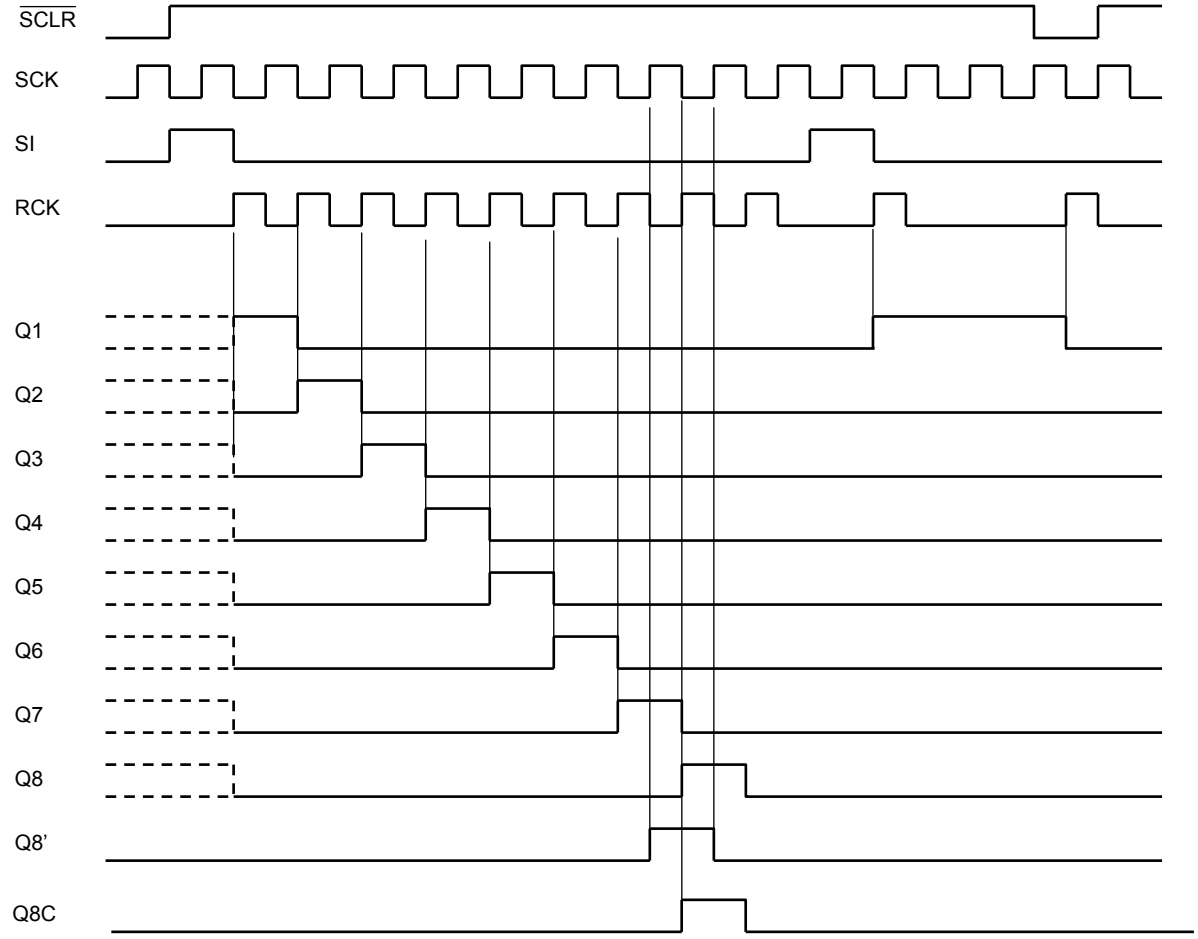
(top view)

Truth Table

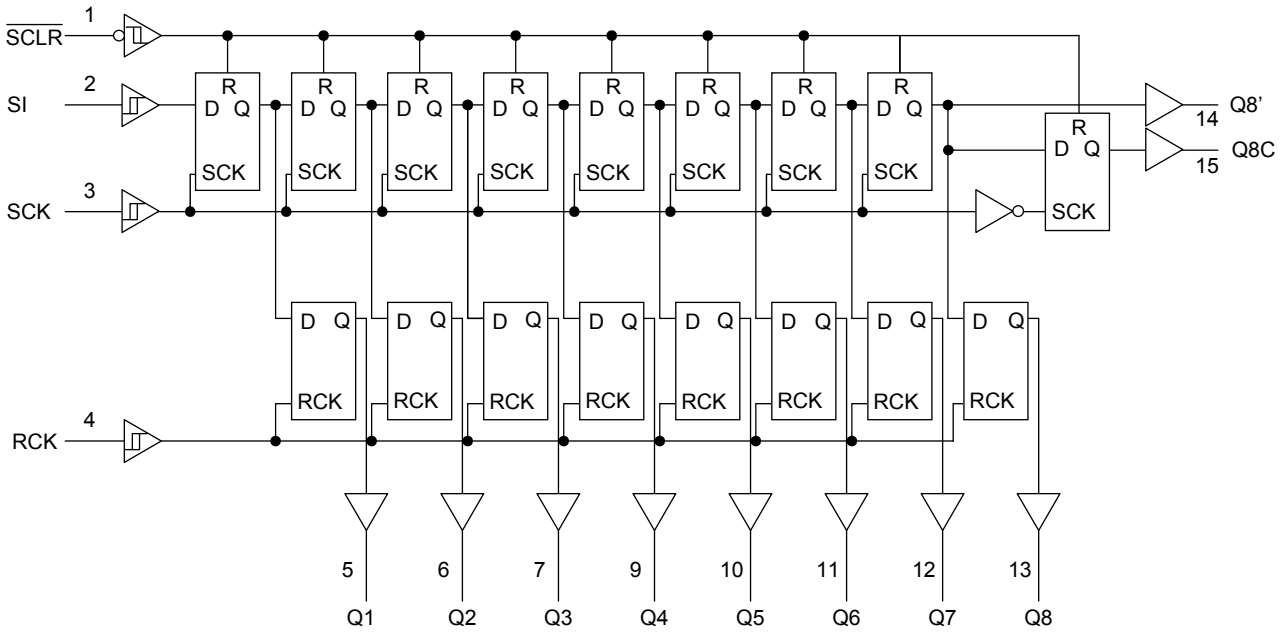
Inputs				Function
$\overline{SCLR}$	SI	SCK	RCK	
L	X	X	X	Shift register is cleared.
H	L	↑	X	First stage of S.R. becomes “L”. Other stages store the data of previous stage, respectively.
H	H	↑	X	First stage of S.R. becomes “H”. Other stages store the data of previous stage, respectively.
H	X	↓	X	Shift register is not changed. Q8C outputs store the data of previous stage, respectively.
H	X	X	↑	S.R. data is stored into storage register.
X	X	X	↓	Storage register stage is not changed.

X: Don’t care

Timing Chart



System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
Positive threshold voltage	V_P	—		3.0	—	—	2.20	—	2.20	V
				4.5	—	—	3.15	—	3.15	
				5.5	—	—	3.85	—	3.85	
Negative threshold voltage	V_N	—		3.0	0.90	—	—	0.90	—	V
				4.5	1.35	—	—	1.35	—	
				5.5	1.65	—	—	1.65	—	
Hysteresis voltage	V_H	—		3.0	0.30	—	1.20	0.30	1.20	V
				4.5	0.40	—	1.40	0.40	1.40	
				5.5	0.50	—	1.60	0.50	1.60	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4 mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8 mA	4.5	—	—	0.36	—	0.44	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (SCK, RCK)	$t_{w\,(H)}$	—	3.3 ± 0.3	—	5.0	5.0	ns
	$t_{w\,(L)}$		5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width ($\overline{SCLR}$)	$t_{w\,(L)}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time (SI-SCK)	t_s	—	3.3 ± 0.3	—	5.0	5.5	ns
			5.0 ± 0.5	—	3.5	3.5	
Minimum set-up time (SCK-RCK)	t_s	—	3.3 ± 0.3	—	8.0	8.5	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time ($\overline{SCLR}$-RCK)	t_s	—	3.3 ± 0.3	—	8.0	9.0	ns
			5.0 ± 0.5	—	5.5	6.5	
Minimum hold time (SI-SCK)	t_h	—	3.3 ± 0.3	—	0	0	ns
			5.0 ± 0.5	—	0	0	
Minimum hold time (SCK-RCK, $\overline{SCLR}$-RCK)	t_h	—	3.3 ± 0.3	—	0	0	ns
			5.0 ± 0.5	—	0	0	
Minimum removal time ($\overline{SCLR}$)	t_{rem}	—	3.3 ± 0.3	—	5.0	6.0	ns
			5.0 ± 0.5	—	3.0	3.5	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time (SCK- Q8',Q8C)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	6.3	10.1	1.0	11.5	ns
				50	—	8.5	13.7	1.0	15.7	
			5.0 ± 0.5	15	—	4.5	6.8	1.0	7.8	
				50	—	6.3	9.3	1.0	10.6	
Propagation delay time ($\overline{SCLR}$ -Q8',Q8C')	t_{pHL}	—	3.3 ± 0.3	15	—	10.6	16.2	1.0	18.5	ns
				50	—	12.9	19.6	1.0	22.4	
			5.0 ± 0.5	15	—	8.1	11.5	1.0	13.1	
				50	—	10.2	14.5	1.0	16.6	
Propagation delay time (RCK-Q_n)	t_{pLH} t_{pHL}	—	3.3 ± 0.3	15	—	7.0	11.2	1.0	12.8	ns
				50	—	9.8	15.1	1.0	17.2	
			5.0 ± 0.5	15	—	5.3	8.3	1.0	9.5	
				50	—	7.7	10.9	1.0	12.4	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	99	160	—	87	—	MHz
				50	73	118	—	64	—	
			5.0 ± 0.5	15	148	224	—	129	—	
				50	108	160	—	94	—	
Input capacitance	C_{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)			—	67	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

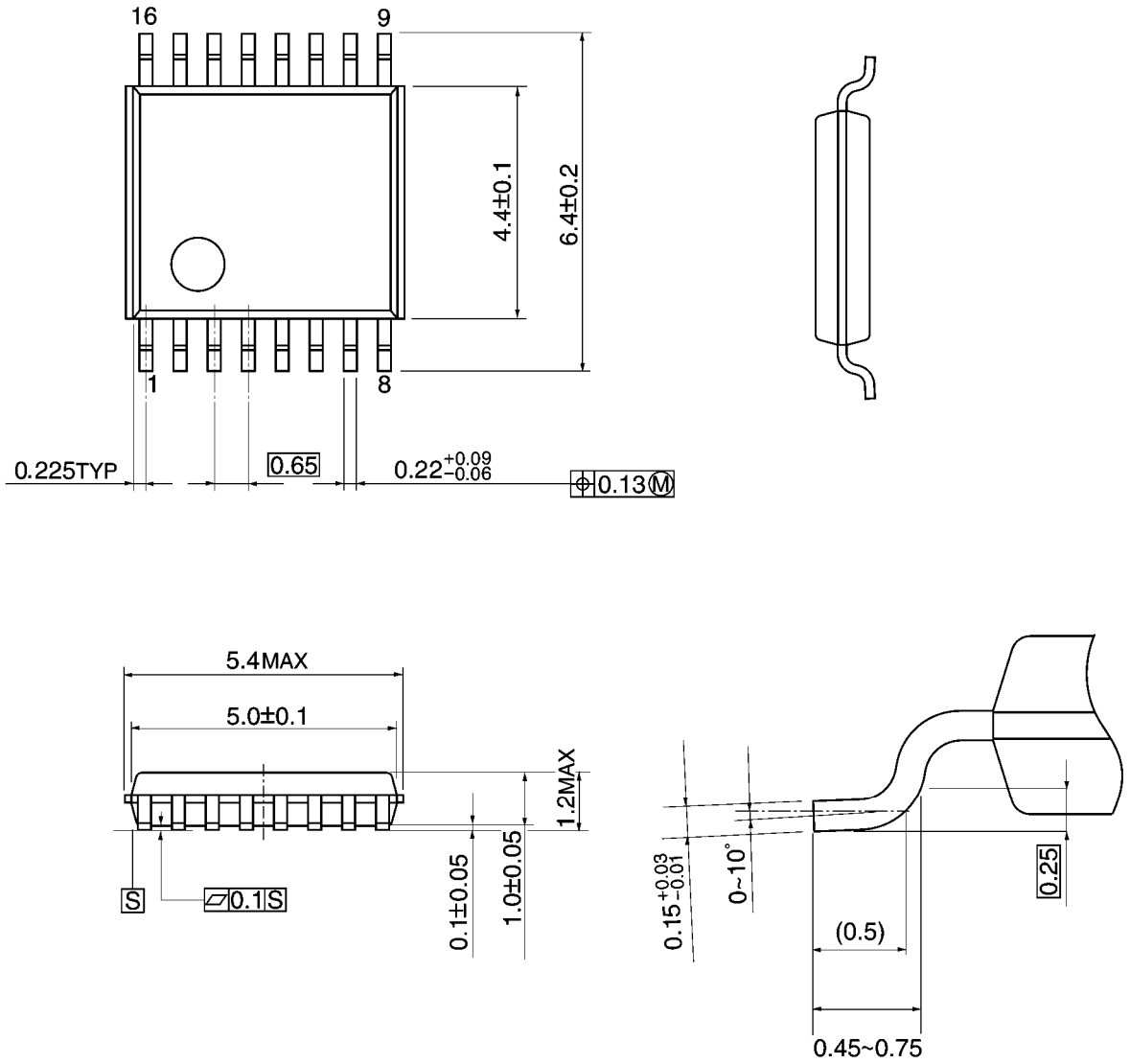
$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

Noise Characteristics (input: tr = tf = 3 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V_{CC} (V)	Typ.	Limit	
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.6	1.0	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	-0.6	−1.0	V
Minimum high level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

Package Dimensions

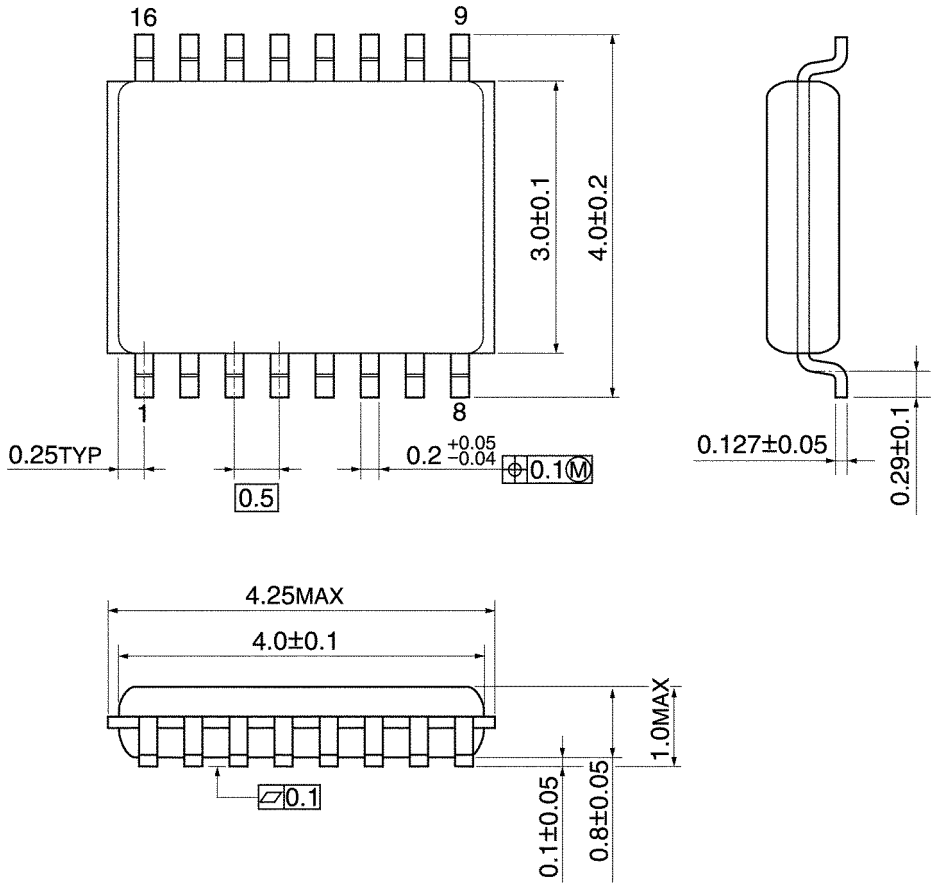
TSSOP16-P-0044-0.65A Unit: mm



Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50 Unit: mm



Weight: 0.02 g (typ.)

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