

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC9164FT, TC74VHC9164FK

## 8-Bit Shift Register (Parallel-IN/ Serial-OUT, Serial -IN/ Parallel -OUT)

The TC74VHC9164 is an ultra-high-speed 8-Bit Shift Register fabricated using silicon-gate CMOS technology. The TC74VHC9164 combines low power consumption of CMOS with Schottky TTL speeds.

The TC74VHC9164 has parallel data inputs/outputs, a serial input and a serial output. It converts parallel data into serial data or vice versa.

When P/S CONT is Low, Q/D1 to Q/D8 are configured as parallel data outputs. At this time, the SI input is serially loaded on the rising edges of CK and unloaded from the Q/D1 to Q/D8 outputs in parallel. When CLR/LOAD input is Low, all flip-flops are asynchronously reset, irrespective of the CK state.

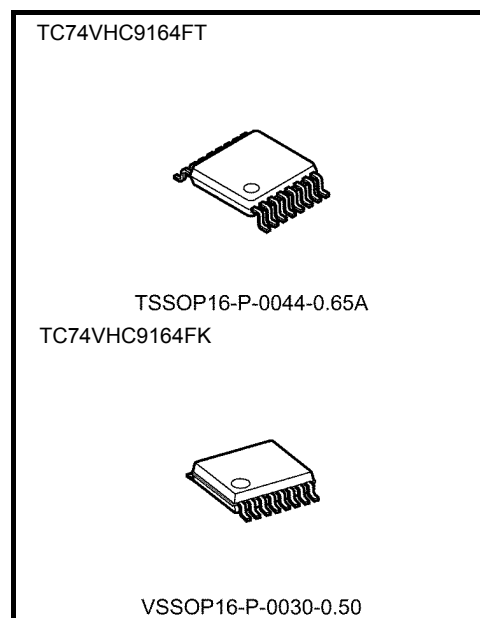
When P/S CONT is High, Q/D1 to Q/D8 are configured as parallel data inputs. At this time, when CLR/LOAD is Low, Q/D1 to Q/D8 latch data in parallel asynchronously from the CK input.

All the inputs have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHC9164 is capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.

Additionally, all the inputs have a newly developed protection circuit without a diode returned to VCC. This enables the inputs to be tolerant of up to 5.5 volts even when power supply is down. The input power-down protection capability makes the TC74VHC9164 ideal for a wide range of applications, such as interfacing between different voltages, voltage translation from 5 V to 3 V and battery back-up circuits.

### Features

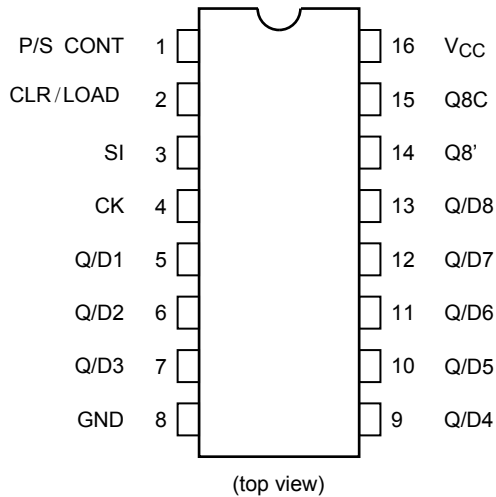
- High speed:  $f_{max} = 149$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC} (opr) = 2$  to 5.5 V



#### Weight

TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

## Pin Assignment

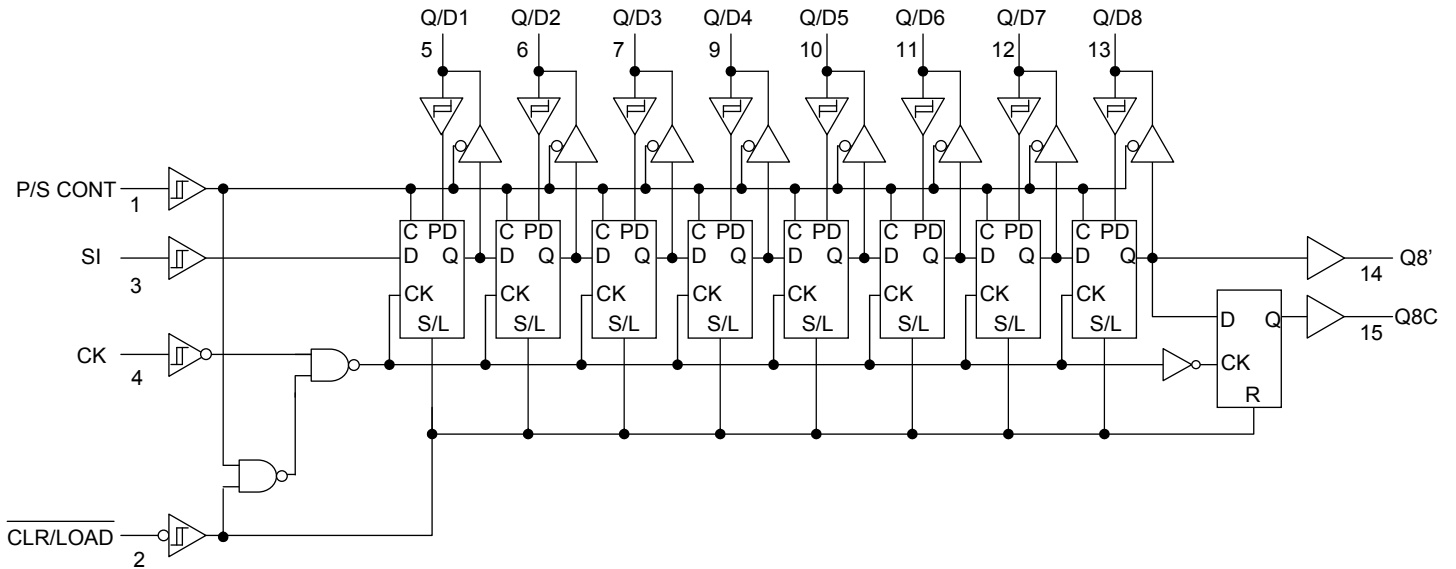


## Truth Table

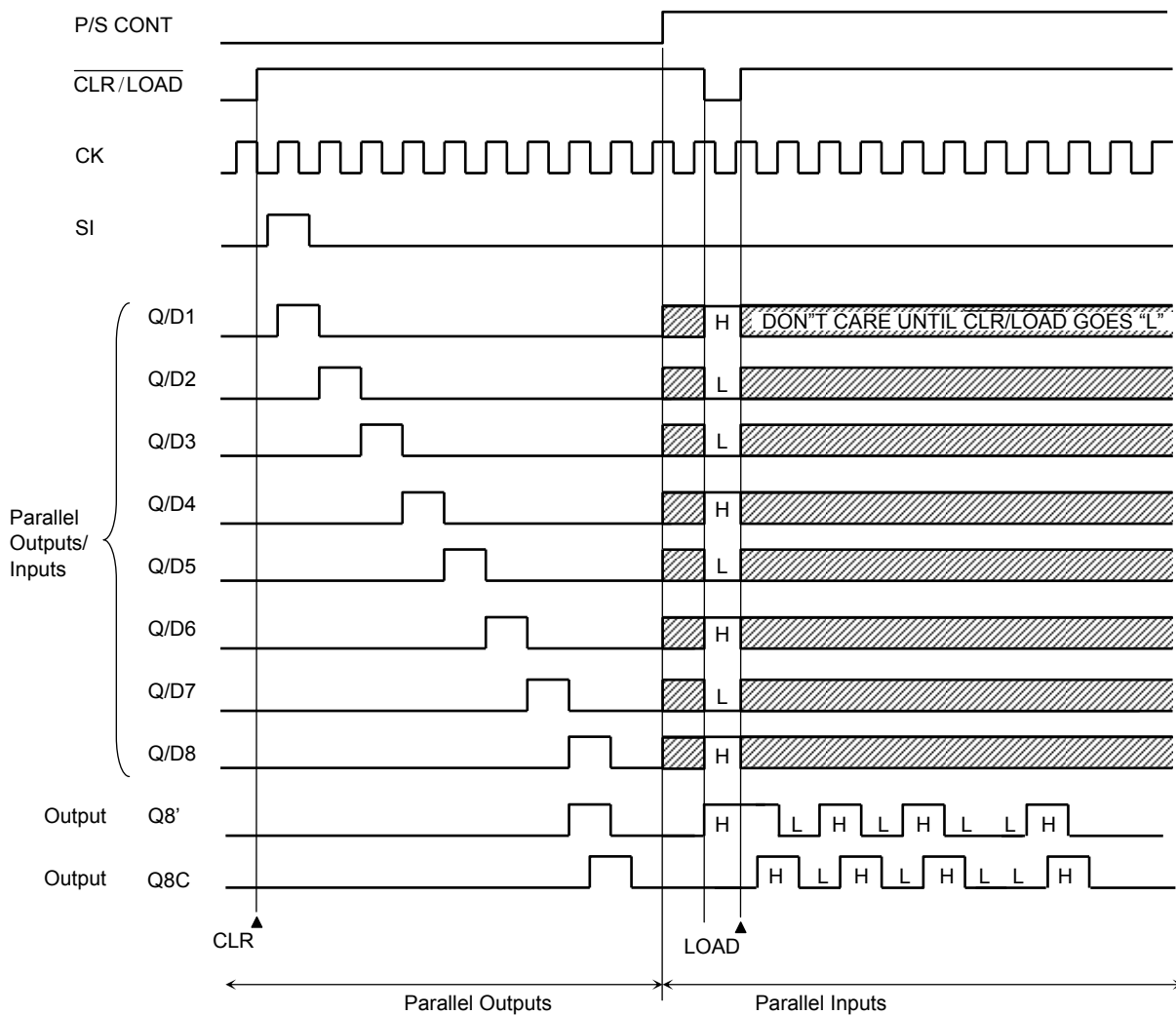
Inputs				Parallel Outputs/Inputs	Function
P/S CONT	$\overline{\text{CLR/LOAD}}$	SI	CK	Q/D1.....Q/D8	
L	X	X	X	Output- state Parallel Outputs	Q/D1 to Q/D8 are configured as parallel outputs.
L	L	X	X		Shift register is cleared.
L	H	L	$\uparrow$		First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
L	H	H	$\uparrow$		First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
L	H	X	$\downarrow$		The shift register remains unchanged. The Q8C output keeps the value of the previous flip-flop.
H	X	X	X	Input- state Parallel Inputs	Q/D1 to Q/D8 are configured as parallel inputs.
H	L	X	X		Q/D1 to Q/D8 are latched into the shift register.
H	H	L	$\uparrow$		First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	H	H	$\uparrow$		First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
H	H	X	$\downarrow$		The shift register remains unchanged. The Q8C output keeps the value of the previous flip-flop.

X: Don't care

## System Diagram



## Timing Chart



## Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
DC bus I/O voltage (Q/D1 to Q/D8)	$V_{I/O}$	-0.5 to 7.0 (Note2)	V
		-0.5~ $V_{CC} + 0.5$ (Note3)	
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 75$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note2 Output in off-state

Note3 High or low state. IOUT absolute maximum rating must be observed.

## Operating Ranges (Note1)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
DC bus I/O voltage (Q/D1 to Q/D8)	$V_{I/O}$	0 to 5.5 (Note2)	V
		0 to $V_{CC}$ (Note3)	
Operating temperature	$T_{opr}$	-40 to 85	$^{\circ}C$

Note1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note2 Output in off-state

Note3 High or low state.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40~85°C		Unit		
				V <sub>CC</sub> (V)	Min	Typ	Max	Min		Max	
Positive threshold voltage	V <sub>P</sub>	—		3.0	—	—	2.20	—	2.20	V	
				4.5	—	—	3.15	—	3.15		
				5.5	—	—	3.85	—	3.85		
Negative threshold voltage	V <sub>N</sub>	—		3.0	0.90	—	—	0.90	—	V	
				4.5	1.35	—	—	1.35	—		
				5.5	1.65	—	—	1.65	—		
Hysteresis voltage	V <sub>H</sub>	—		3.0	0.30	—	1.20	0.30	1.20	V	
				4.5	0.40	—	1.40	0.40	1.40		
				5.5	0.50	—	1.60	0.50	1.60		
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	1.9	—	V
					3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—		
				I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
					4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>		I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	—	0.1	V
					3.0	—	0.0	0.1	—	0.1	
					4.5	—	0.0	0.1	—	0.1	
				I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
					4.5	—	—	0.36	—	0.44	
3-state output off-state current (Q/D1 to Q/D8)	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>I/O</sub> = 5.5 V or GND		0 to 5.5	—	—	±0.25	—	±2.5	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	—	—	4.0	—	40.0	μA	

### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_w$ (L)	—	3.3 ± 0.3	—	7.0	8.0	ns
	$t_w$ (H)		5.0 ± 0.5	—	5.0	6.0	
Minimum pulse width ( CLR/LOAD )	$t_w$ (L)	—	3.3 ± 0.3 5.0 ± 0.5	— —	6.0 5.0	7.0 6.0	ns
Minimum set-up time (Q/D1 to Q/D8 – CLR/LOAD )	$t_s$	—	3.3 ± 0.3	—	6.0	7.0	ns
			5.0 ± 0.5	—	5.0	6.0	
Minimum set-up time (SI-CK)	$t_s$	—	3.3 ± 0.3	—	6.0	7.0	ns
			5.0 ± 0.5	—	5.0	5.0	
Minimum hold time (Q/D1 to Q/D8 – CLR/LOAD )	$t_h$	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.0	1.0	
Minimum hold time (SI-CK)	$t_h$	—	3.3 ± 0.3	—	1.0	1.0	ns
			5.0 ± 0.5	—	1.5	1.5	
Minimum removal time ( CLR/LOAD -CK)	$t_{rem}$	—	3.3 ± 0.3	—	5.0	5.0	ns
			5.0 ± 0.5	—	3.0	3.0	

## AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (CK – Q/D1 to Q/D8)	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	9.3	14.7	1.0	16.7	ns
				50	—	12.1	19.0	1.0	21.6	
	5.0 ± 0.5		15	—	6.7	9.7	1.0	11.1		
			50	—	9.1	13.1	1.0	14.9		
Propagation delay time (CK – Q8', Q8C)	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	9.0	14.4	1.0	16.4	ns
				50	—	11.8	18.6	1.0	21.2	
	5.0 ± 0.5		15	—	6.4	9.4	1.0	10.7		
			50	—	8.7	12.7	1.0	14.5		
Propagation delay time (CLR/LOAD – Q/D1 to Q/D8)	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	7.9	11.7	1.0	13.4	ns
				50	—	10.2	15.1	1.0	17.2	
	5.0 ± 0.5		15	—	6.2	8.4	1.0	9.6		
			50	—	8.0	11.1	1.0	12.6		
Propagation delay time (CLR/LOAD – Q8', Q8C)	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	8.0	11.8	1.0	13.5	ns
				50	—	10.3	15.3	1.0	17.5	
	5.0 ± 0.5		15	—	6.2	8.5	1.0	9.7		
			50	—	8.1	11.2	1.0	12.8		
Propagation delay time (Q/D8-Q8)	t <sub>pLH</sub>	—	3.3 ± 0.3	15	—	9.5	15.2	1.0	17.3	ns
				50	—	11.8	18.9	1.0	21.6	
	5.0 ± 0.5		15	—	6.7	9.6	1.0	10.9		
			50	—	8.4	12.2	1.0	13.9		
3-state output enable time (P/S CONT – Q/D1 to Q/D8)	t <sub>pZL</sub>	RL=1kΩ	3.3 ± 0.3	15	—	6.7	10.4	1.0	11.9	ns
				50	—	9.9	15.4	1.0	17.6	
	5.0 ± 0.5		15	—	5.0	7.3	1.0	8.3		
			50	—	7.6	11.0	1.0	12.5		
3-state output disable time (P/S CONT – Q/D1 to Q/D8)	t <sub>pLZ</sub>	RL=1kΩ	3.3 ± 0.3	50	—	10.1	12.8	1.0	13.7	ns
	t <sub>pHZ</sub>		5.0 ± 0.5	50	—	7.8	9.8	1.0	10.6	
Maximum clock frequency	f <sub>max</sub>	—	3.3 ± 0.3	15	68	107	—	59	—	MHz
				50	52	82	—	46	—	
			5.0 ± 0.5	15	103	149	—	90	—	
				50	76	109	—	67	—	
Input capacitance	C <sub>IN</sub>	—			—	4	10	—	10	pF
bus Input capacitance	C <sub>I/O</sub>	—			—	8	—	—	—	pF
Power dissipation capacitance (Note)	C <sub>PD</sub>	P/S CONT=L (Parallel Outputs)			—	102	—	—	—	pF
		P/S CONT=H (Parallel Inputs)			—	34	—	—	—	

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

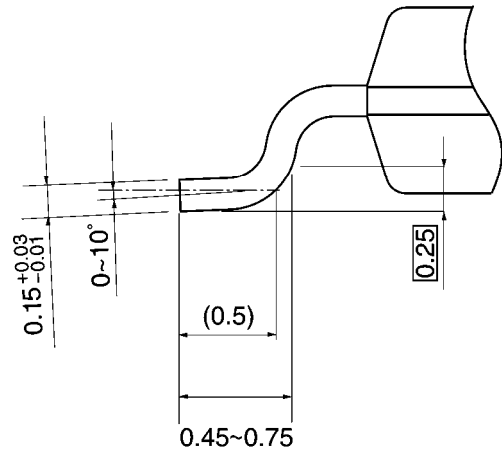
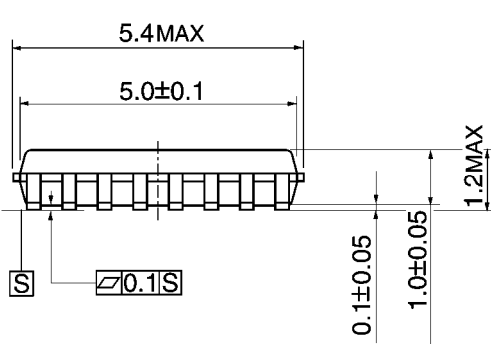
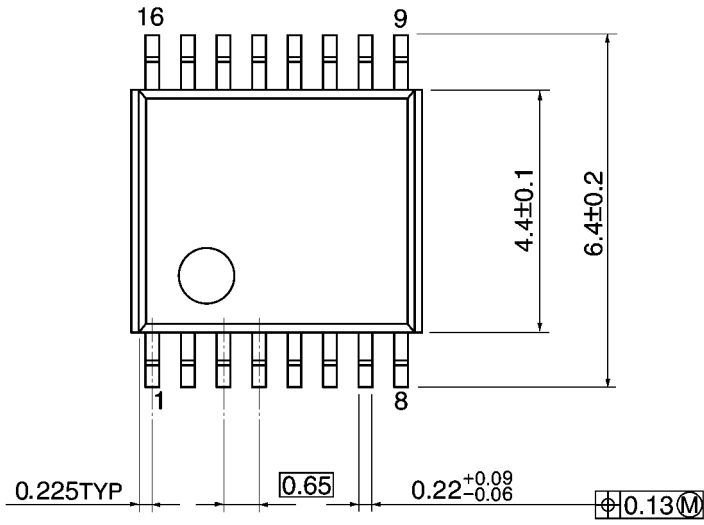
Noise Characteristics (input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Unit
			V <sub>CC</sub> (V)	Typ.	Max	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.6	1.0	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.5	-1.0	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Package Dimensions**

TSSOP16-P-0044-0.65A

Unit: mm

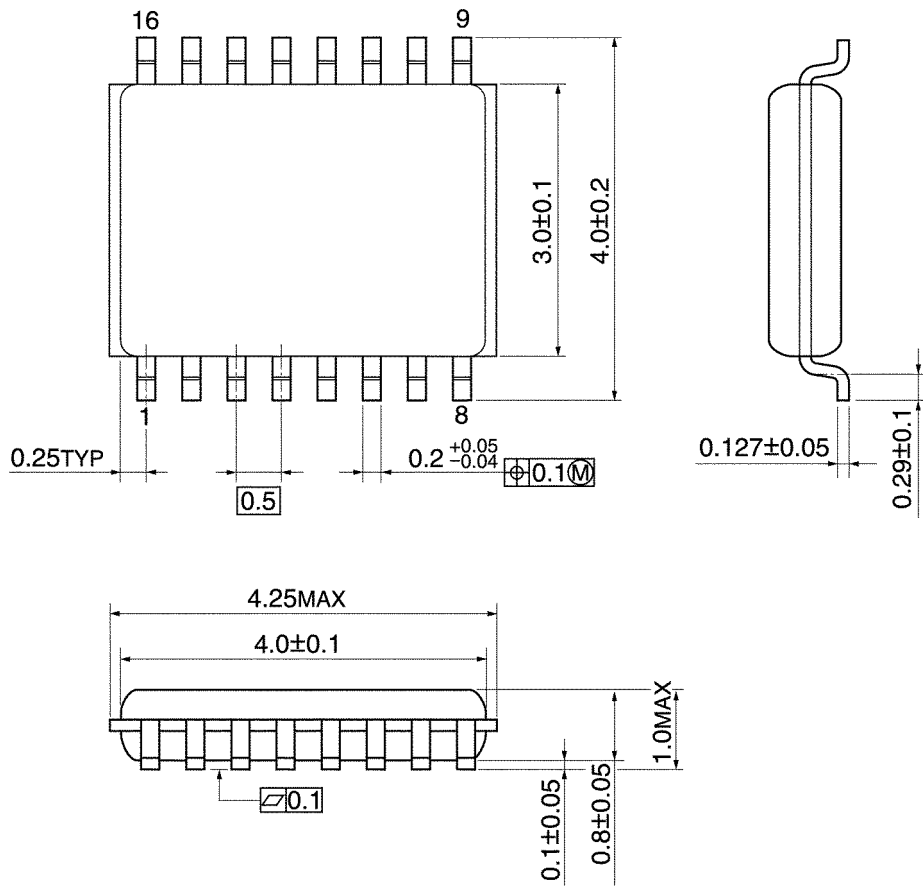


Weight: 0.06 g (typ.)

## Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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