

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VCXHR162652FT

Low-Voltage 16-Bit Bus Transceiver/Register with Bushold

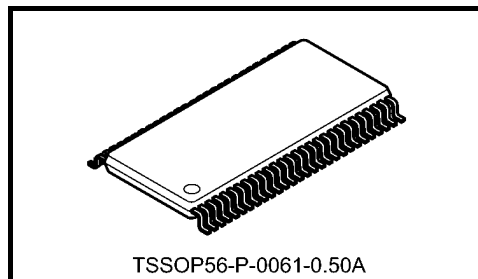
The TC74VCXHR162652FT is a high-performance CMOS 16-bit bus transceiver/register. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

The A, B data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

All inputs are equipped with protection circuits against static discharge.



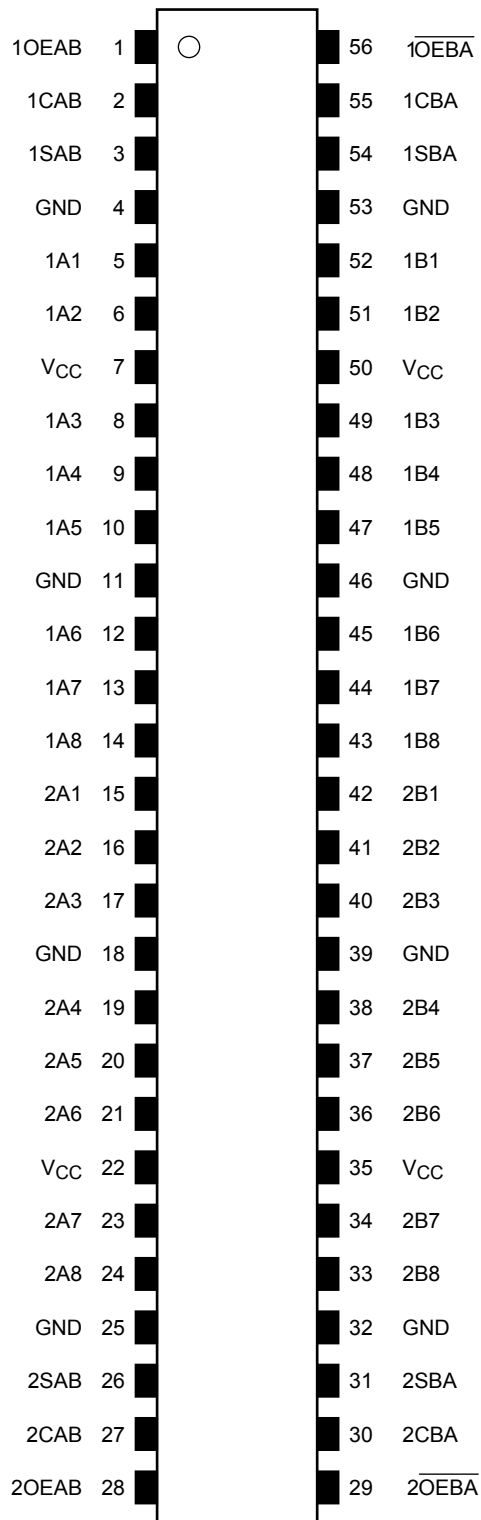
Weight: 0.25 g (typ.)

Features (Note)

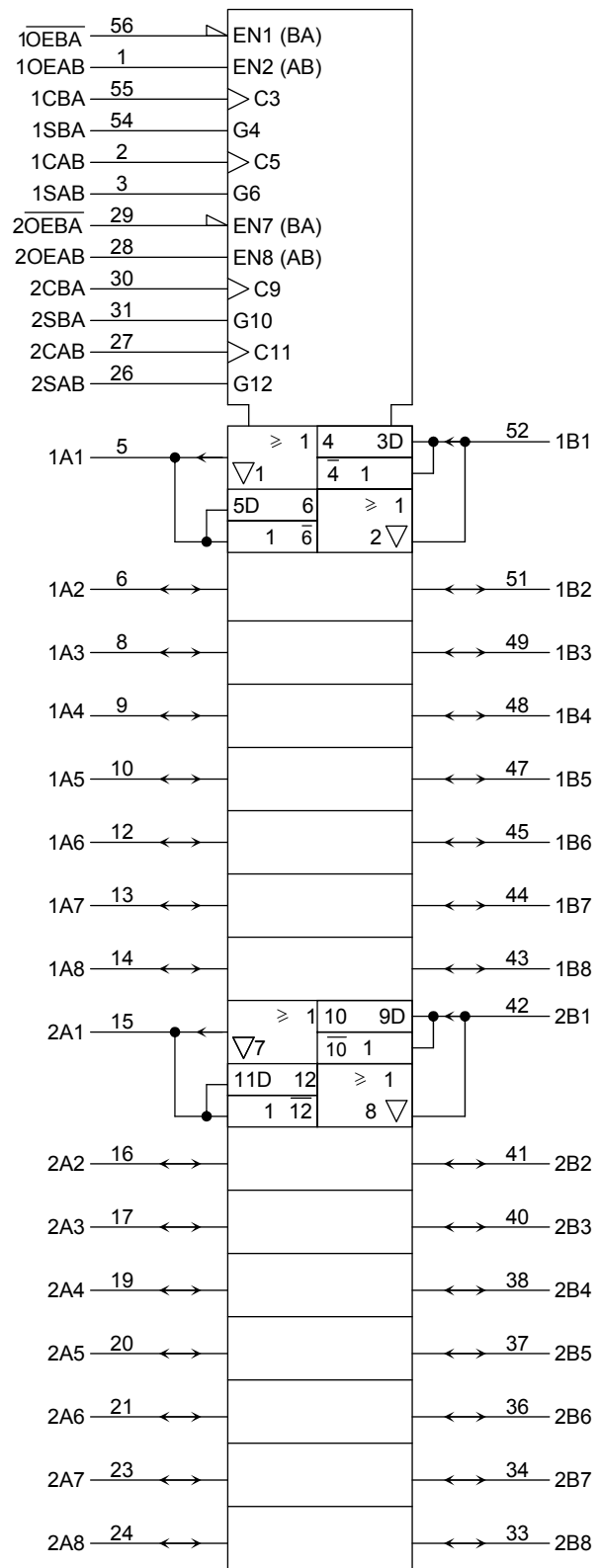
- 26- Ω series resistors on outputs
- Low-voltage operation: $V_{CC} = 1.8$ to 3.6 V
- Bushold on data inputs eliminating the need for external pull-up/pull-down resistors
- High-speed operation: $t_{pd} = 3.8$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
: $t_{pd} = 4.9$ ns (max) ($V_{CC} = 2.3$ to 2.7 V)
: $t_{pd} = 9.8$ ns (max) ($V_{CC} = 1.8$ V)
- 3.6-V tolerant control inputs
- Output current: $I_{OH}/I_{OL} = \pm 12$ mA (min) ($V_{CC} = 3.0$ V)
: $I_{OH}/I_{OL} = \pm 8$ mA (min) ($V_{CC} = 2.3$ V)
: $I_{OH}/I_{OL} = \pm 4$ mA (min) ($V_{CC} = 1.8$ V)
- Latch-up performance: -300 mA
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Package: TSSOP

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.







Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Control Inputs						Bus		Function
OEAB	\overline{OEBA}	CAB	CBA	SAB	SBA	A	B	
L	H	X*	X*	X	X	Input	Input	The output functions of A and B Busses are disabled.
		Z	Z			Z	Z	
				X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
		X*	X*	L	X	Input	Output	The data on the A bus are displayed on the B bus.
H	H	X*	X*	L	X	L	L	
		H	H			H	H	
			X*	L	X	L	L	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		H	H			H	H	
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
			X*	H	X	L	L	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
		X*	X*	X	L	Output	Input	The data on the B Bus are displayed on the A bus.
		L	L			L	L	
L	L	X*		X	L	L	L	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		H	H			H	H	
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
			X*	X	H	L	L	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
		X*	X*	X	H	Output	Output	The data in the A storage flop-flops are displayed on the B Bus, and the data in the B storage flop-flops are displayed on the A.
		H	L	X*	X*	H	H	Qn

X: Don't care

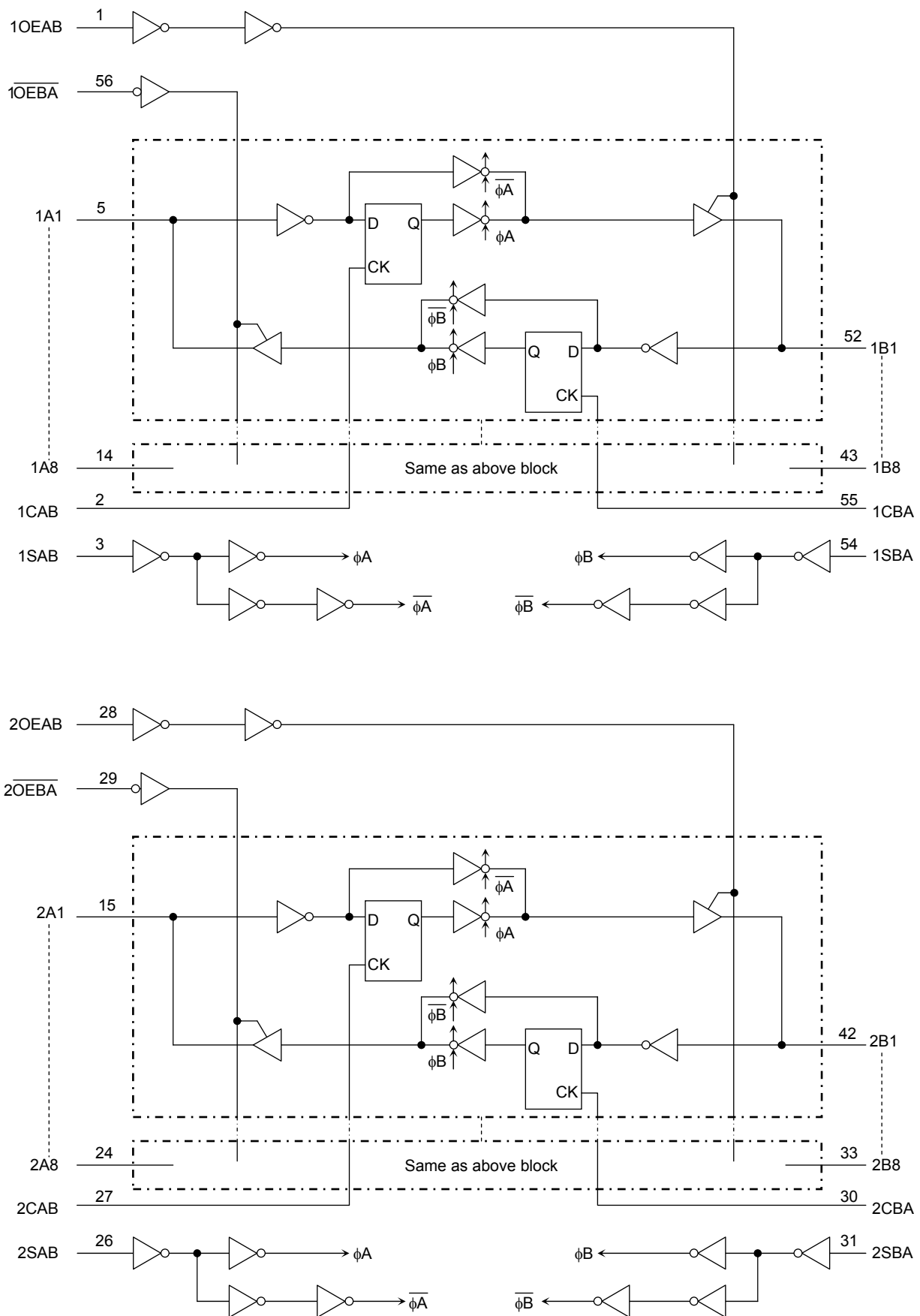
Z: High impedance

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

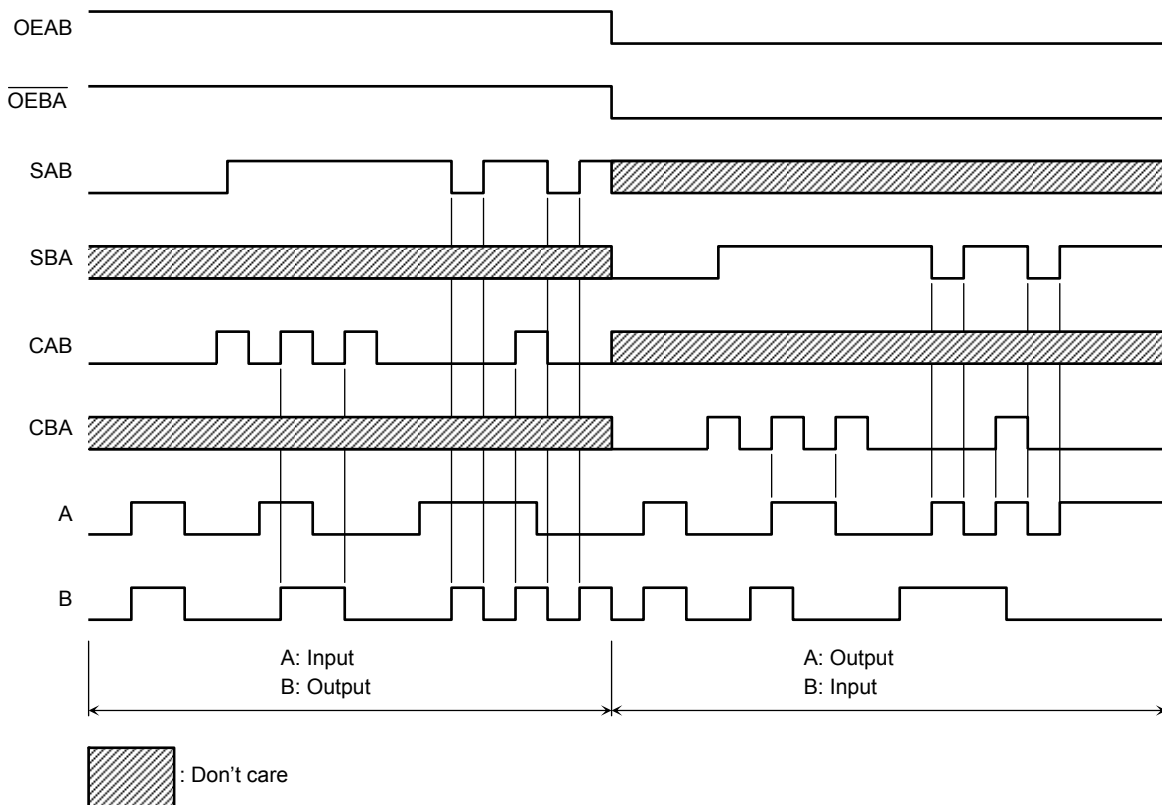
*: The clocks are not internally gated with either OEAB or \overline{OEBA} .

Therefore, data on the A and/or B busses may be clocked into the storage flip-flops at any time.

System Diagram



Timing Chart



Absolute Maximum Ratings (Note 1)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	-0.5 to 4.6	V
DC input voltage	(OEAB, \overline{OEBA} , SAB, SBA, CAB, CBA)	V_{IN}	-0.5 to 4.6	V
	(An, Bn)		-0.5 to $V_{CC} + 0.5$ (Note 2)	
DC output voltage	(An, Bn)	V_{OUT}	-0.5 to $V_{CC} + 0.5$ (Note 3)	V
Input diode current		I_{IK}	-50	mA
Output diode current		I_{OK}	± 50 (Note 4)	mA
Output current		I_{OUT}	± 50	mA
Power dissipation		P_D	400	mW
DC V_{CC} /ground current per supply pin		I_{CC}/I_{GND}	± 100	mA
Storage temperature		T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

Operating Ranges (Note 1) (Note 2)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	1.8 to 3.6	V
			1.2 to 3.6 (Note 3)	
Input voltage	(OEAB, \overline{OEBA} , SAB, SBA, CAB, CBA)	V_{IN}	-0.3 to 3.6	V
	(An, Bn)		0 to V_{CC} (Note 4)	
Output voltage	(An, Bn)	V_{OUT}	0 to V_{CC} (Note 5)	V
Output current		I_{OH}/I_{OL}	± 12 (Note 6)	mA
			± 8 (Note 7)	
			± 4 (Note 8)	
Operating temperature		T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time		dt/dv	0 to 10 (Note 9)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Note 2: Floating or unused control inputs must be held high or low.

Note 3: Data retention only

Note 4: OFF state

Note 5: High or low state

Note 6: $V_{CC} = 3.0$ to 3.6 V

Note 7: $V_{CC} = 2.3$ to 2.7 V

Note 8: $V_{CC} = 1.8$ V

Note 9: $V_{IN} = 0.8$ to 2.0 V, $V_{CC} = 3.0$ V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C, 2.7 V < VCC ≤ 3.6 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.7 to 3.6	2.0	—	V
	L-level	V _{IL}	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.7 to 3.6	V _{CC} - 0.2	—	V
				I _{OH} = -6 mA	2.7	2.2	—	
				I _{OH} = -8 mA	3.0	2.4	—	
				I _{OH} = -12 mA	3.0	2.2	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7 to 3.6	—	0.2	
				I _{OL} = 6 mA	2.7	—	0.4	
				I _{OL} = 8 mA	3.0	—	0.5	
				I _{OL} = 12 mA	3.0	—	0.8	
Input leakage current (OEAB, $\overline{\text{OEBA}}$, SAB, SBA, CAB, CBA)		I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
Bushold input minimum drive hold current		I _I (HOLD)	V _{IN} = 0.8 V		3.0	75	—	μA
			V _{IN} = 2.0 V		3.0	-75	—	
Bushold input over-drive current to change state		I _I (OD)	(Note 1)		3.6	—	450	μA
			(Note 2)		3.6	—	-450	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		2.7 to 3.6	—	±10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.7 to 3.6	—	20.0	μA
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7 to 3.6	—	750	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta = -40 to 85°C, 2.3 V ≤ VCC ≤ 2.7 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		2.3 to 2.7	1.6	—	V
	L-level	V _{IL}	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3 to 2.7	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	2.3	2.0	—	
				I _{OH} = -6 mA	2.3	1.8	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3 to 2.7	—	0.2	
				I _{OL} = 6 mA	2.3	—	0.4	
				I _{OL} = 8 mA	2.3	—	0.6	
Input leakage current (OEAB, $\overline{\text{OEBA}}$, SAB, SBA, CAB, CBA)		I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
Bushold input minimum drive hold current		I _I (HOLD)	V _{IN} = 0.7 V		2.3	45	—	μA
			V _{IN} = 1.6 V		2.3	-45	—	
Bushold input over-drive current to change state		I _I (OD)	(Note 1)		2.7	—	300	μA
			(Note 2)		2.7	—	-300	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		2.3 to 2.7	—	±10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.3 to 2.7	—	20.0	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

DC Characteristics (Ta = -40 to 85°C, 1.8 V ≤ VCC < 2.3 V)

Characteristics		Symbol	Test Condition		VCC (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		1.8 to 2.3	0.7 × V _{CC}	—	V
	L-level	V _{IL}	—		1.8 to 2.3	—	0.2 × V _{CC}	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	1.8	1.4	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0.2	
				I _{OL} = 4 mA	1.8	—	0.3	
Input leakage current (OEAB, $\overline{\text{OEBA}}$, SAB, SBA, CAB, CBA)		I _{IN}	V _{IN} = 0 to 3.6 V		1.8	—	±5.0	μA
Bushold input minimum drive hold current		I _I (HOLD)	V _{IN} = 0.36 V		1.8	25	—	μA
			V _{IN} = 1.26 V		1.8	-25	—	
Bushold input over-drive current to change state		I _I (OD)	(Note 1)		1.8	—	200	μA
			(Note 2)		1.8	—	-200	
3-state output OFF state current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		1.8	—	±10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		1.8	—	20.0	μA

Note 1: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 2: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

AC Characteristics (Ta = -40 to 85°C, input: tr = tf = 2.0 ns, CL = 30 pF, RL = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	VCC (V)	Min	Max	Unit
Maximum clock frequency	f _{max}	Figure 1, Figure 3	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation delay time (An, Bn-Bn, An)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
Propagation delay time (CAB, CBA-Bn, An)	t _{pLH} t _{pHL}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.1	
Propagation delay time (SAB, SBA-Bn, An)	t _{pLH} t _{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.8	
			3.3 ± 0.3	0.6	4.4	
Output enable time (OEAB, OEBA -An, Bn)	t _{pZL} t _{pZH}	Figure 1, Figure 4, Figure 5	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
Output disable time (OEAB, OEBA -An, Bn)	t _{pLZ} t _{pHZ}	Figure 1, Figure 4, Figure 5	1.8	1.5	9.4	ns
			2.5 ± 0.2	0.8	5.2	
			3.3 ± 0.3	0.6	4.5	
Minimum pulse width	t _w (H) t _w (L)	Figure 1, Figure 3	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t _s	Figure 1, Figure 3	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t _h	Figure 1, Figure 3	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t _{osLH} t _{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic Switching Characteristics

($T_a = 25^\circ\text{C}$, input: $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note)	1.8	0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note)	2.5	0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note)	3.3	0.35	
Quiet output minimum dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note)	1.8	-0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note)	2.5	-0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note)	3.3	-0.35	
Quiet output minimum dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note)	1.8	1.55	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note)	2.5	2.05	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note)	3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Typ.	Unit
Input capacitance	C _{IN}	(OEAB, $\overline{\text{OEBA}}$, CAB, CBA, SAB, SBA)	1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	C _{I/O}	An, Bn	1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C _{PD}	f _{IN} = 10 MHz (Note)	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/16 \text{ (per bit)}$$

AC Test Circuit

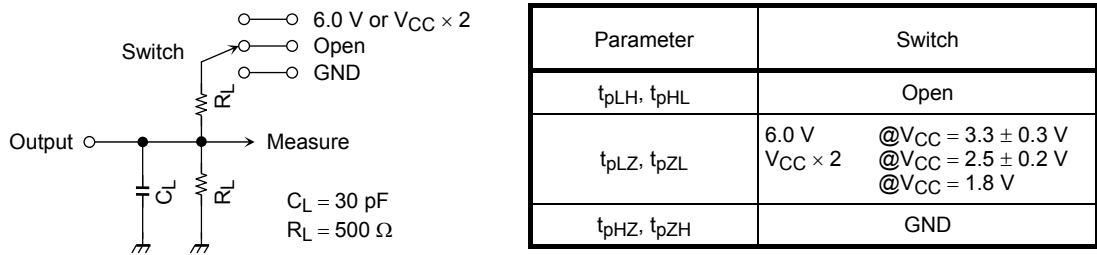


Figure 1

AC Waveform

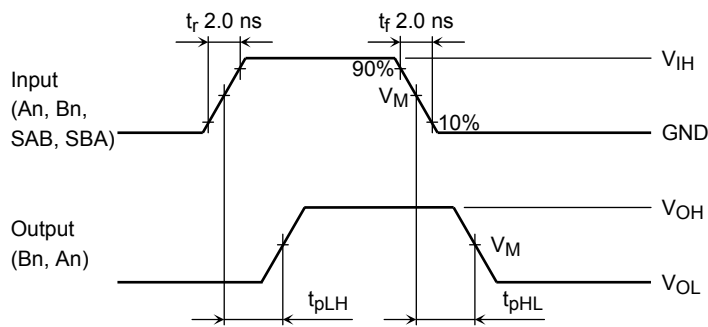


Figure 2 t_{pLH} , t_{pHL}

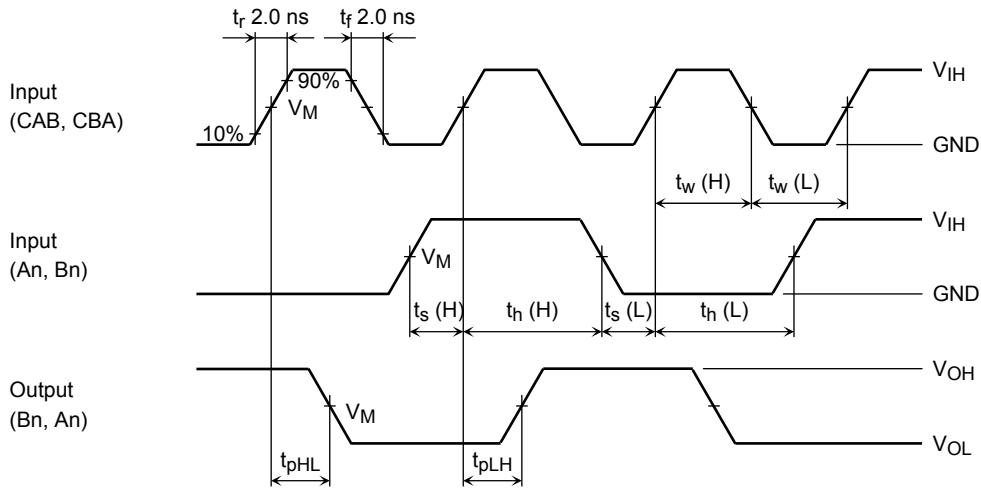


Figure 3 t_{pLH} , t_{pHL} , t_w , t_s , t_h

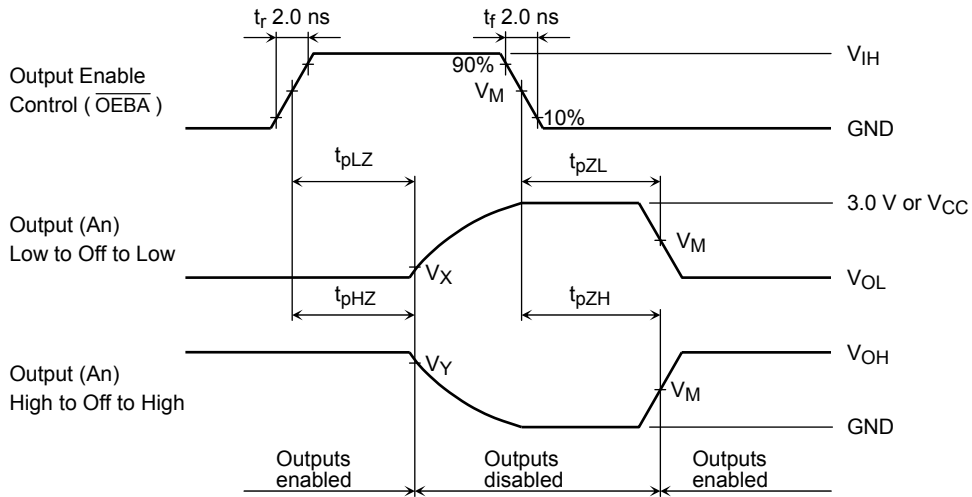


Figure 4 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

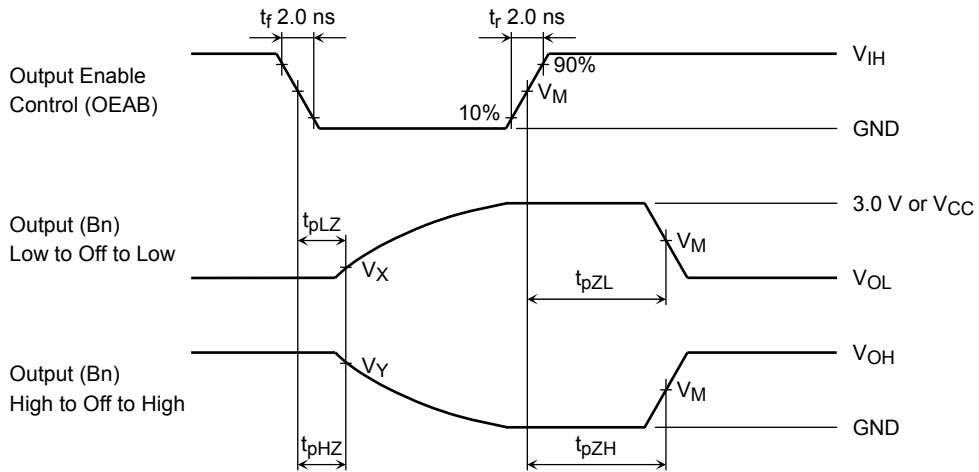


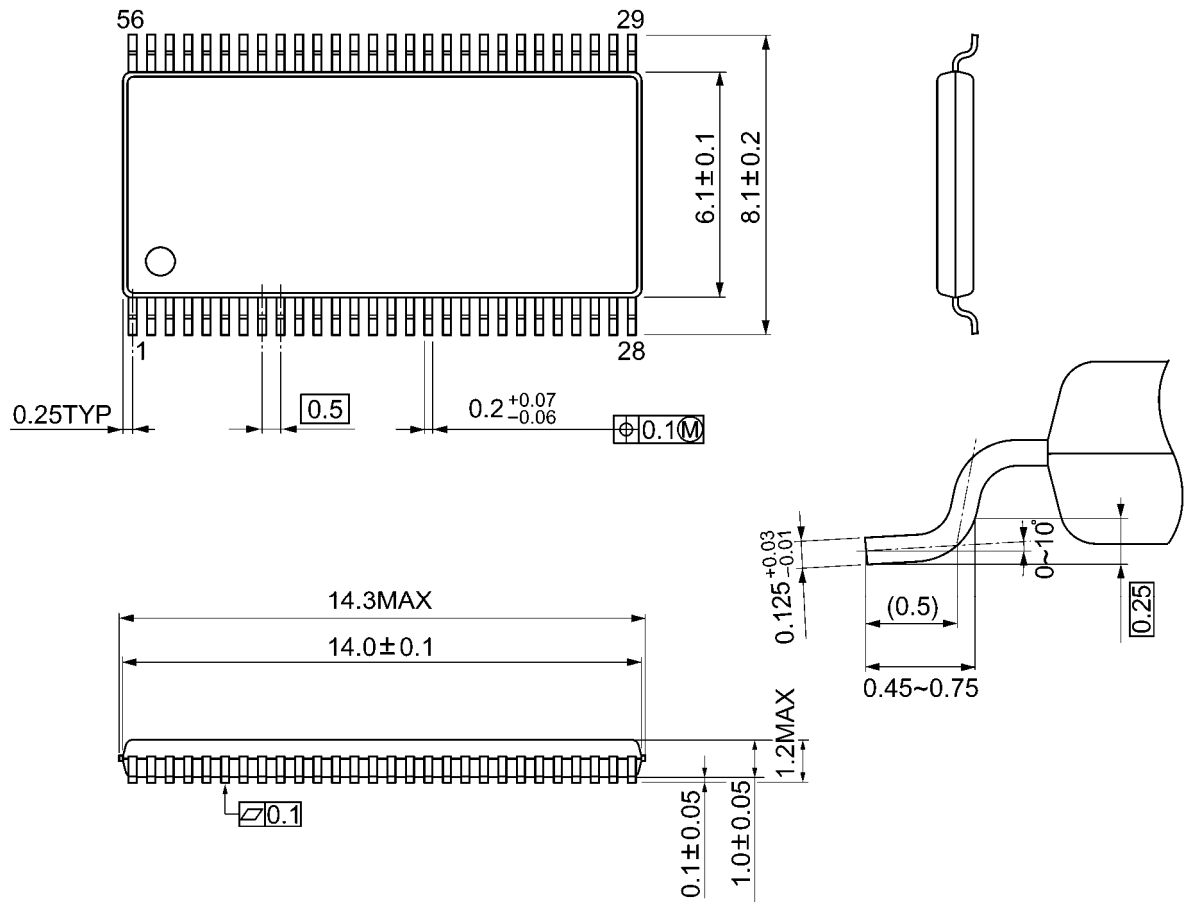
Figure 5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V

Package Dimensions

TSSOP56-P-0061-0.50A

Unit: mm



Weight: 0.25 g (typ.)

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