AAT2215

SwitchReg™ High Current Synchronous Step-Up Regulator with Programmable Current Limit

General Description

The AAT2215 SwitchReg™ is a high current, synchronous step-up converter with a programmable peak NMOS current limit. It is ideal to prevent the input current from overloading the system power in PC Card GSM/GPRS/3G and WiMax modem card applications. The AAT2215's internal compensation is optimized for the large bulk tantalum output capacitors needed to support the output voltage during large load pulses.

The output voltage may be programmed from 3.0V to 5.5V by external resistor divider. Light load switching frequency modulation and low quiescent current maintain high efficiency performance for light load mode conditions.

Two current limits are designed into the AAT2215. One is the low-side power MOSFET programmable peak current limit, which works when the device is in step-up regulation state. An external resistor is used to program the current limit from 600mA to 4.0A. The other is the high-side current limit, which operates in a linear mode to limit inrush current to 750mA when the output charges up to the input voltage. The AAT2215 includes internal over-voltage protection and a system ready signal.

The AAT2215 is available in a Pb-free, 3mm x 3mm, 12-pin TDFN package (TDFN33-12) rated from -40°C to +85°C.

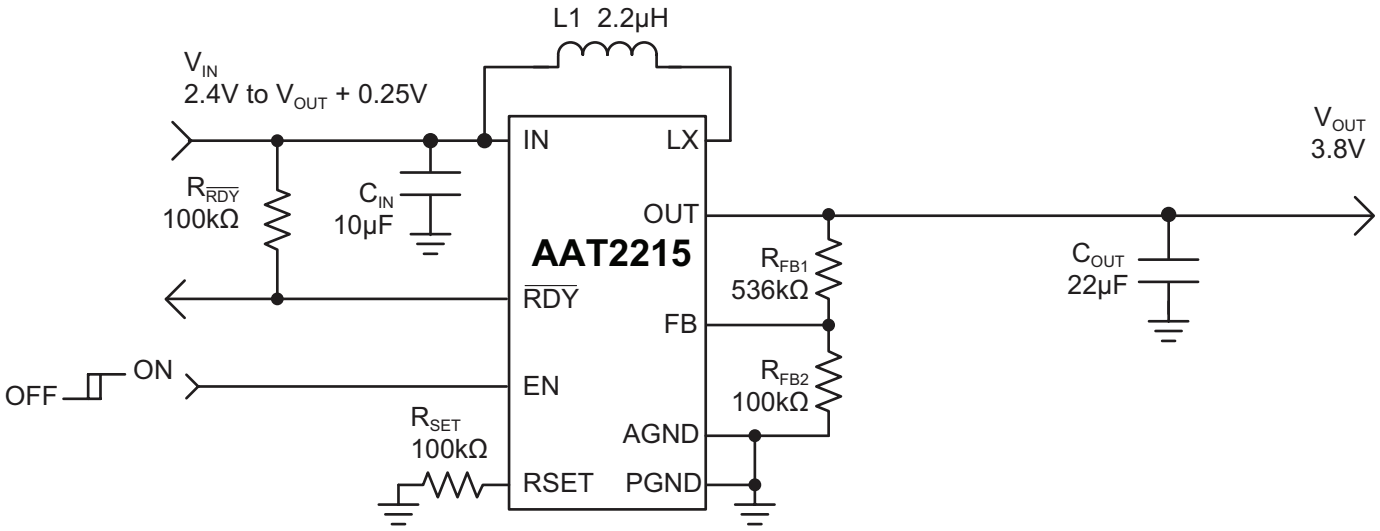
Features

- 2.4V to V_{OUT} + 0.25V Input Voltage Range
- Adjustable 3.0V to 5.5V Output Voltage
- Internal Compensation
- 600kHz Switching Frequency
- Programmable Peak NMOS Current Limit (0.6A to 4.0A)
- Synchronous P-Channel MOSFET
  - True Load Disconnect in Shutdown
  - Reverse Current Block When Enabled
  - Start-Up Inrush Current Limit (0.75A) and Overload Current Limit (3A)
- Up to 95% Efficiency
- Active-Low Power Ready Indicator ($\overline{RDY}$)
- Very Low 55µA No-Load Operating Current
- Less than 1µA Shutdown Current
- 6V Output Over-Voltage Protection (OVP)
- Thermal Shutdown Protection (TSHDN)
- Short Circuit Protection
- Low-Profile TDFN33-12 Package

Applications

- Media Tablets
- PCI-Express Cards
- PCMCIA Cards
- Modems
- Wireless Data Cards

Typical Application Figure

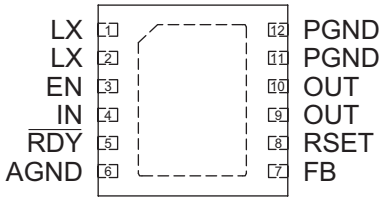


Pin Descriptions

Pin	Name	Function
1, 2	LX	Inductor switching node. LX is internally connected to the source of the internal low-side N-channel MOSFET (NMOS), and synchronous high-side P-channel MOSFET (PMOS). Externally connected to the switching side of the power inductor as shown in the Typical Application drawing.
3	EN	Enable input. A logic high enables the AAT2215 regulator. A logic low forces the AAT2215 into shut-down mode, placing the output into a high-impedance state (true load disconnect) and reducing the quiescent current to less than 1µA.
4	IN	Input supply. IN powers the analog control circuitry during start-up. Bypass IN to GND with a 10µF or greater ceramic capacitor.
5	$\overline{\text{RDY}}$	Power ready signal (active low). $\overline{\text{RDY}}$ is an open-drain, active-low output. $\overline{\text{RDY}}$ is pulled low when the feedback voltage exceeds 95% of the target voltage.
6	AGND	Analog ground. AGND is internally connected to the analog ground of the control circuitry.
7	FB	Feedback input. FB senses the output voltage for regulation control. For adjustable output versions, connect a resistive divider network from the output to FB to GND to set the output voltage accordingly. The FB regulation threshold is 0.6V.
8	RSET	Programmable current-limit control. Connect an external resistor between RSET and AGND to set the peak NMOS current-limit threshold. The current-limit threshold may be adjusted from 0.6A to 4.0A.9
9, 10	OUT	Output of step-up regulator. OUT internally connects to the synchronous high-side P-channel MOSFET.
11, 12	PGND	Power ground. PGND is internally connected to the source of the low-side N-channel MOSFET.
EP	Exposed Pad	Substrate/thermal ground. The exposed pad is internally connected to the substrate of the controller, and provides the lowest thermal impedance between the regulator and the PCB. Connect the exposed pad directly to the ground plane to reduce thermal stress.

Pin Configuration

TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	IN to PGND	-0.3 to 6	V
V_{OUT}, V_{LX}	OUT, LX to PGND[2]	-0.3 to 6	
V_{EN}	EN to AGND	-0.3 to 6	
V_{FB}	FB to AGND	-0.3 to 6	
$V_{\overline{RDY}}$	$\overline{RDY}$ to AGND	-0.3 to 6	
V_{GND}	AGND to PGND	-0.3 to 0.3	
T_J	Junction Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	

Thermal Characteristics[3]

Symbol	Description	Value	Units
TDFN33-12 Thermal Impedance			
θ_{JA}	Maximum Junction-to-Ambient Thermal Resistance	50	°C/W
P_D	Maximum Power Dissipation[4]	2	W

Operating Characteristics

Symbol	Description	Value	Units
T_A	Operating Ambient Temperature Range	-40 to 85	°C
V_{IN}	Input Voltage Range	2.4 to V_{OUT} + 0.25	V
V_{OUT}	Output Voltage Range	3.0 to 5.5	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
2. The P-channel between LX and OUT that changes the substrate connection to control the body diode. This allows the high-side diode when the regulator is active, but allows the output to be isolated from the input during shutdown (true load disconnect).
3. Mounted on 1.6mm thick FR4 board.
4. Derate 25mW/°C above 25°C.

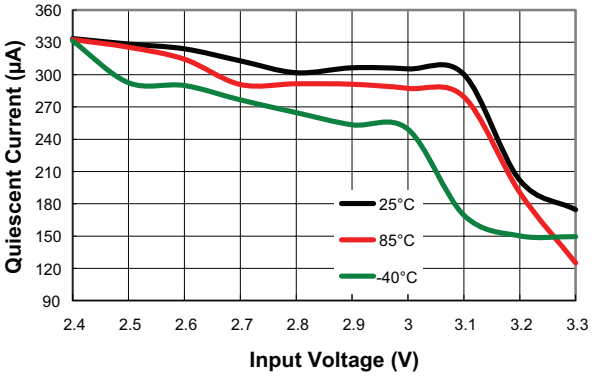
Electrical Characteristics

V_{IN} = 3.3V, V_{OUT} = 3.8V, AGND = PGND. T_A = +25°C, unless otherwise noted.

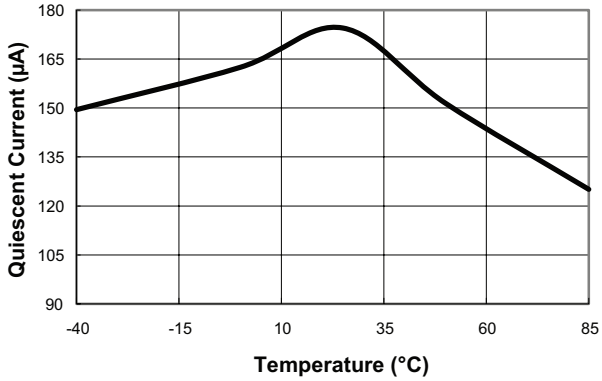
Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		2.4		V_{OUT} + 0.25	V
$V_{IN(MIN)}$	Minimum Start-Up Voltage			2.3	2.4	
V_{OUT}	Output Voltage Range		3.0		5.5	
V_{UVLO}	Input Under-Voltage Lockout	V_{IN} Rising, Hysteresis = 0.1V	1.9	2.1	2.3	
I_Q	Supply Current with No Load	No Load Current; Not Switching		55	80	µA
I_{SHDN}	Shutdown Current	EN = GND, V_{IN} = 5.5V			1	
V_{FB}	FB Accuracy	T_A = 25°C, I_{OUT} = 10mA	0.588	0.60	0.612	V
		T_A = -40°C to 85°C, I_{OUT} = 10mA	0.582	0.60	0618	
I_{FB}	FB Leakage Current	V_{FB} = 0 to 1.0V	-0.2		+0.2	µA
$\Delta V_{OUT}/I_{OUT}$	Load Regulation	V_{IN} = 3.3V, V_{OUT} = 3.8V, 0 to 2.5A Load		1		%/A
$\Delta V_{OUT}/V_{IN}$	Line Regulation	V_{IN} = 2.4V to V_{OUT}, I_{OUT} = 10mA		0.3		%/V
V_{OVP}	OUT Over-Voltage Protection Threshold	Hysteresis = 200mV	5.6	6.0	6.4	V
f_{OSC}	Oscillator Frequency		480	600	720	kHz
D_{MAX}	Maximum Duty Cycle			90		%
$t_{ON(MIN)}$	Minimum On-Time			80		ns
$R_{ON(PMOS)}$	High-Side P-Channel On-Resistance			70		mΩ
$R_{ON(NMOS)}$	Low-Side N-Channel On-Resistance			90		
I_{STRT}	Input Start-Up PMOS Inrush Current Limit	V_{OUT} + 0.5V < V_{IN}, R_{LOAD} = 1Ω	0.5	0.75		A
$I_{LIM(PMOS)}$	PMOS Linear Overload Current Limit	V_{OUT} = 0V		3.0		
I_{LIMPK}	Low-Side Peak Current Limit Threshold	R_{SET} = 75kΩ, T_A = 25°C	2.625	3.5	4.375	
		R_{SET} = 63.4kΩ, T_A = 25°C		4.0		
		R_{SET} = 1000kΩ, T_A = 25°C		0.6		
Enable, Power Ready and Start-Up Features						
$V_{EN(H)}$	Logic Input Threshold High for EN		1.4			V
$V_{EN(L)}$	Logic Input Threshold Low for EN				0.4	
I_{EN}	EN Input Current	V_{EN} = GND or 5.5V	-1.0		+1.0	µA
$V_{\overline{RDY}}$	Power Ready Threshold	FB Rising, Hysteresis = 10%		95		%
$R_{\overline{RDY}}$	$\overline{RDY}$ On-Resistance	V_{FB} = 0.62V, I_{SINK} = 10µA		2700		Ω
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold	Temperature Rising		150		°C
$T_{SD(HYS)}$	Over-Temperature Shutdown Hysteresis			15		

Typical Characteristics

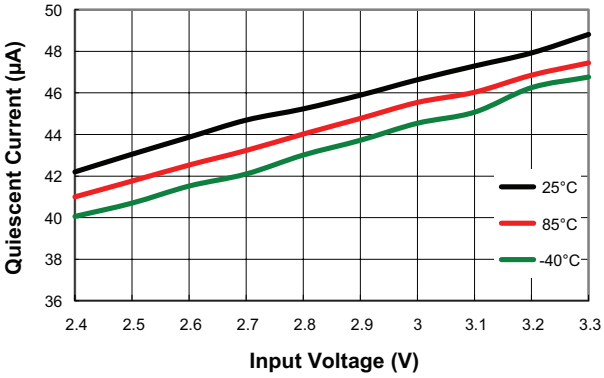
No Load Quiescent Current vs Input Voltage
(Close Loop,V_{OUT} = 3.8V)



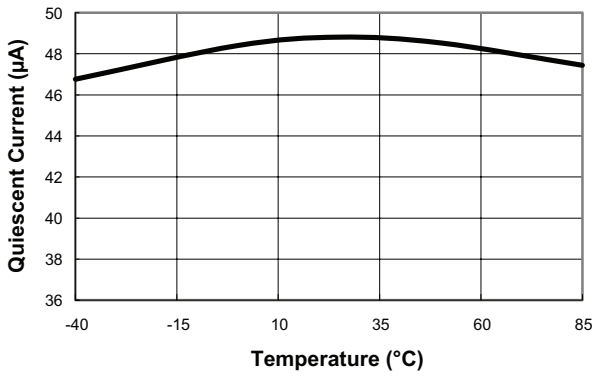
No Load Quiescent Current vs Temperture
(Close Loop,V_{IN} = 3.3V, V_{OUT} = 3.8V)



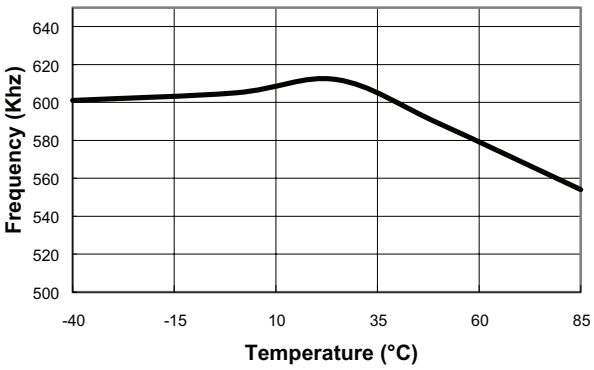
No Load Quiescent Current vs Input Voltage
(Open Loop)



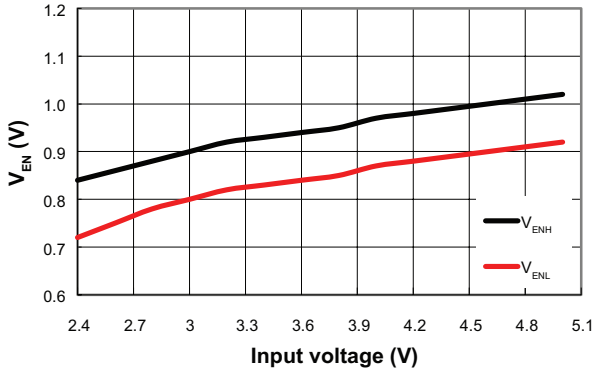
No Load Quiescent Current vs Temperature
(Open Loop, V_{IN} = 3.3V)



Frequency vs Temperature

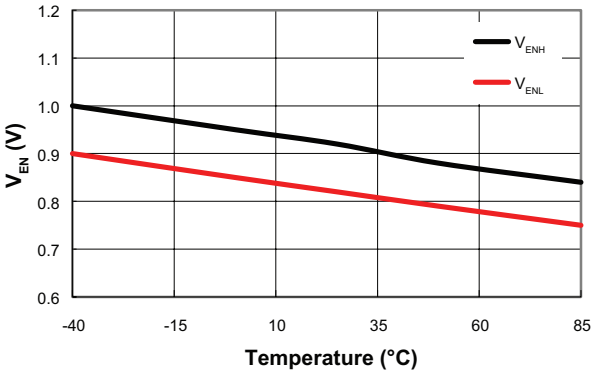


Enable Threshold vs Input Voltage

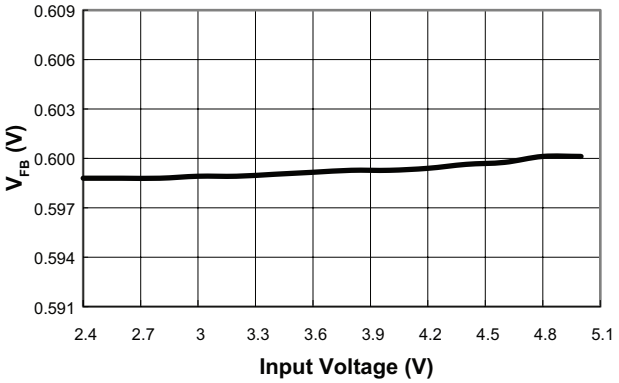


Typical Characteristics

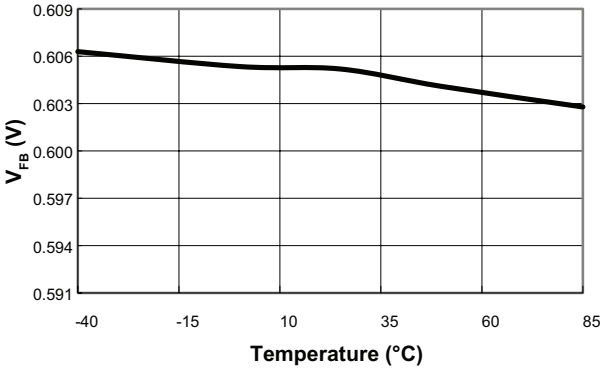
Enable Threshold vs Temperature



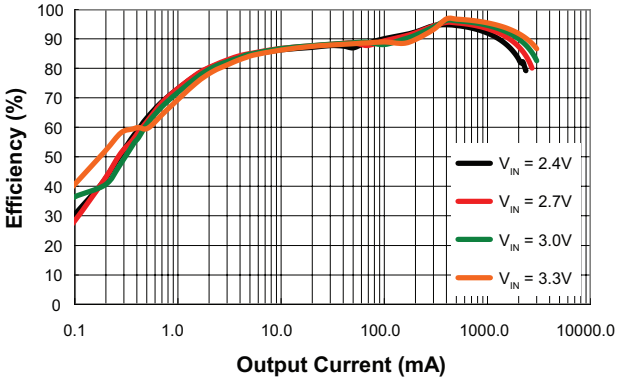
Feedback Voltage vs Input Voltage



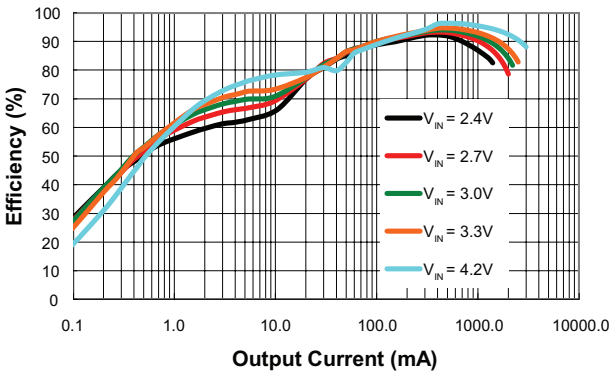
Feedback Voltage vs Temperature



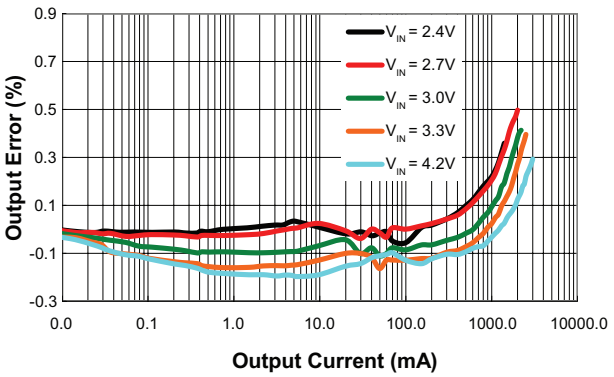
Efficiency
(L = 2.2µH, V_{OUT} = 3.8V)



Efficiency
(L = 2.2µH, V_{OUT} = 5.0V)

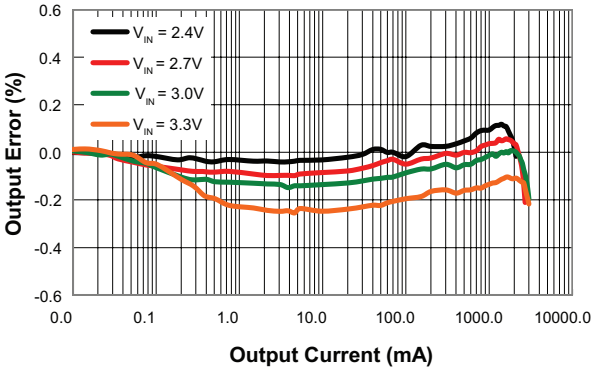


Load Regulation
(L = 2.2µH, V_{OUT} = 5.0V)

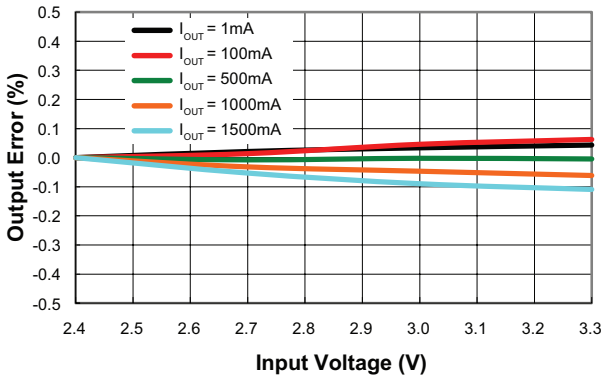


Typical Characteristics

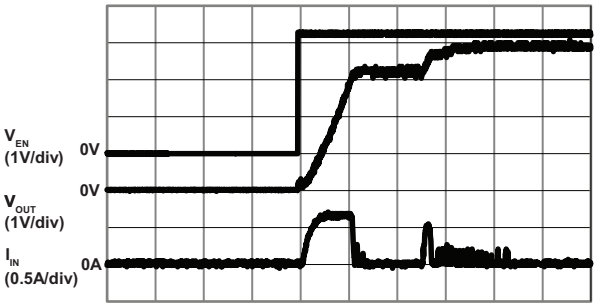
Load Regulation
($L = 2.2\mu H$, $V_{OUT} = 3.8V$)



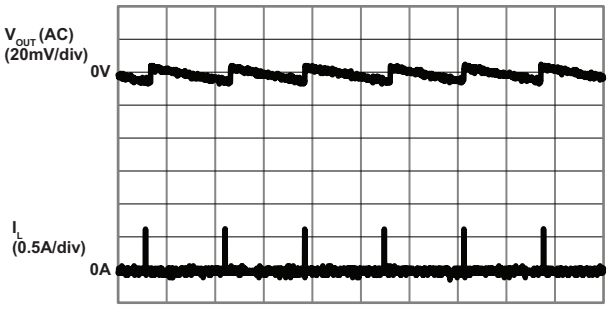
Line Regulation
($L = 2.2\mu H$, $V_{OUT} = 3.8V$)



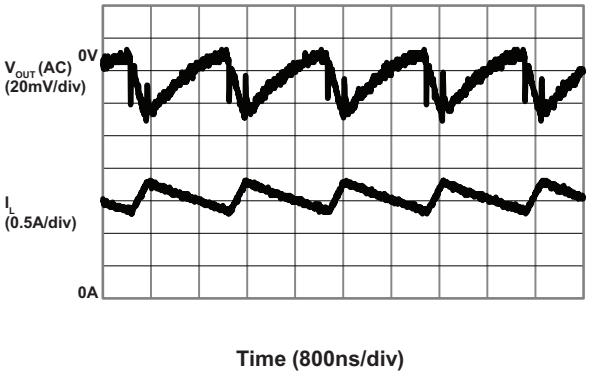
Soft Start
($V_{OUT} = 3.8V$; $V_{IN} = 3.3V$; $I_{OUT} = 0A$)



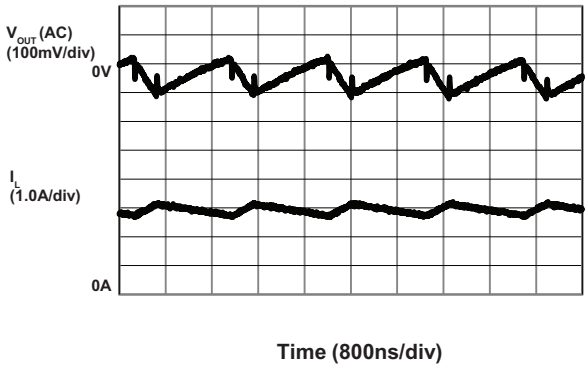
Output Voltage Ripple
($V_{IN} = 3.3V$; $V_{OUT} = 3.8V$; $I = 2.2\mu H$; $I_{OUT} = 0mA$)



Output Voltage Ripple
($V_{IN} = 3.3V$; $V_{OUT} = 3.8V$; $L = 2.2\mu H$; $I_{OUT} = 1A$)

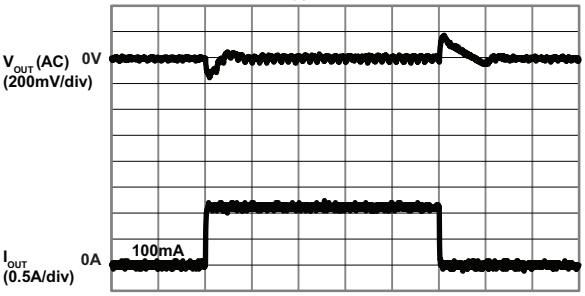


Output Voltage Ripple
($V_{IN} = 3.3V$; $V_{OUT} = 3.8V$; $L = 2.2\mu H$; $I_{OUT} = 2.5A$)



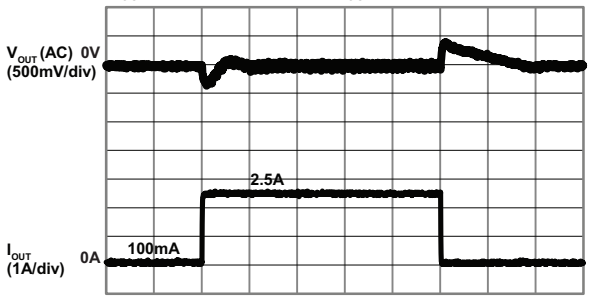
Typical Characteristics

Load Transient
(V_{OUT} = 3.8V; V_{IN} = 3.3V; I_{OUT} = 100mA to 1.2A;
L = 2.2µH; C_{OUT} = 22µF + 220µF)



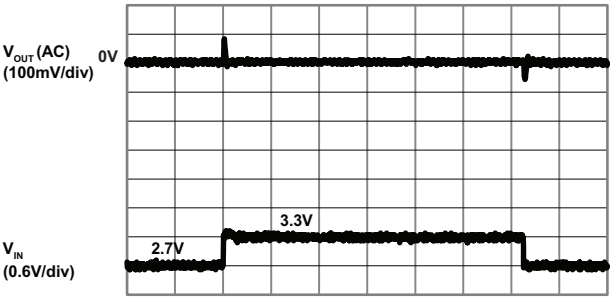
Time (400µs/div)

Load Transient
(V_{OUT} = 3.8V; V_{IN} = 3.3V; L = 2.2µH;
I_{OUT} = 100mA to 2.5A; C_{OUT} = 22µF + 220µF)



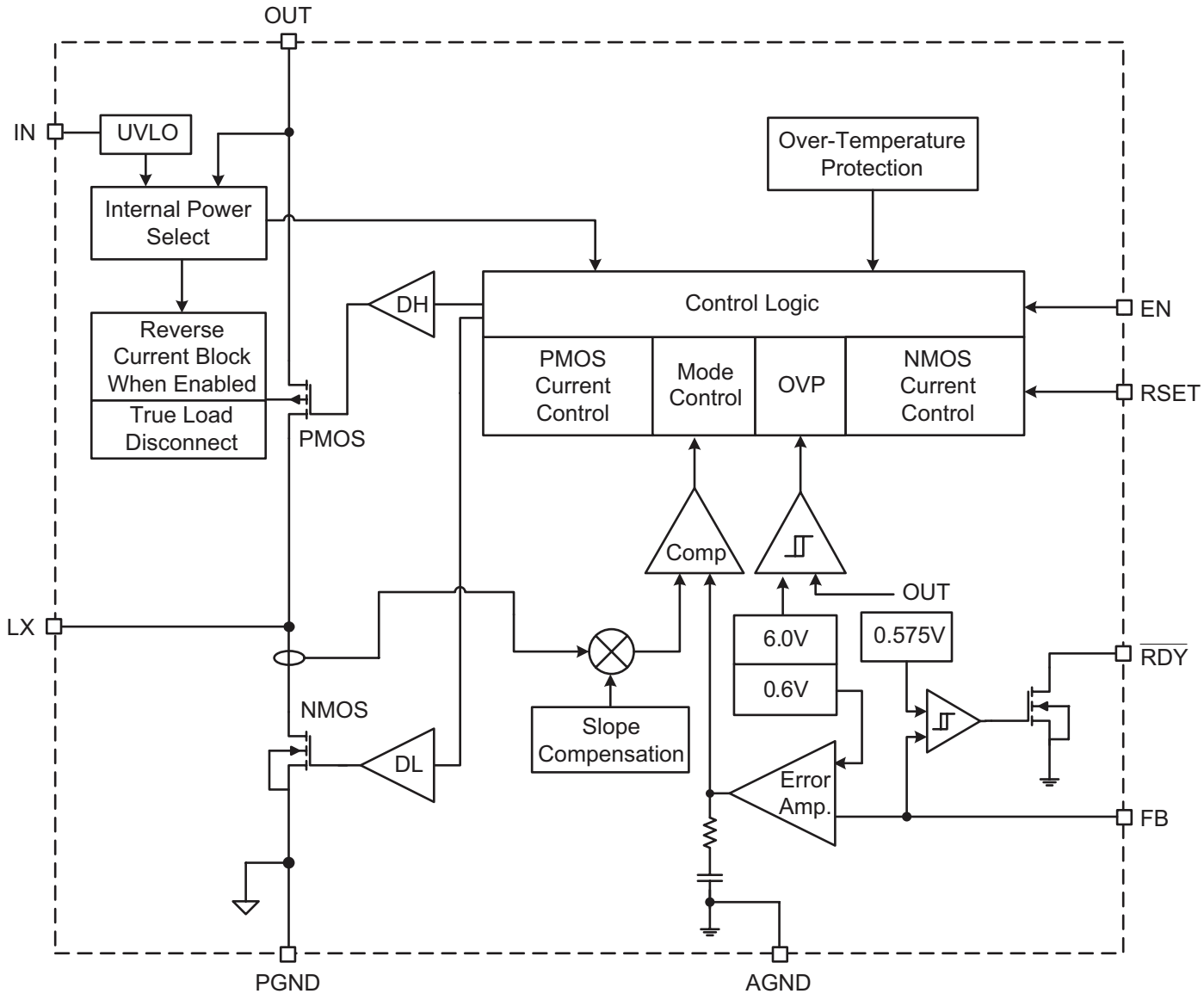
Time (400µs/div)

Line Transient Response
(V_{IN} = 2.7V to 3.3V; V_{OUT} = 3.8V; L = 2.2µH;
I_{OUT} = 100mA; C_{OUT}= 22µF)



Time (400µs/div)

Functional Block Diagram



Functional Description

The AAT2215 synchronous step-up converter is targeted for PC Card GSM/GPRS/3G and WiMax modem card applications. It includes a 0.75A start-up PMOS current limit to ensure fast, controlled power-up, a 3A overload PMOS current limit after startup, and a programmable peak NMOS step-up current limit up to 4A for continuous step-up operation within the PCMCIA specifications.

The 600kHz switching frequency of the AAT2215 facilitates output filter component size reduction for improved power density and reduced overall footprint. It also provides greater bandwidth and improved transient response over other lower frequency step-up converters. The compensation and feedback is integrated with only three external components (C_{IN}, C_{OUT}, L). Low $R_{DS(ON)}$ synchronous power switches provide high efficiency for heavy load conditions. Switching frequency modulation and low quiescent current maintains this high efficiency for light load mode condition. In addition to the improved efficiency, the synchronous step-up has the added performance advantage of true load disconnect during shutdown (<1µA shutdown current), reverse current blocking when enabled, inrush current limit, and short-circuit protection.

PWM Control Scheme with Low-Noise Light-Load

The AAT2215 is a fixed-frequency PWM peak current mode control step-up converter. For light load condition (70mA to 80mA and below), the converter stays in a variable frequency (Light Load) mode to reduce the dominant switching losses. In addition to Light Load operation, a zero current comparator blocks reverse current in the P-channel synchronous MOSFET, forcing DCM operation at light load. These controls, along with very low quiescent current, help to maintain high efficiency over the complete load range without increased output voltage ripple during light load conditions.

Shutdown and True Load Disconnect

A typical synchronous step-up (step-up) converter has a conduction path from the input to the output via the parasitic body diode of the P-channel MOSFET when the converter shuts down. The AAT2215 design a special power selection for the substrate to keep the parasitic body diode in off-state during shutdown and startup. This enables the AAT2215 to provide true load disconnect during shutdown and PMOS inrush current limit at startup.

During the initial PMOS linear mode start-up period, the start-up control circuitry is powered by the input supply pin. When the output voltage of the AAT2215 enters step-up mode ($V_{IN} \approx V_{OUT}$), the step-up control circuitry draws power directly from the output supply to ensure sufficient voltage head-room.

When EN is set to logic low, the step-up converter is forced into shutdown state with less than 1µA input current.

Soft-start and PMOS Current Limit Protection

Start-Up Inrush Current Protection

When initially powering up, the load disconnect feature allows the output voltage to be less than the input voltage. In order to avoid large surge current when the regulator is enabled, the AAT2215 operates the synchronous P-channel MOSFET in a current-limited linear mode to softly charge the large output capacitor. This linear start-up feature effectively limits the input current to 0.75A until the output voltage exceeds the input voltage. After V_{OUT} exceeds V_{IN}, the regulator switches the body diode connection and begins step-up operation.

Overload Current-Limit Protection

Once start-up is completed, ($\overline{RDY}$ is pulled low), the AAT2215 increases the PMOS overload current-limit threshold to 3A. If the output is overloaded, causing V_{OUT} to drop below V_{IN} by 210mV, the regulator will switch back to a linear operating mode. This activates the 3A PMOS overload current protection and the AAT2215 will reverse the body-diode connection. This effectively limits the output current under such fault conditions.

Combined with the thermal shutdown protection, the PMOS current-limit protects the regulator against overload and short-circuit fault conditions.

The overload current limit is fixed at 3A, and short-circuit protection also adopts this 3A current limit; the 3A current limit is not changed with R_{SET} value.

Programmable Peak NMOS Current-Limit

When the output voltage of the AAT2215 enters step-up mode ($V_{IN} < V_{OUT}$), the NMOS starts switching and the NMOS peak current-limit becomes active. During the inductor charge cycle, the low-side NMOS turns on and the AAT2215 monitors the current through the NMOS. If the current exceeds the current-limit threshold set by

the R_{SET} resistor, the regulator immediately turns off the low-side NMOS. The regulator limits the instantaneous peak inductor/NMOS current, so the current-limit threshold must be set high enough to support the desired output current.

Power Ready

To indicate the output voltage is in regulation, an active-low open-drain output pin ($\overline{RDY}$) pulls down when the feedback voltage is above 95% of the nominal regulation voltage level. $\overline{RDY}$ becomes a high-impedance output if the feedback voltage drops below 85% of the nominal regulation voltage level.

Over-Voltage Protection

The AAT2215's over-voltage protection function prevents the output voltage from exceeding the fixed 6V (typ) over-voltage point, which would exceed the absolute maximum rating of the regulator. If OUT exceeds 6V, the regulator will stop switching until the output voltage drops below 5.8V (200mV hysteresis) and FB is below its regulation threshold.

Thermal Shutdown

When the junction temperature exceeds the over-temperature threshold, the AAT2215 thermal protection circuitry shuts down the regulator. Thermal shutdown disables switching and PMOS current limit is functional to control the current flowing through to avoid any damage of the step-up converter. When the over-temperature fault condition is removed, the step-up recovers regulation automatically.

Application Information

R_{SET} Selection for Programmable Current Limit

The current limit of the internal low-side NMOS power switch is programmable from 0.6A to 4.0A by an external resistor connected from RSET to ground.

When the inductor's peak current reaches the current limit, the $\overline{RDY}$ indicator is pulled high. Table 1 gives standard 1% standard metal film resistor example values for the peak NMOS current-limit programming.

R_{SET} (kΩ)	I_{LIMIT} (A)
63.4	4
75.0	3.48
82.0	3.1
100.0	2.6
118.0	2.15
150.0	1.75
180.0	1.52
300.0	1.02
432.0	0.82
1000.0	0.6

Table 1: Examples of 1% Standard Resistor Value of R_{SET}

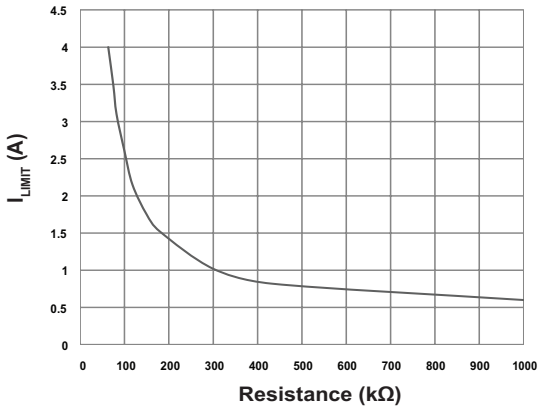


Figure 1: I_{LIMIT} vs R_{SET}

Output Voltage Programming

The output voltage of the AAT2215 may be programmed from 3.0V to 5.5V with an external resistive voltage divider. Resistors R1 and R2 in Figure 1 program the output voltage as shown by the following equation:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2$$

where 0.6V is the feedback reference voltage (V_{REF}). To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the suggested value for R2 is 100kΩ. Table 2 summarizes the resistor values with R2 set to 100kΩ for good noise immunity and 6µA increased load current and gives some 1% standard metal film resistor values for R1 at different output voltage settings.

V_{OUT}(V)	R2 = 100kΩ R1 = (kΩ)
3	400
3.3	450
3.6	500
3.8	536
4.2	600
4.5	650
5	733
5.5	816

Table 2: Resistor Selection for Output Voltage

Inductor Selection

The AAT2215 is designed to operate with a 2.2µH inductor for all input/output voltage combinations. For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor.

Input Capacitor

Select a low ESR ceramic capacitor with a value of at least 10µF as the input capacitor. Place the input capacitor as close to the IN and PGND pins as possible in order to minimize the stray resistance from the converter to the input power source.

Output Capacitor

The output capacitor provides energy to the load when the high-side MOSFET is switched off. The output capacitance together with the boost switching frequency, duty cycle, and load current value determine the capacitive output voltage ripple when the boost operation is in the continuous PWM state.

$$\Delta V_{OUT} = \left(\frac{I_{OUT} \cdot D}{C_{OUT} \cdot f_{SW}}\right)$$

where D is the duty ratio of low-side MOSFET turn-on time divided by the switching period. It is calculated using the equation:

$$D = 1 - \left(\frac{V_{IN}}{V_{OUT}}\right)$$

The output capacitor's ESR increases the output ripple by $I_{OUT} \cdot ESR$. The total output ripple is:

$$\Delta V_{OUT} = (I_{OUT} \cdot ESR) + \left(\frac{I_{OUT} \cdot D}{C_{OUT} \cdot f_{SW}}\right)$$

So the minimum recommended output capacitor value may be determined by:

$$C_{OUT} \geq \left(\frac{I_{OUT} \cdot D}{\Delta V_{OUT} - (I_{OUT} \cdot ESR)}\right) \cdot \frac{1}{f_{SW}}$$

High Load Pulse Application

Together with a large value output capacitor or supercap, the AAT2215 can support a higher load pulse in lower input current limited applications such as GSM burst mode in WCDMA, Edge, GPRS and TD-SCDMA applications. The large capacitance is determined by NMOS peak current limit, inductor current ripple, V_{IN}, V_{OUT}, load pulse high current level and elapsed time. The capacitor value can be calculated using the following three steps as follows:

First calculate the AAT2215's load-on current from the expected I_{LIM}. Assume the input current equals I_{LIM} because the inductor current ripple is low enough when compared to the input current:

$$I_{OUT\_BOOST} = \frac{V_{IN} \cdot I_{LIM} \cdot \eta}{V_{OUT}}$$

Second, calculate the maximum current the large capacitor C_{OUT} should provide:

$$I_{COUT} = I_{LOAD\_PEAK} - I_{OUT\_BOOST}$$

Finally, derive the C_{OUT} at a certain load-on period T_{ON}:

$$C_{OUT} = \frac{I_{COUT} \cdot T_{ON}}{\Delta V_{OUT}}$$

To consider the real tantalum capacitor having 20% tolerance, the selected capacitance should be 20% higher than the calculated value. Example: A 2.0A, 217Hz 12.5% duty cycle load pulse is applied on 3.8V V_{OUT} at 3.3V V_{IN}. An input peak current limit of 2.4A and a VOUT drop of less than 450mV are required. Under these conditions, with 89% efficiency, the AAT2215's output current is

$$I_{OUT\_BOOST} = \frac{3.3 \cdot 2.4 \cdot 89\%}{3.8} = 1.86A$$

The maximum current necessary for the large capacitor value is:

$$I_{COUT} = 2.0 - 1.86 = 0.14A$$

T_{ON} is 577µs for a 217Hz 12.5% duty cycle load pulse. Considering 20% capacitance tolerance, the minimum capacitance should be 220µF. Figure 2 shows the AAT2215 operating waveform under a 2.0A 577µs load pulse with 220µF tantalum capacitor as C_{OUT}, as well as a 22µF ceramic capacitor to closely filter the output voltage.

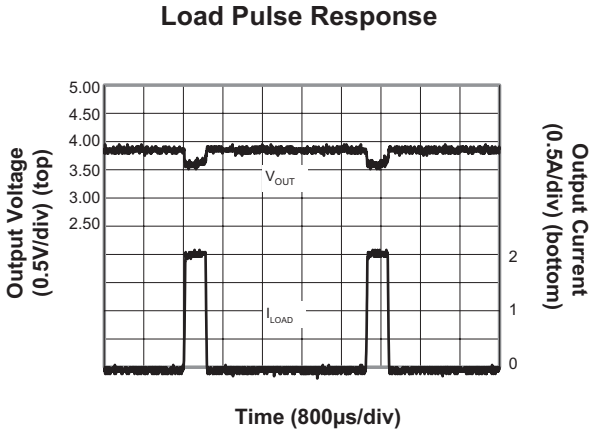


Figure 2: AAT2215 Operation Waveform When 2.0A 217Hz 577µs Load Pulse is Applied.

Layout Guidance

For best performance of the AAT2215, the following guidelines should be followed when designing the PCB layout:

1. Make the power trace as short and wide as possible, including the input/output power lines and switching node, etc.
2. Connect the analog and power grounds together with a single short line and connect all low current loop grounds to analog ground to decrease the power ground noise on the analog ground and achieve better load regulation.
3. For good power dissipation, connect the exposed pad under the package to the top and bottom ground planes by PCB pads.

Schematic and Layout

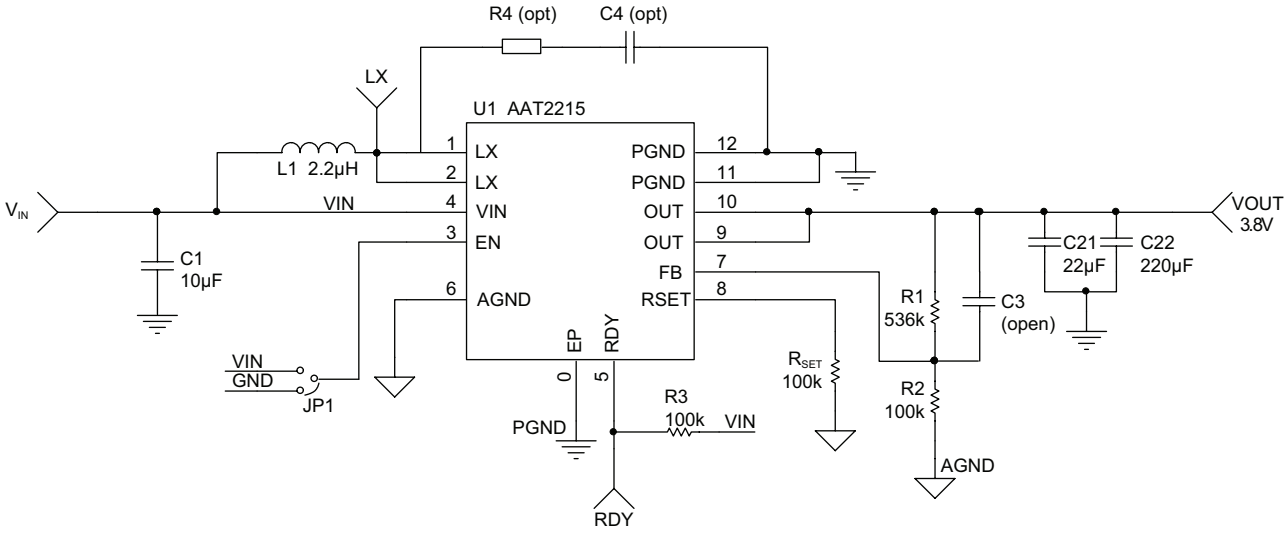


Figure 3: AAT2215 Evaluation Board Schematic.

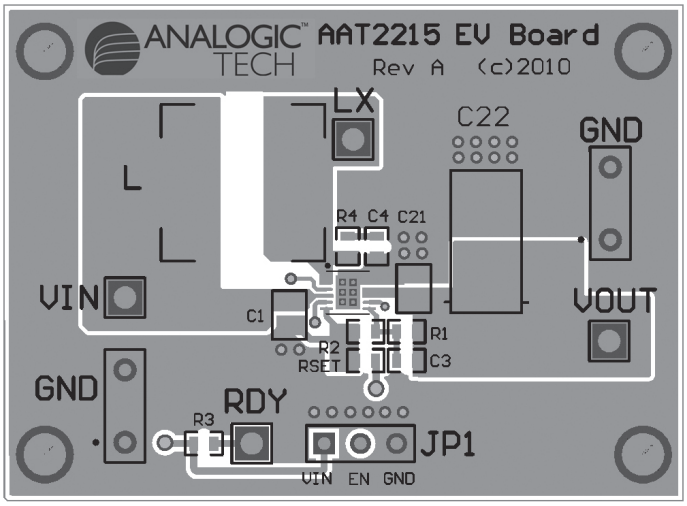


Figure 4: AAT2215 Evaluation Board Top Side Layout.

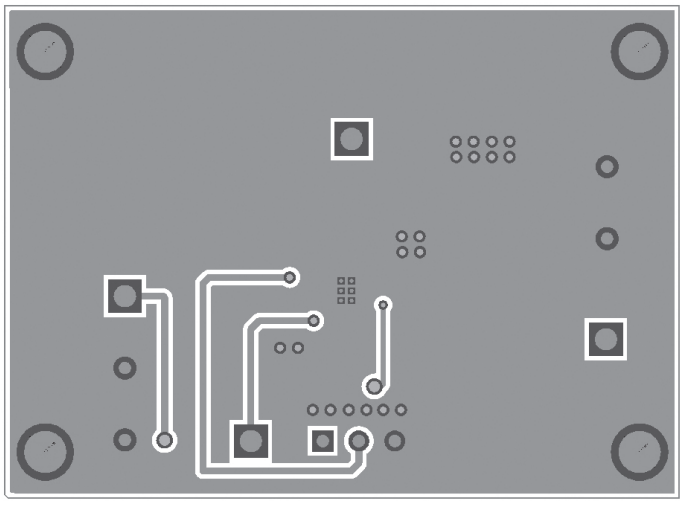


Figure 5: AAT2215 Evaluation Board Bottom Side Layout.

Part Number	Inductance (µH)	Max DC Current (A)	DCR (mΩ)	Size LxWxH (mm)	Type
CHRH103RNP-2R2NC	2.2	6.7	20	10x10x2.8	Shielded
CDRH103RNP-3R3NC	3.3	5.5	21	10x10x2.8	Shielded
7440650033	3.3	4.7	20	10x10x2.8	Shielded
LQH6PPN3R3N43	3.3	4.5	16	6x6x4.3	Shielded

Table 3: Surface Mount Inductors.

Part Number	Description	Manufacturer
AAT2215IWP-0.6	High Current Step-Up Converter with Adjustable Current Limit	AnalogicTech
RC0603FR-07536KL	Res 536kΩ 1/10W 1% 0603 SMD	Yageo
RC0603FR-07100KL	Res 100kΩ 1/10W 1% 0603 SMD	
RC0603FR-07100KL	Res 100kΩ 1/10W 1% 0603 SMD	
RC0603FR-07100KL	Res 100kΩ 1/10W 1% 0603 SMD	
GRM21BR61C106K	Cap Ceramic 10µF 0805 X5R 16V 10%	Murata
GRM21BR60J226M	Cap Ceramic 22µF 0805 X5R 6.3V 20%	
TPSY227M006R0150	Cap Tan 220µF case 6.3V 20%	AVX
CDRH103RNP-2R2NC	Inductor 2.2µH 6.7A SMD	Sumida

Table 4: AAT2215 Evaluation Board Bill of Materials.

SwitchReg™ *High Current Synchronous Step-Up Regulator with Programmable Current Limit*

Ordering Information

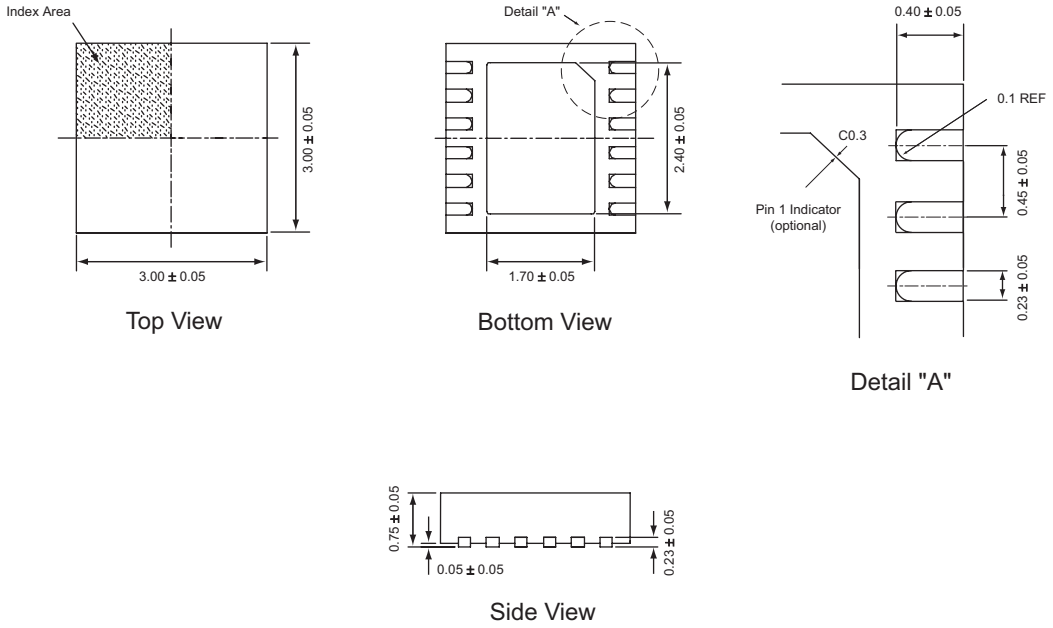
Package	Marking[1]	Part Number (Tape and Reel)[2]
TDFN33-12	P5XYY	**AAT2215IWP -T1**

Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/aboutus/quality.php.

Package Information[3]

TDFN33-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

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