

TOSHIBA Photocoupler GaAlAs Ired & Photo IC

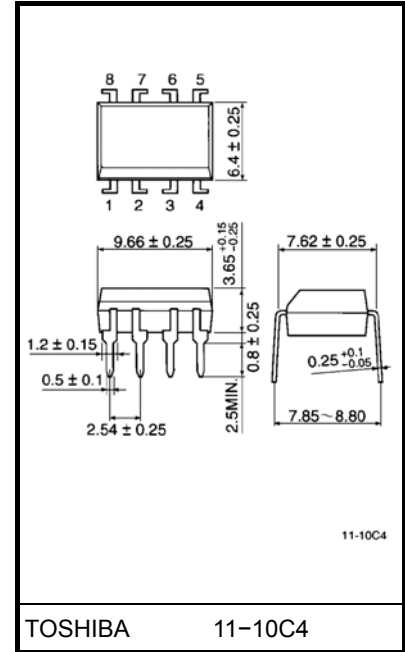
# 6N135, 6N136

- Digital Logic Isolation.
- Line Receiver.
- Power Supply Control
- Switching Power Supply
- Transistor Inverter

The TOSHIBA 6N135 and 6N136 consists of a high emitting diode and a one chip photo diode-transistor. Each unit is 8-lead DIP package.

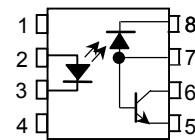
- Isolation voltage: 2500V<sub>rms</sub> (min.)
- High speed:  $t_{pHL}, t_{pLH} = 0.5\mu s$  (typ.) ( $R_L = 1.9k\Omega$ )
- TTL compatible
- If base pin is open, output signal will be noisy by environmental condition. For this base, TLP550 is suitable
- UL recognized: UL1577, file no. E67349

Unit in mm

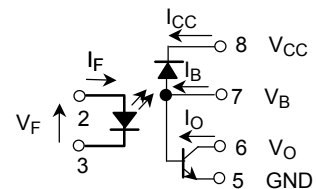


Weight: 0.54 g (typ.)

## Pin Configurations



- 1 : N.C.
- 2 : ANODE
- 3 : CATHODE
- 4 : N.C.
- 5 : EMITTER
- 6 : COLLECTOR
- 7 : BASE, ANODE
- 8 : CATHODE



## Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (Note 1)	$I_F$	25	mA
	Pulse forward current (Note 2)	$I_{FP}$	50	mA
	Total pulse forward current (Note 3)	$I_{FPT}$	1	A
	Reverse voltage	$V_R$	5	V
	Diode power dissipation (Note 4)	$P_D$	45	mW
Detector	Output current	$I_O$	8	mA
	Peak output current	$I_{OP}$	16	mA
	Emitter-base reverse voltage (pin 5-7)	$V_{EB}$	5	V
	Supply voltage	$V_{CC}$	-0.5~15	V
	Output voltage	$V_O$	-0.5~15	V
	Base current (pin 7)	$I_B$	5	mA
	Output power dissipation (Note 5)	$P_o$	100	mW
Operating temperature range		$T_{opr}$	-55~100	°C
Storage temperature range		$T_{stg}$	-55~125	°C
Lead solder temperature (10s) (Note 6)		$T_{sol}$	260	°C
Isolation voltage (Note 7)		$BV_S$	2500	$V_{rms}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) Derate 0.8mA above 70°C.

(Note 2) 50% duty cycle, 1ms pulse width.  
Derate 1.6mA / °C above 70°C.

(Note 3) Pulse width 1μs, 300pps.

(Note 4) Derate 0.9mW / °C above 70°C.

(Note 5) Derate 2mW / °C above 70°C.

(Note 6) Soldering portion of lead: Up to 2mm from the body of the device.

(Note 7) R.H. ≤ 60%, AC / 1min.

## Electrical Characteristics Over Recommended Temperature (Ta = 0°C~70°C unless otherwise noted)

Characteristic		Symbol	Test Condition	Min.	(**)Typ.	Max.	Unit
Current transfer ratio	6N135	CTR	$I_F = 16\text{mA}, V_O = 0.4\text{V}$ $V_{CC} = 4.5\text{V}, T_a = 25^\circ\text{C}$ (Note 8)	7	18	—	%
	6N136			19	24	—	%
	6N135	CTR	$I_F = 16\text{mA}, V_O = 0.5\text{V}$ $V_{CC} = 4.5\text{V}$ (Note 1)	5	13	—	%
	6N136			15	21	—	%
Logic low output voltage	6N135	V <sub>OL</sub>	$I_F = 16\text{mA}, I_O = 1.1\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
	6N136		$I_F = 16\text{mA}, I_O = 2.4\text{mA}$ $V_{CC} = 4.5\text{V}$	—	0.1	0.4	V
Logic high output current			$I_F = 0\text{mA}, V_O = V_{CC} = 5.5\text{V}$ $T_a = 25^\circ\text{C}$	—	3	500	nA
			$I_F = 0\text{mA}, V_O = V_{CC} = 15\text{V}$ $T_a = 25^\circ\text{C}$	—	0.1	1	μA
			$I_F = 0\text{mA}, V_O = V_{CC} = 15\text{V}$	—	—	50	μA
Logic low supply current		I <sub>CCL</sub>	$I_F = 16\text{mA}, V_O = \text{open}$ $V_{CC} = 15\text{V}$	—	40	—	μA
Logic high supply current		I <sub>CCH</sub>	$I_F = 0\text{mA}, V_O = \text{open}$ $V_{CC} = 15\text{V}, T_a = 25^\circ\text{C}$	—	0.01	1	μA
		I <sub>CCH</sub>	$I_F = 0\text{mA}, V_O = \text{open}$ $V_{CC} = 15\text{V}$	—	—	2	μA
Input forward voltage		V <sub>F</sub>	$I_F = 16\text{mA}, T_a = 25^\circ\text{C}$	—	1.65	1.7	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta T_a$	$I_F = 16\text{mA}$	—	-1.9	—	mV / °C
Input reverse breakdown voltage		BV <sub>R</sub>	$I_R = 10\mu\text{A}, T_a = 25^\circ\text{C}$	5	—	—	V
Input capacitance		C <sub>IN</sub>	$f = 1\text{MHz}, V_F = 0$	—	60	—	pF
Resistance (input-output)		R <sub>I-O</sub>	$V_{I-O} = 500\text{V}$ R.H. ≤ 60% (Note 9)	—	10 <sup>12</sup>	—	Ω
Capacitance (input-output)		C <sub>I-O</sub>	$f = 1\text{MHz}$ (Note 9)	—	0.6	—	pF
Transistor DC current gain		h <sub>FE</sub>	$V_O = 5\text{V}, I_O = 3\text{mA}$	—	80	—	—

(\*\*) All typicals at Ta = 25°C

## Switching Specifications

(unless otherwise specified.  $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ ,  $I_F = 16\text{mA}$ )

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit	
Propagation delay time to logic low at output	6N135	$t_{pHL}$	1	$R_L = 4.1\text{k}\Omega$	—	0.2	1.5	$\mu\text{s}$
	6N136			$R_L = 1.9\text{k}\Omega$	—	0.2	0.8	$\mu\text{s}$
Propagation delay time to logic high at output	6N135	$t_{pLH}$	1	$R_L = 4.1\text{k}\Omega$	—	1.0	1.5	$\mu\text{s}$
	6N136			$R_L = 1.9\text{k}\Omega$	—	0.5	0.8	$\mu\text{s}$
Common mode transient immunity at logic high level output (Note 10)	6N135	$CM_H$	2	$I_F = 0\text{mA}$ $V_{CM} = 10V_{p-p}$ $R_L = 4.1\text{k}\Omega$	—	1000	—	$V / \mu\text{s}$
	6N136			$I_F = 0\text{mA}$ $V_{CM} = 10V_{p-p}$ $R_L = 1.9\text{k}\Omega$	—	1000	—	$V / \mu\text{s}$
Common mode transient immunity at logic low level output (Note 10)	6N135	$CM_L$	2	$V_{CM} = 10V_{p-p}$ $R_L = 4.1\text{k}\Omega$ $I_F = 16\text{mA}$	—	-1000	—	$V / \mu\text{s}$
	6N136			$V_{CM} = 10V_{p-p}$ $R_L = 1.9\text{k}\Omega$ $I_F = 16\text{mA}$	—	-1000	—	$V / \mu\text{s}$
Bandwidth (Note 11)	BW	—	$R_L = 100\Omega$	—	2	—	MHz	

(Note 8) DC current transfer ratio is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.

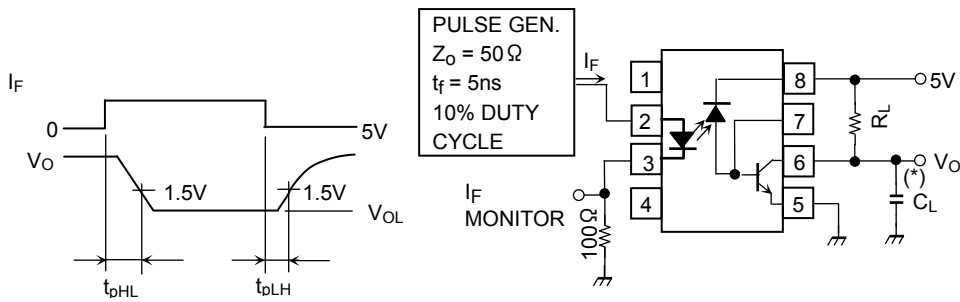
(Note 9) Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

(Note 10) Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{CM} / dt$  on the leading edge of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0\text{V}$ ).

Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{CM} / dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8\text{V}$ ).

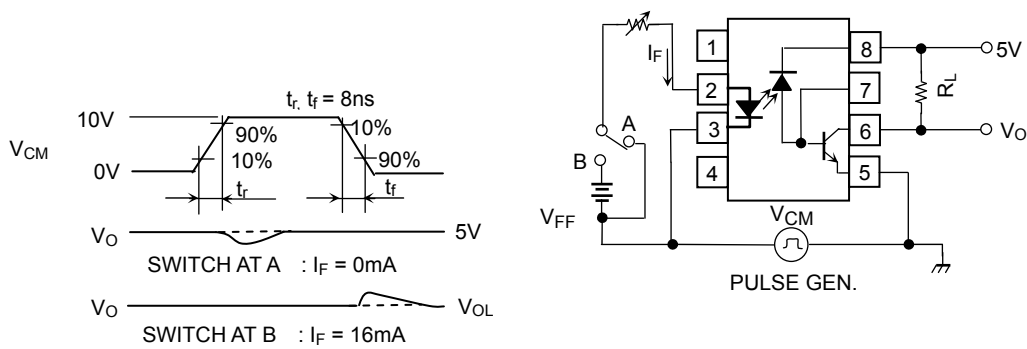
(Note 11) The frequency at which the AC output voltage is 3dB below the low frequency asymptote.

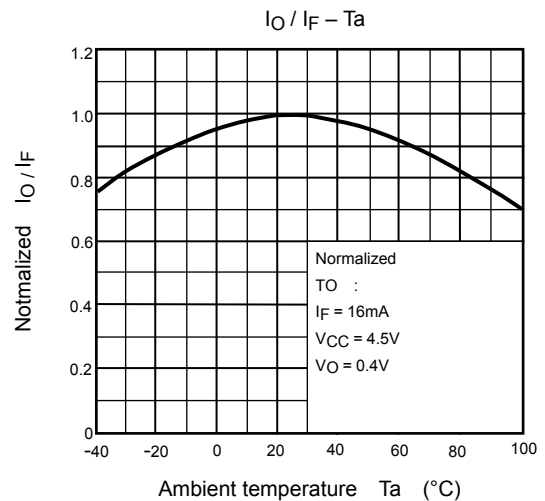
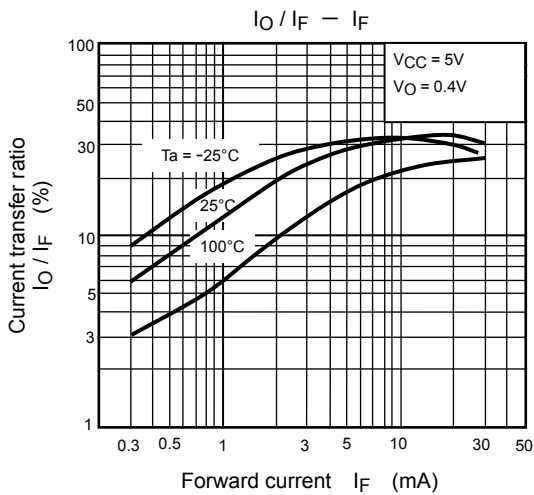
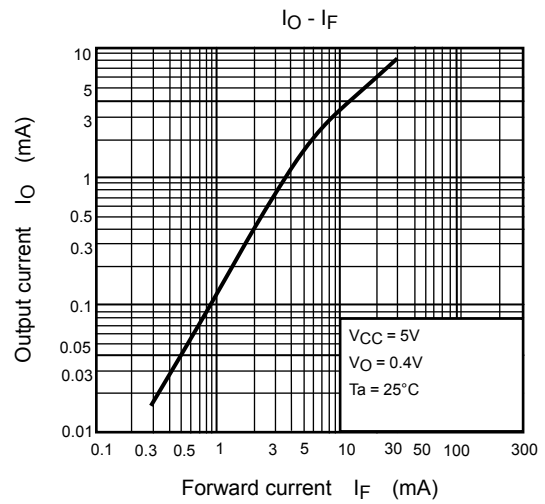
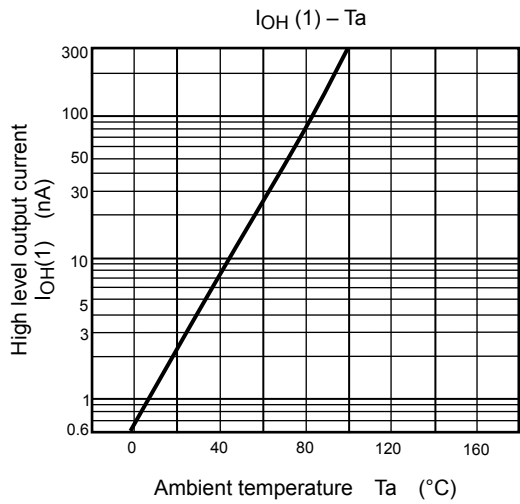
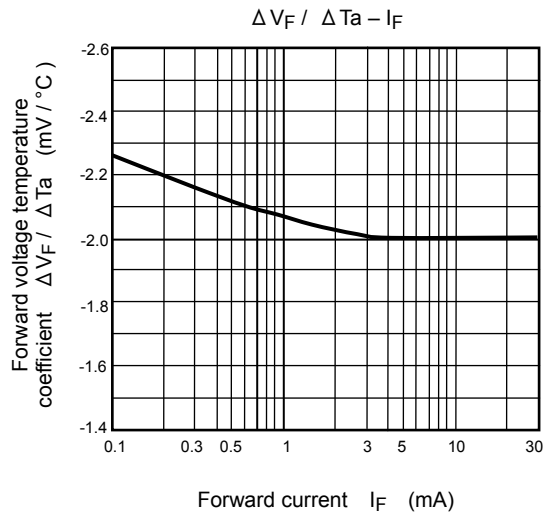
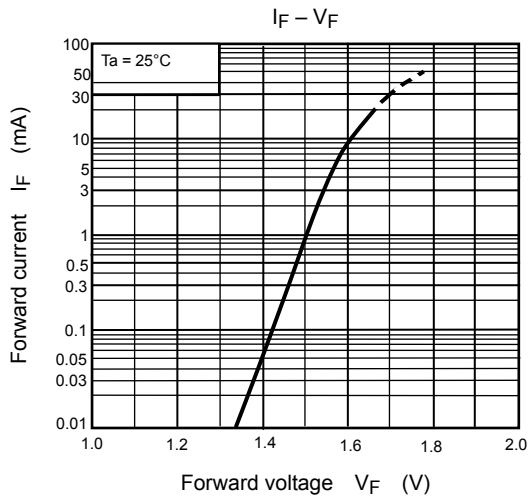
**Test Circuit 1.**

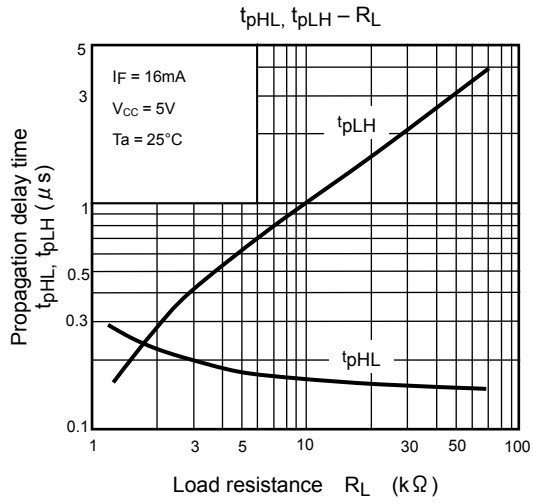
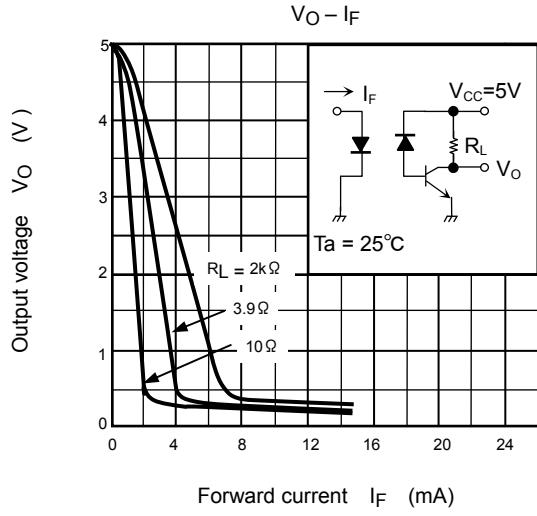
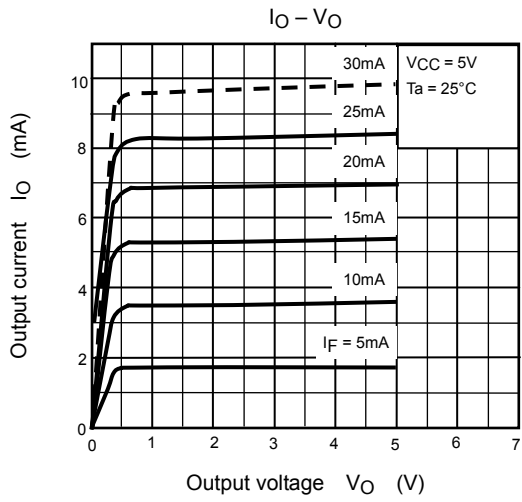


(\*)  $C_L$  is approximately 15pF which includes probe and stray wiring capacitance.

**Test Circuit 2.**







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