

TOSHIBA Multi-Chip Device
Silicon P-Channel MOS Type (U-MOS II) + N-Channel MOS Type (Planer)

SSM6E01TU

Load Switch Applications

- P-channel MOSFET and N-channel MOSFET incorporated into one package.
- Low power dissipation due to P-channel MOSFET that features low RDS (ON) and low-voltage operation

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	-12	V
Gate-Source voltage		V_{GSS}	±12	V
Drain current	DC	I_D	-1.0	A
	Pulse	I_{DP} (Note 2)	-2.0	

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	20	V
Gate-Source voltage		V_{GSS}	10	V
Drain current	DC	I_D	0.05	A
	Pulse	I_{DP} (Note 2)	0.2	

Absolute Maximum Ratings (Q1, Q2 common) (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain power dissipation	P_D (Note 1)	0.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	-55 to 150	°C

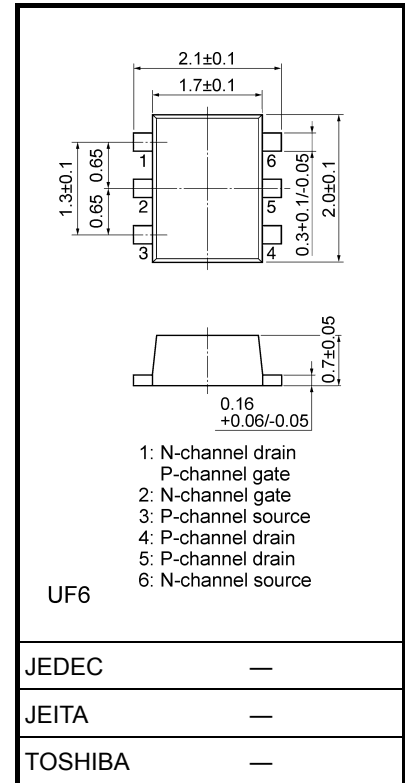
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 t, Cu pad: 645 mm²)

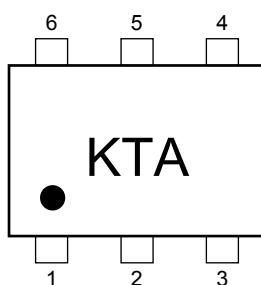
Note 2: Pulse width limited by maximum channel temperature.

Unit: mm

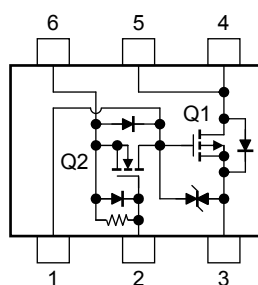


Weight: 7.0 mg (typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

This product has a MOS structure and is sensitive to electrostatic discharge. When handling individual devices (that have not yet been mounted on a PCB), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, containers and other objects which may come into direct contact with devices should be made of anti-static materials.

Thermal resistance $R_{th(j-a)}$ and drain power dissipation P_D vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration.

Q1 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage (diode)	V_{DSF}	$I_{DR} = 1.0 \text{ A}$, $V_{GS} = 0 \text{ V}$	—	—	1.2	V
Gate leakage current	I_{GSS}	$V_{GS} = \pm 10 \text{ V}$, $V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}$, $V_{GS} = 0$	-12	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = -12 \text{ V}$, $V_{GS} = 0$	—	—	-1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}$, $I_D = -0.1 \text{ mA}$	-0.4	—	-1.1	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}$, $I_D = -0.5 \text{ A}$ (Note 3)	1.3	2.5	—	S
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = -0.5 \text{ A}$, $V_{GS} = -4 \text{ V}$ (Note 3)	—	125	160	m Ω
		$I_D = -0.5 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ (Note 3)	—	180	240	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$	—	310	—	pF

Note 3: Pulse test

Q2 Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0$	—	—	15	μA
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}$, $V_{GS} = 0$	20	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = 20 \text{ V}$, $V_{GS} = 0$	—	—	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 3 \text{ V}$, $I_D = 0.1 \text{ mA}$	0.7	—	1.3	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}$, $I_D = 10 \text{ mA}$ (Note 3)	25	50	—	mS
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = 10 \text{ mA}$, $V_{GS} = 2.5 \text{ V}$ (Note 3)	—	4	10	Ω
Input capacitance	C_{iss}	$V_{DS} = 3 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$	—	11	—	pF
Gate-Source resistance	R_{GS}	$V_{GS} = 0 \text{ to } 10 \text{ V}$	0.7	1.0	1.3	M Ω

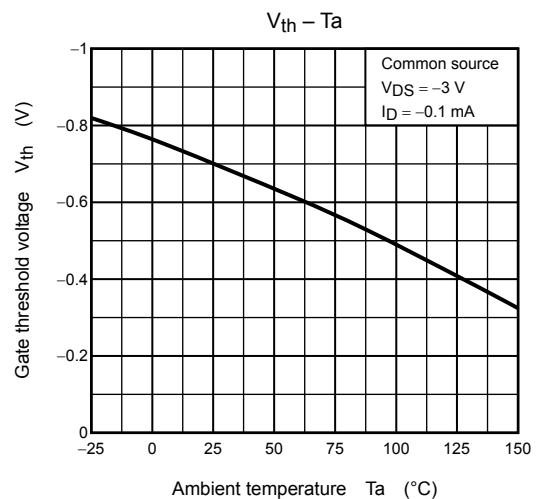
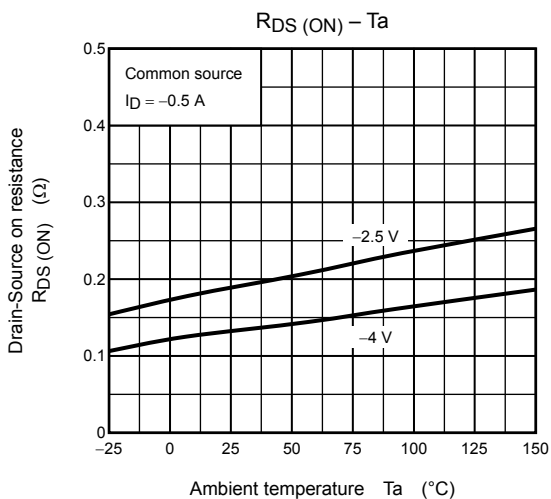
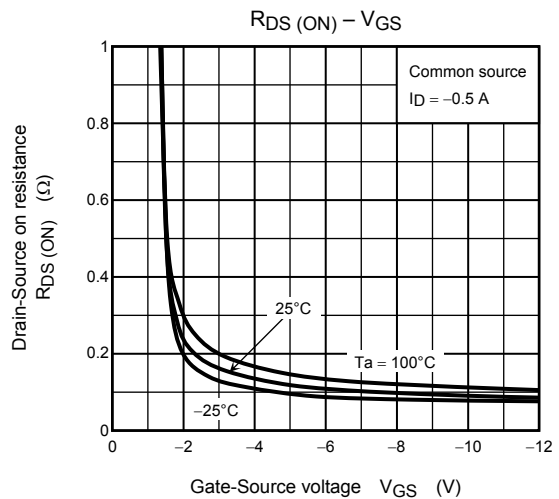
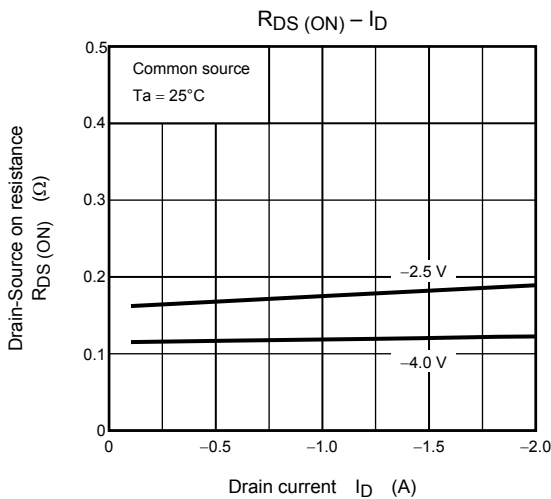
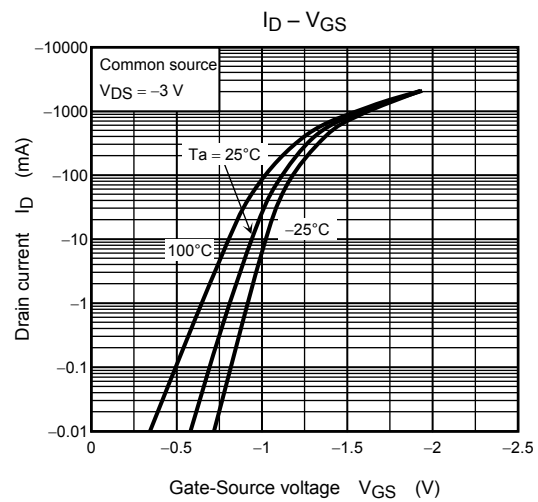
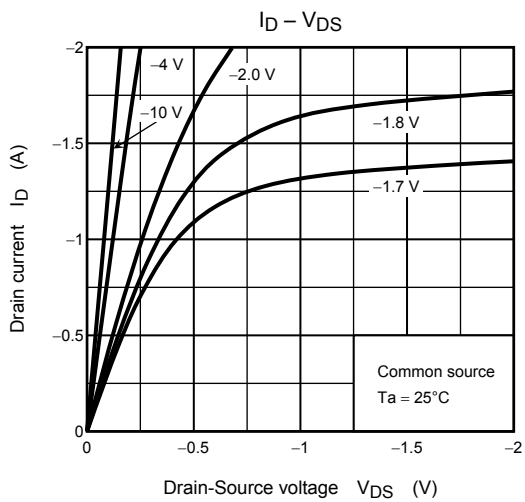
Note 3: Pulse test

Precaution

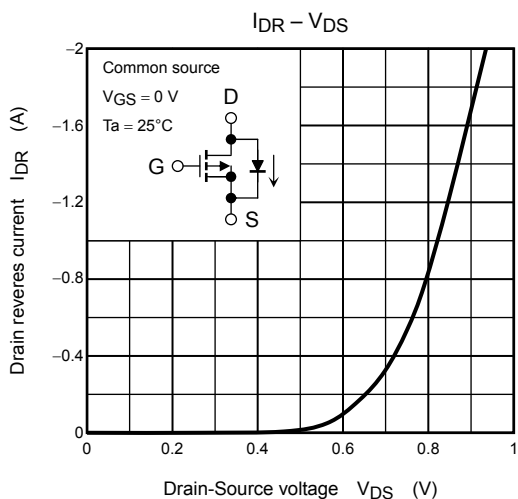
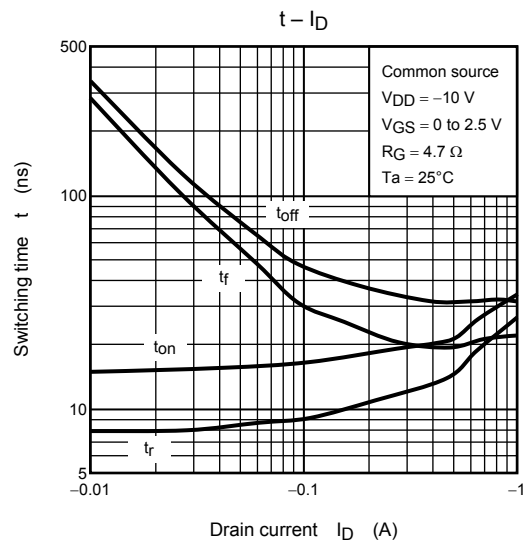
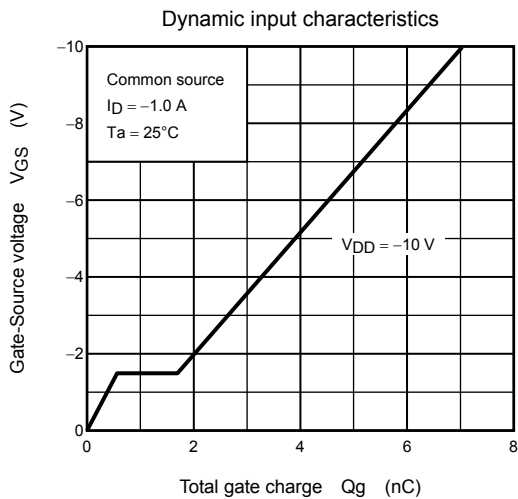
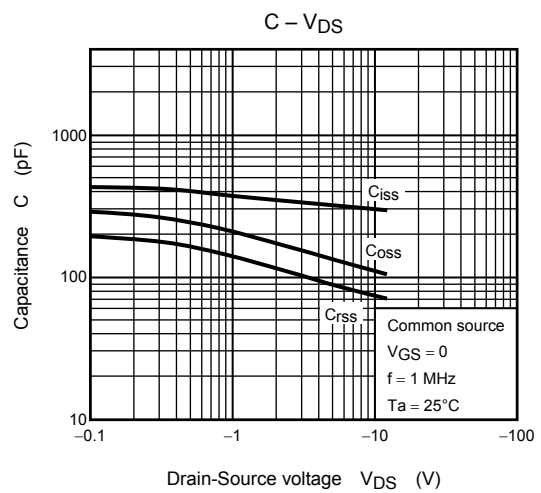
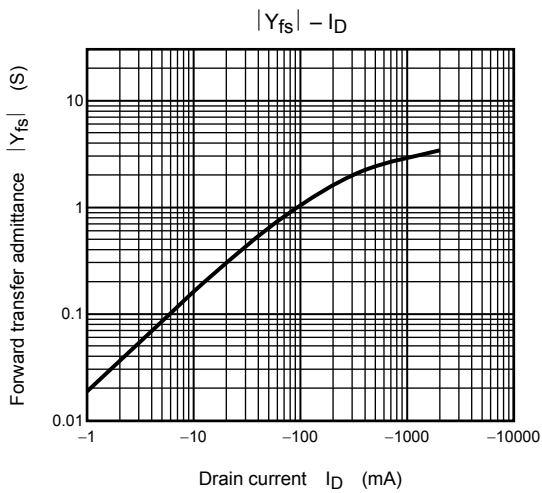
V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = \pm 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.

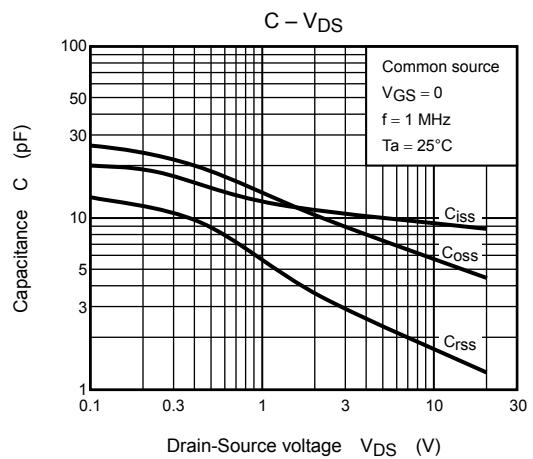
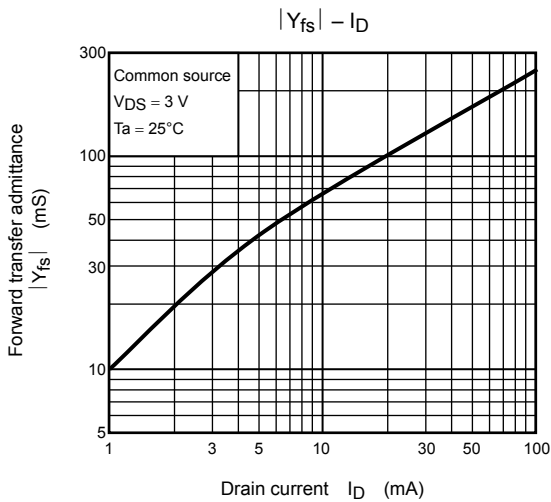
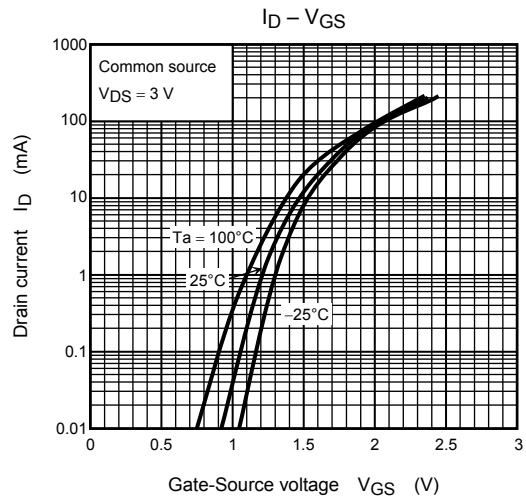
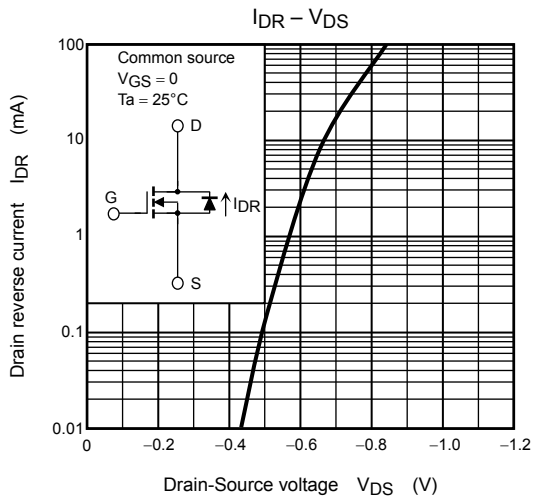
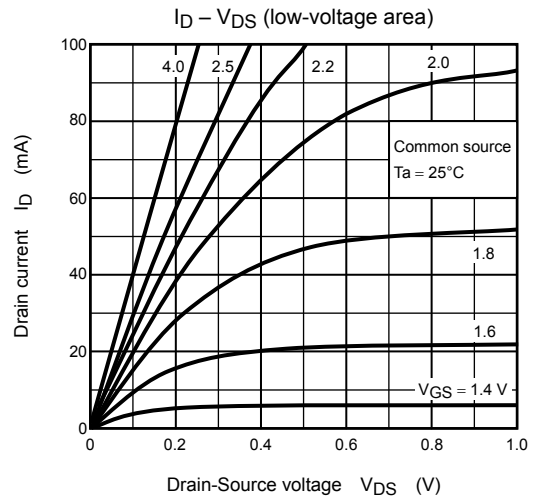
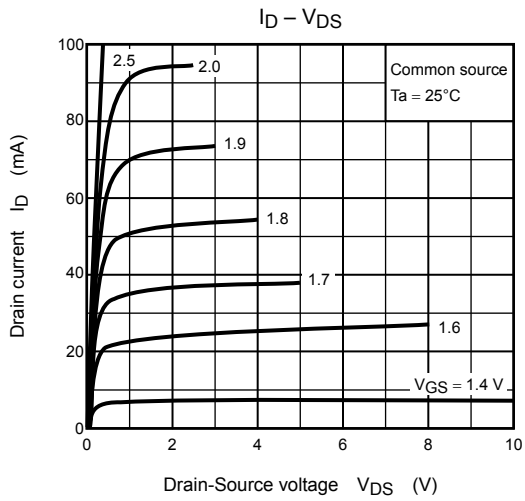
Q1 (Pch MOSFET)



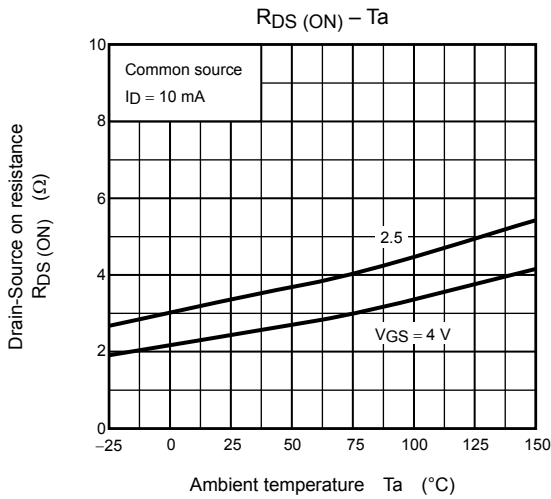
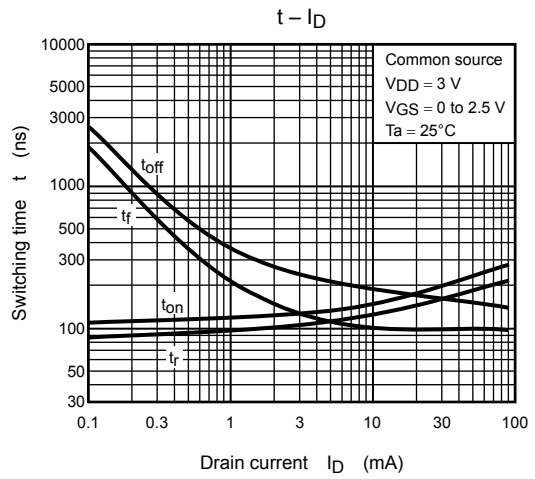
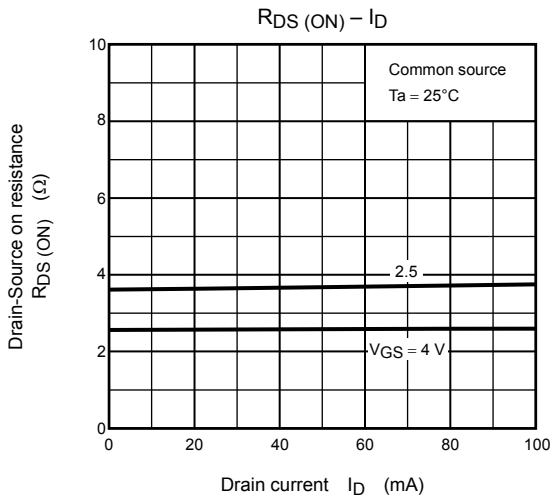
Q1 (Pch MOSFET)



Q2 (Nch MOSFET)



Q2 (Nch MOSFET)



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