MOSFETs Silicon P-Channel MOS (U-MOSⅥ)

TJ40S04M3L

1. Applications

- Automotive
- Motor Drivers
- DC-DC Converters
- Switching Voltage Regulators

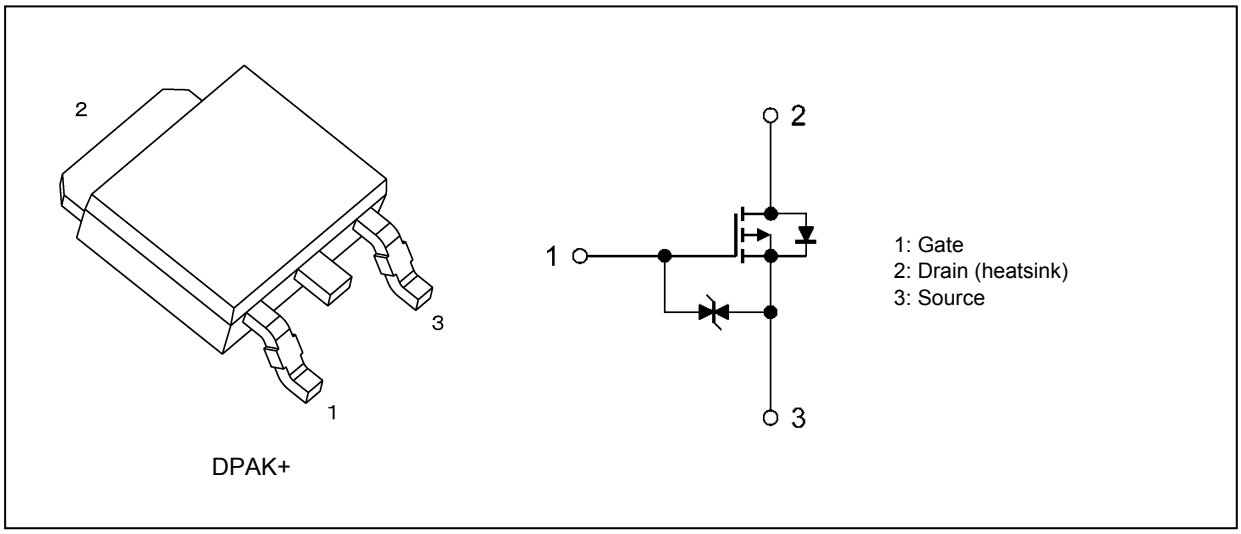
2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 7.0 mΩ (typ.) (V_{GS} = -10 V)

(2) Low leakage current: I_{DSS} = -10 μA (max) (V_{DS} = -40 V)

(3) Enhancement mode: V_{th} = -2.0 to -3.0 V (V_{DS} = -10 V, I_D = -1 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (T_a = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	-40	V
Gate-source voltage		V_{GSS}	-20/+10	
Drain current (DC)	(Note 1)	I_D	-40	A
Drain current (pulsed)	(Note 1)	I_{DP}	-80	
Power dissipation	(T_c = 25°C)	P_D	68	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	72	mJ
Avalanche current		I_{AR}	-40	A
Channel temperature	(Note 3)	T_{ch}	175	°C
Storage temperature	(Note 3)	T_{stg}	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	2.2	°C/W

Note 1: Ensure that the channel temperature does not exceed 175°C.
Note 2: V_{DD} = -25 V, T_{ch} = 25°C (initial), L = 47 μH, R_G = 25 Ω, I_{AR} = -40 A
Note 3: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

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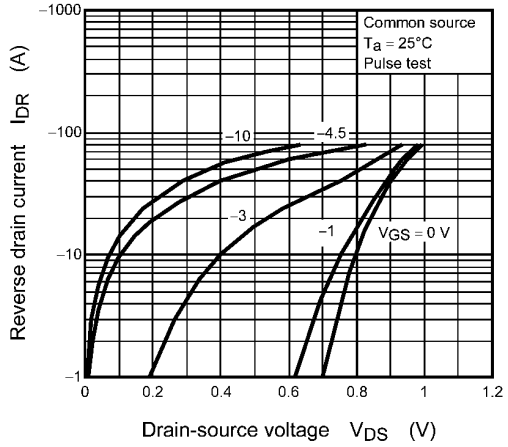


Fig. 8.7 I_{DR} - V_{DS}

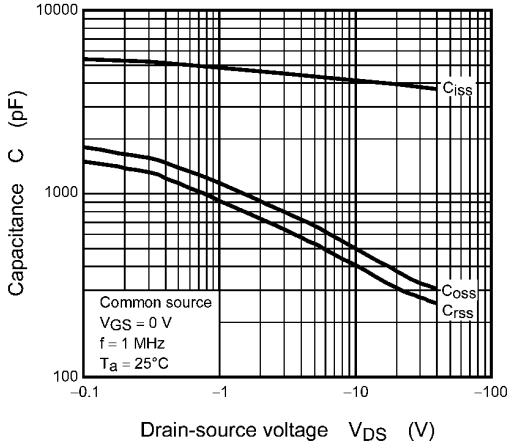


Fig. 8.8 Capacitance - V_{DS}

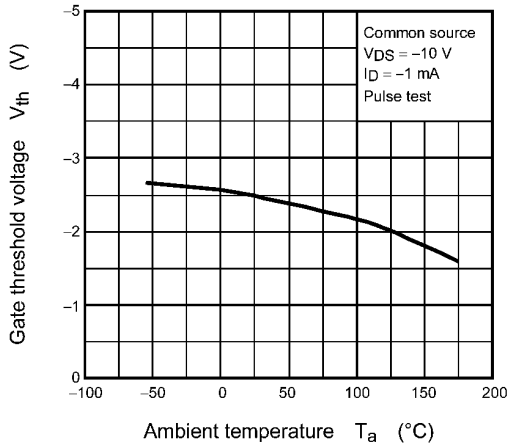


Fig. 8.9 V_{th} - T_a

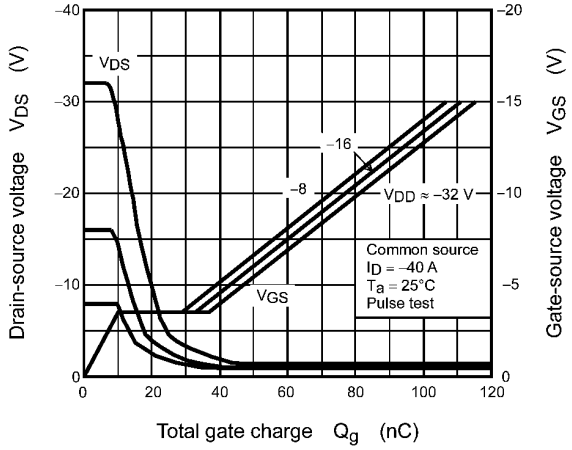


Fig. 8.10 Dynamic Input/Output Characteristics

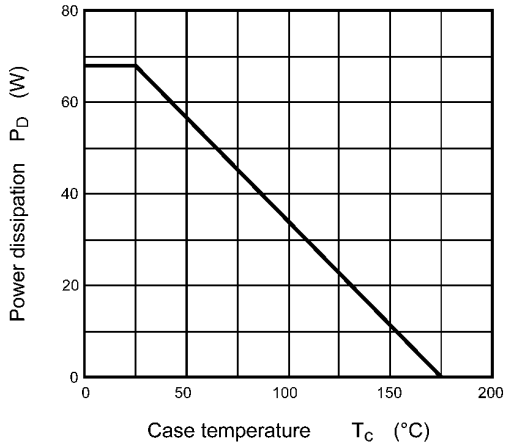


Fig. 8.11 P_D - T_c
(Guaranteed Maximum)

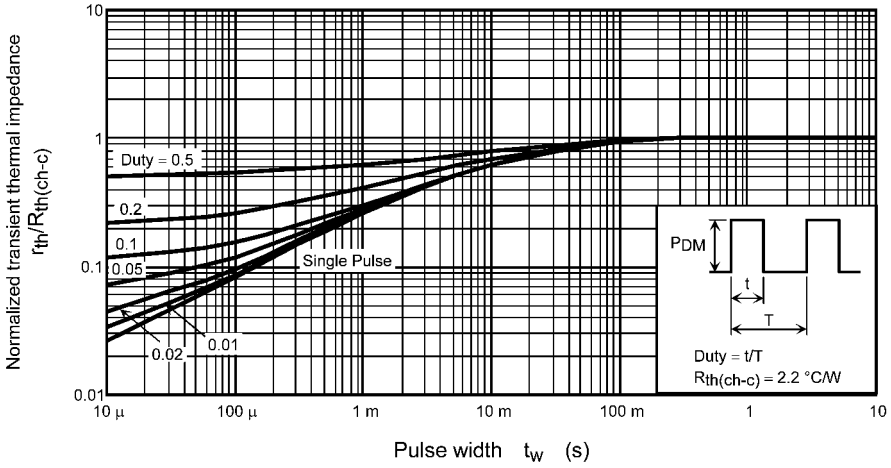


Fig. 8.12 $r_{th}/R_{th(ch-c)}$ - t_w (Guaranteed Maximum)

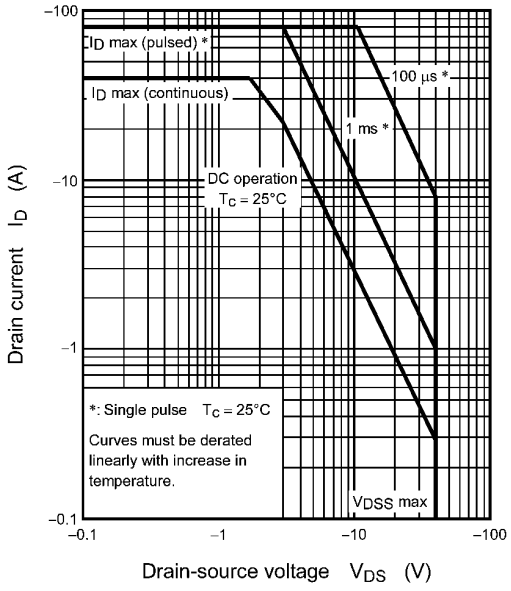


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

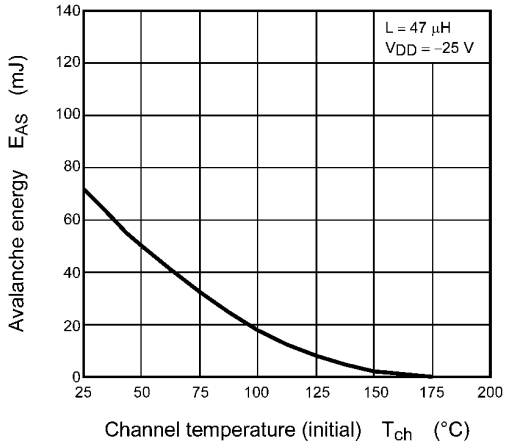
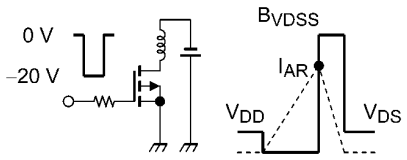


Fig. 8.14 E_{AS} - T_{ch} (Guaranteed Maximum)



$R_G = 25\ \Omega$
$V_{DD} = -25$ V, L = 47 μH

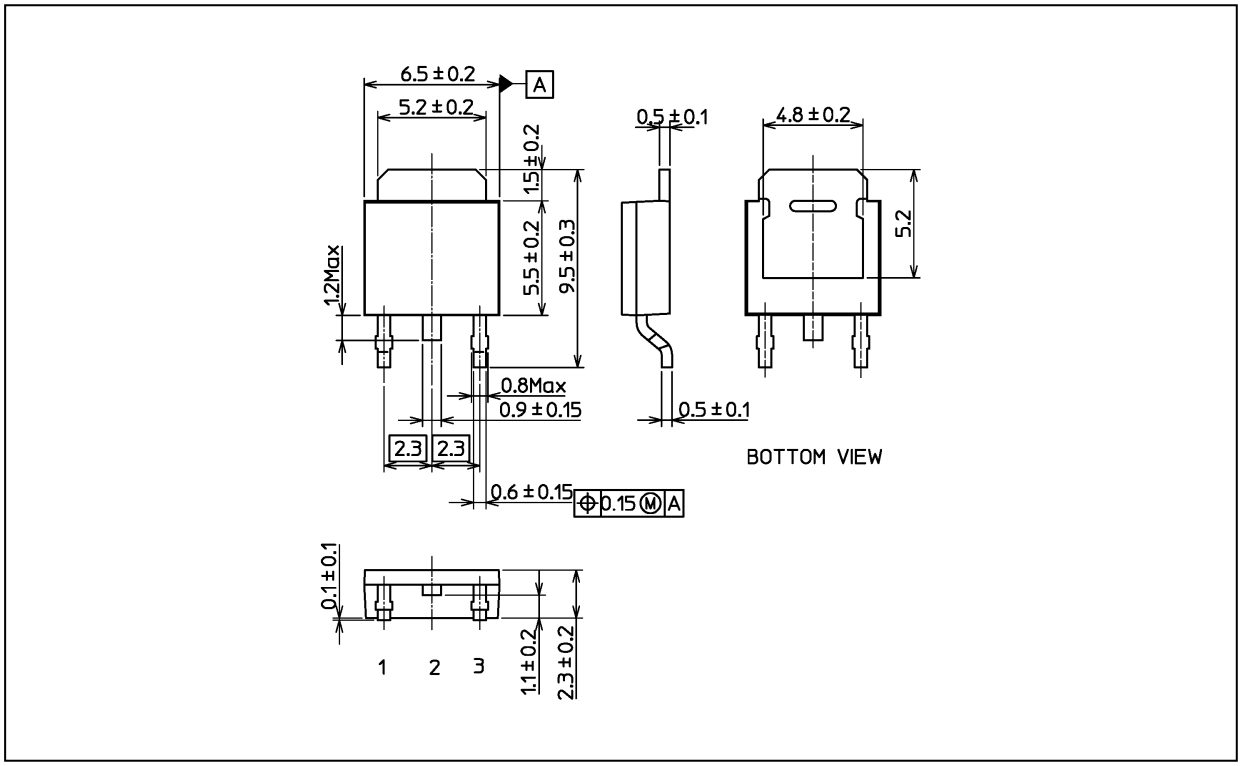
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.36 g (typ.)

Package Name(s)
TOSHIBA: 2-7M1A
Nickname: DPAK+

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