

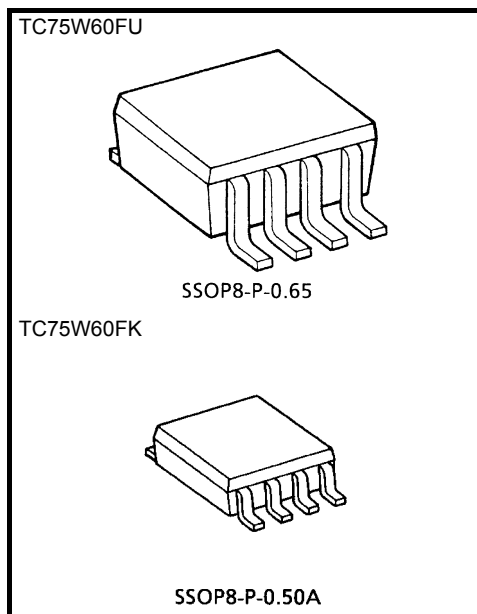
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC75W60FU, TC75W60FK

Dual Operational Amplifier

## Features

- High slew rate : SR ( $V_{DD} = 3\text{ V}$ ) = 5.1 V/ $\mu\text{s}$  (typ.)
- Single and dual power Supply operations are possible.  
:  $V_{DD} = \pm 0.9$  to 3.5 V or 1.8 to 7 V
- Lower supply current than general-purpose bipolar type op amps  
:  $I_{DD} (V_{DD} = 3\text{ V}) = 660\ \mu\text{A}$  (typ.)
- The internally phase compensated operational amplifier.
- Small package



Weight  
 SSOP8-P-0.65 : 0.021 g (typ.)  
 SSOP8-P-0.50A : 0.01 g (typ.)

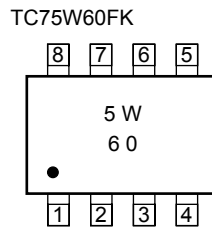
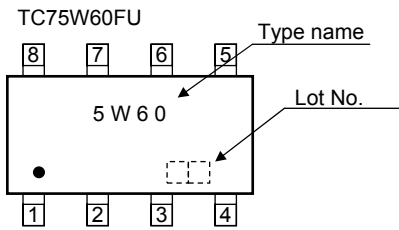
## Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics		Symbol	Rating	Unit
Supply voltage		$V_{DD}, V_{SS}$	7	V
Differential input voltage		$DV_{IN}$	$\pm 7$	V
Input voltage		$V_{IN}$	$V_{DD}$ to $V_{SS}$	V
Power dissipation	TC75W60FU	$P_D$	250	mW
	TC75W60FK		200	
Operating temperature		$T_{opr}$	-40 to 85	$^\circ\text{C}$
Storage temperature		$T_{stg}$	-55 to 125	$^\circ\text{C}$

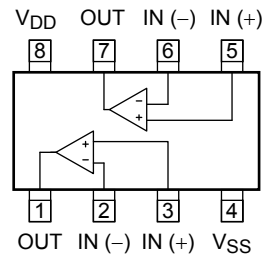
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Marking (top view)



## Pin Connection (top view)



## Electrical Characteristics

### DC Characteristics ( $V_{DD} = 3.0\text{ V}$ , $V_{SS} = \text{GND}$ , $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	$V_{IO}$	—	$R_S = 1\text{ k}\Omega$	—	2	7	mV
Input offset current	$I_{IO}$	—	—	—	1	—	pA
Input bias current	$I_I$	—	—	—	1	—	pA
Common mode input voltage	$CMV_{IN}$	—	—	0.0	—	2.1	V
Voltage gain (open loop)	$G_V$	—	—	60	70	—	dB
Maximum output voltage	$V_{OH}$	—	$R_L = 100\text{ k}\Omega$	2.9	—	—	V
	$V_{OL}$	—	$R_L = 100\text{ k}\Omega$	—	—	0.1	
Common mode rejection ratio	CMRR	—	$V_{IN} = 0.0\text{ to }2.1\text{ V}$	54	70	—	dB
Supply voltage rejection ratio	SVRR	—	$V_{DD} = 1.8\text{ to }7.0\text{ V}$	60	70	—	dB
Supply current	$I_{DD}$	—	—	—	660	1000	$\mu\text{A}$
Source current	$I_{\text{source}}$	—	—	330	700	—	$\mu\text{A}$
Sink current	$I_{\text{sink}}$	—	—	600	1250	—	$\mu\text{A}$

### DC Characteristics ( $V_{DD} = 1.8\text{ V}$ , $V_{SS} = \text{GND}$ , $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	$V_{IO}$	—	$R_S = 1\text{ k}\Omega$	—	2	7	mV
Input offset current	$I_{IO}$	—	—	—	1	—	pA
Input bias current	$I_I$	—	—	—	1	—	pA
Common mode input voltage	$CMV_{IN}$	—	—	0.3	—	0.9	V
Voltage gain (open loop)	$G_V$	—	—	—	70	—	dB
maximum output voltage	$V_{OH}$	—	$R_L = 100\text{ k}\Omega$	1.7	—	—	V
	$V_{OL}$	—	$R_L = 100\text{ k}\Omega$	—	—	0.1	
Common mode rejection ratio	CMRR	—	$V_{IN} = 0.3\text{ to }0.9\text{ V}$	50	60	—	dB
Supply current	$I_{DD}$	—	—	—	600	900	$\mu\text{A}$
Source current	$I_{\text{source}}$	—	—	300	700	—	$\mu\text{A}$
Sink current	$I_{\text{sink}}$	—	—	550	1150	—	$\mu\text{A}$

### AC Characteristics ( $V_{DD} = 3.0\text{ V}$ , $V_{SS} = \text{GND}$ , $T_a = 25^\circ\text{C}$ )

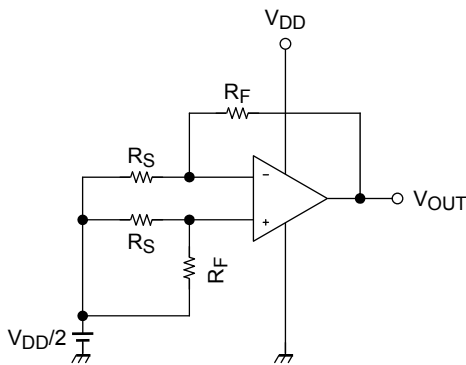
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	5.1	—	V/ $\mu\text{s}$
Unity gain cross frequency	$f_T$	—	—	—	3.7	—	MHz

### AC Characteristics ( $V_{DD} = 1.8\text{ V}$ , $V_{SS} = \text{GND}$ , $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	—	—	—	4.0	—	V/ $\mu\text{s}$
Unity gain cross frequency	$f_T$	—	—	—	3.0	—	MHz

## TEST CIRCUIT

### (1) SVRR, $V_{IO}$



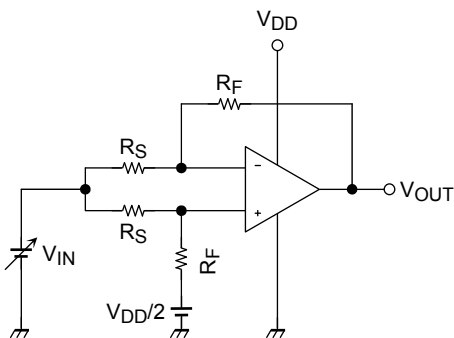
- SVRR  
 $V_{DD} = 1.5\text{ V} : V_{DD} = V_{DD1}, V_{OUT} = V_{OUT1}$   
 $V_{DD} = 7.0\text{ V} : V_{DD} = V_{DD2}, V_{OUT} = V_{OUT2}$

$$SVRR = 20 \log \left( \left| \frac{V_{OUT1} - V_{OUT2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

- $V_{IO}$

$$V_{IO} = \left( V_{OUT} - \frac{V_{DD}}{2} \right) \times \frac{R_S}{R_F + R_S}$$

### (2) CMRR, $CM_{VIN}$

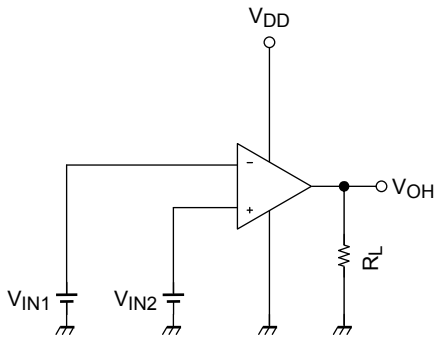


- CMRR  
 $V_{IN} = 0.0\text{ V} : V_{IN} = V_{DD1}, V_{OUT} = V_{OUT1}$   
 $V_{IN} = 2.5\text{ V} : V_{IN} = V_{DD2}, V_{OUT} = V_{OUT2}$

$$CMRR = 20 \log \left( \left| \frac{V_{OUT1} - V_{OUT2}}{V_{IN1} - V_{IN2}} \right| \times \frac{R_S}{R_F + R_S} \right)$$

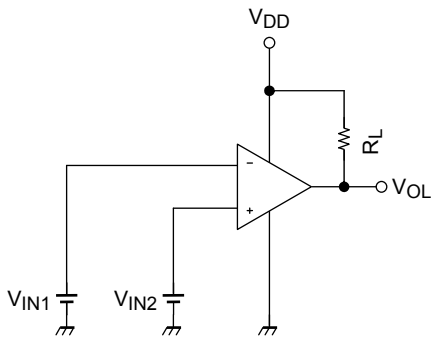
- $CM_{VIN}$

(3) V<sub>OH</sub>



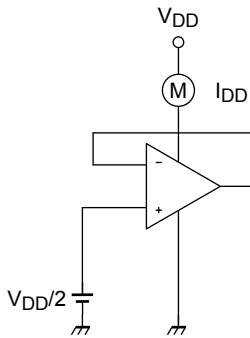
- V<sub>OH</sub>  
 $V_{IN1} = \frac{V_{DD}}{2} - 0.05 \text{ V}$   
 $V_{IN2} = \frac{V_{DD}}{2} + 0.05 \text{ V}$

(4) V<sub>OL</sub>

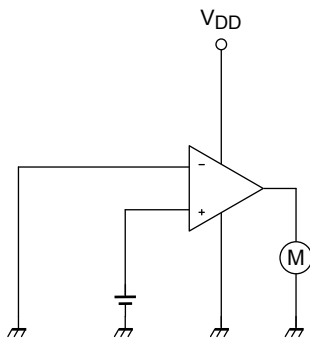


- V<sub>OL</sub>  
 $V_{IN1} = \frac{V_{DD}}{2} + 0.05 \text{ V}$   
 $V_{IN2} = \frac{V_{DD}}{2} - 0.05 \text{ V}$

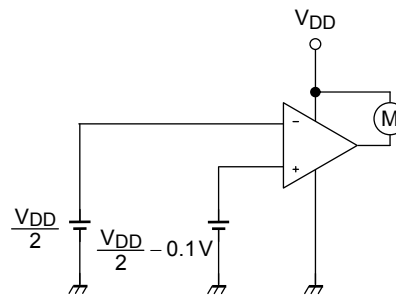
(5) I<sub>DD</sub>

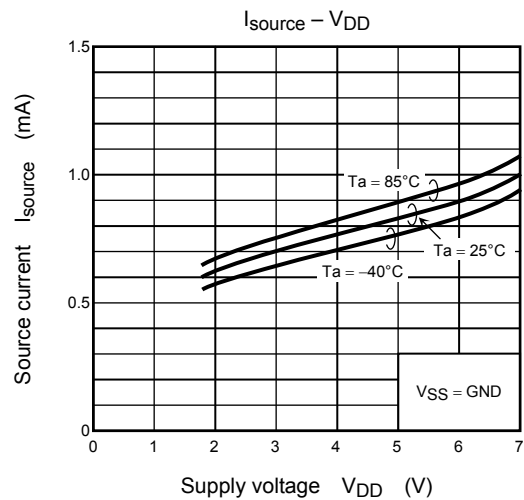
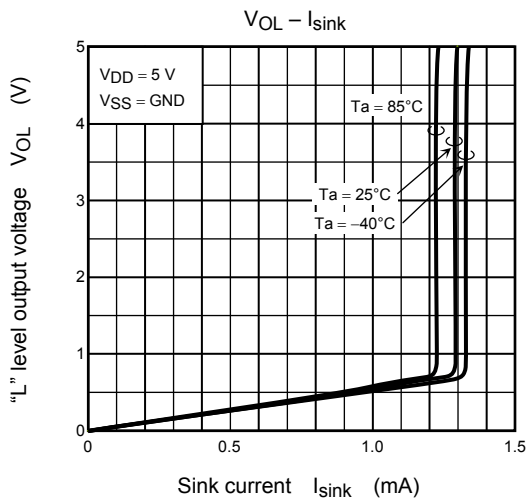
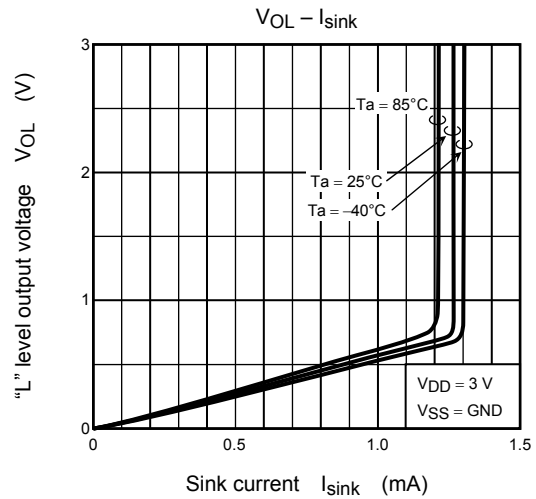
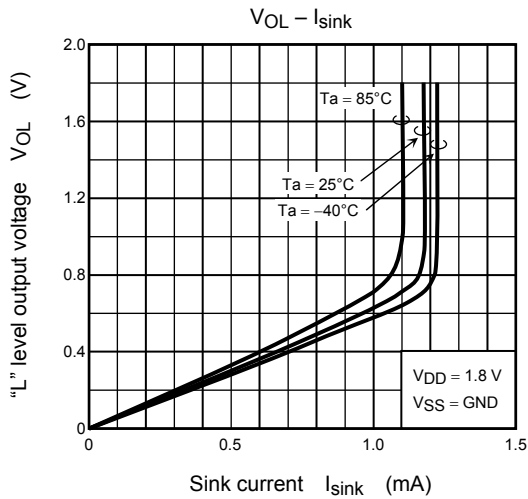
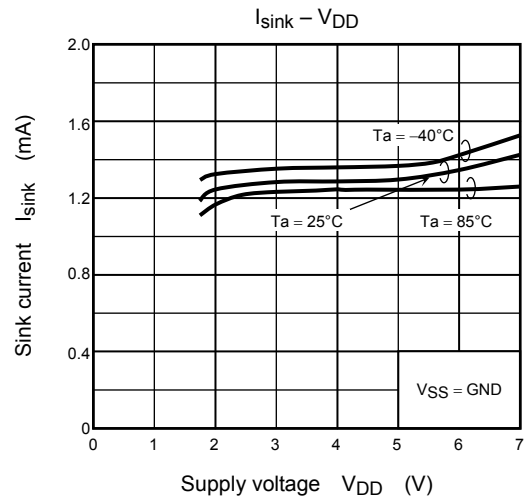
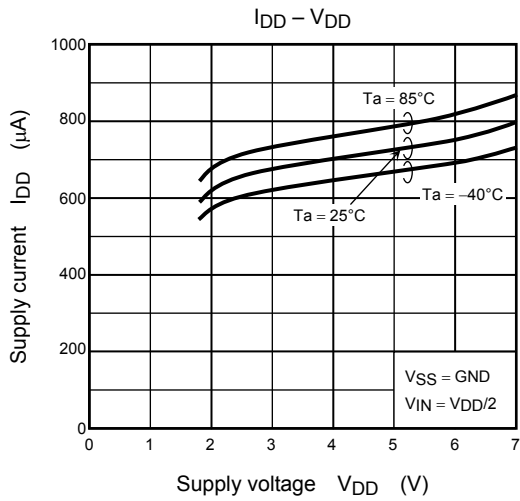


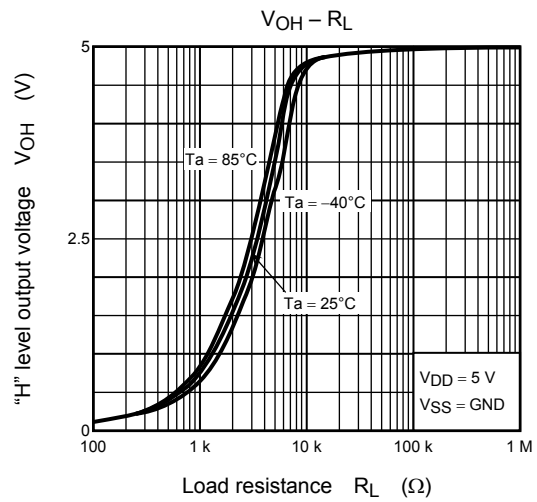
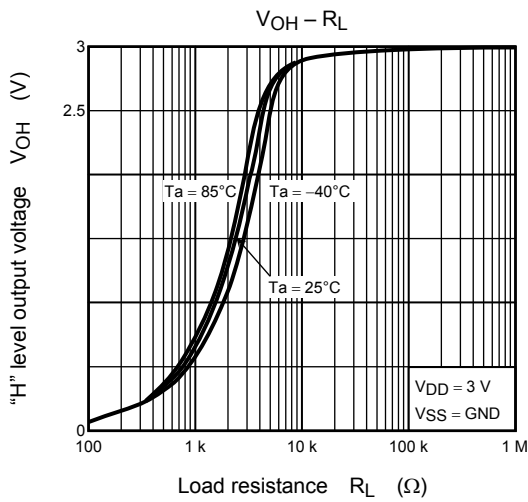
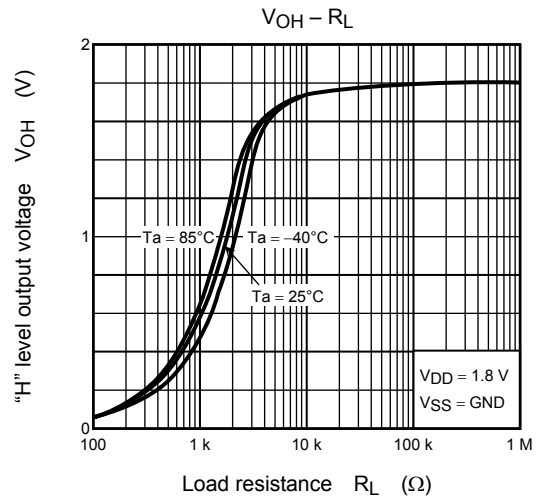
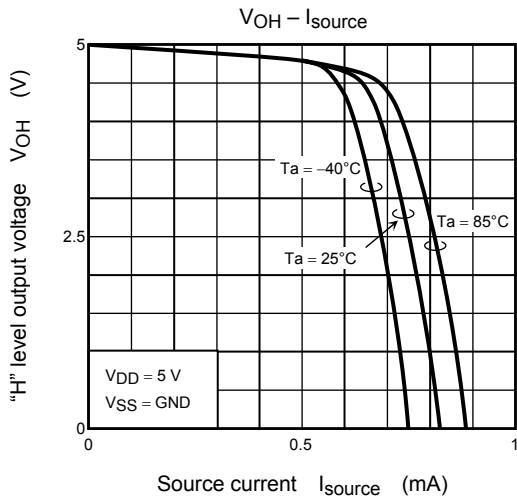
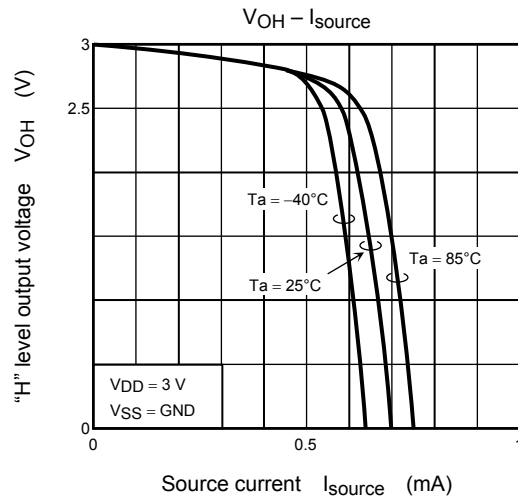
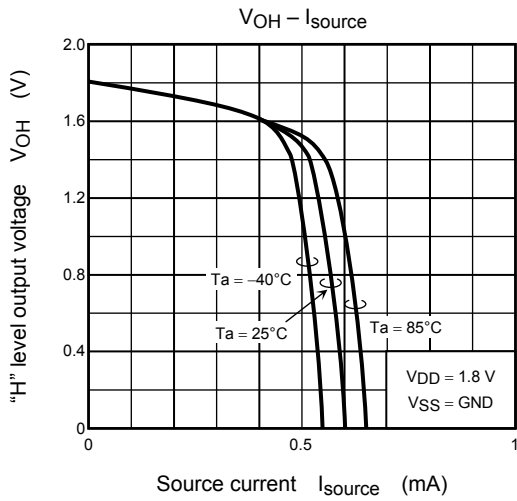
(6) I<sub>source</sub>

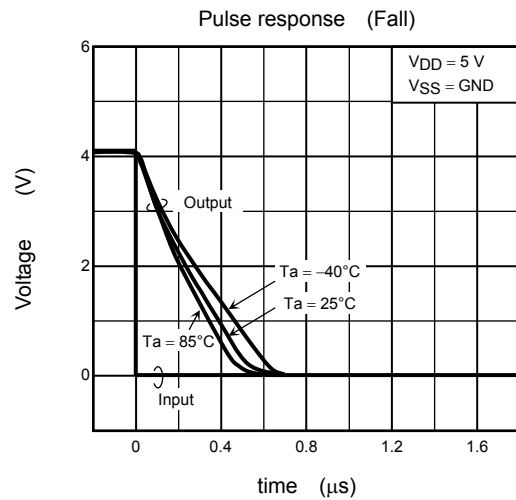
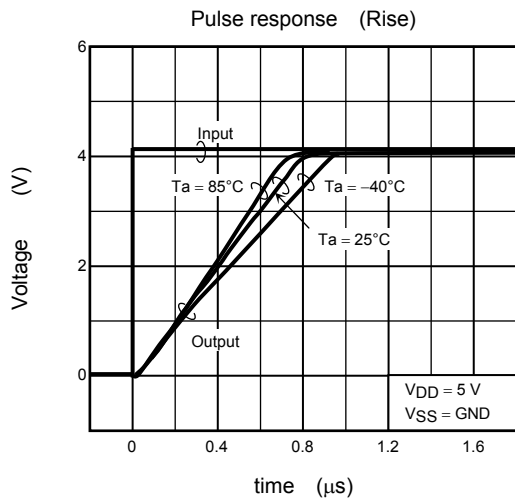
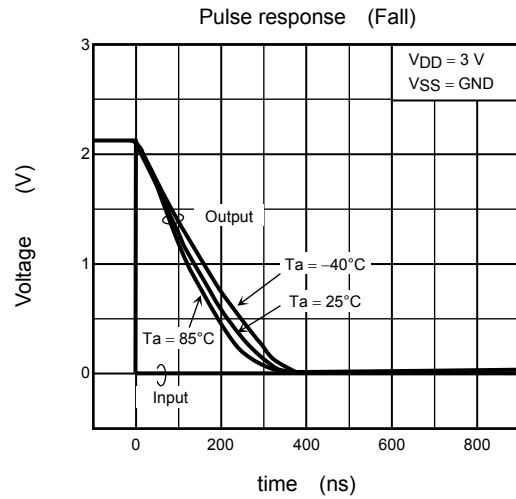
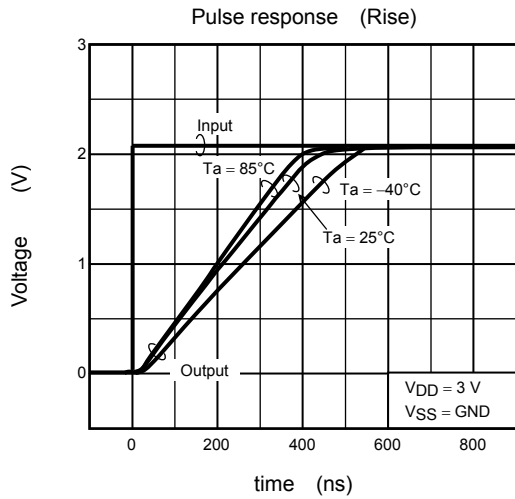
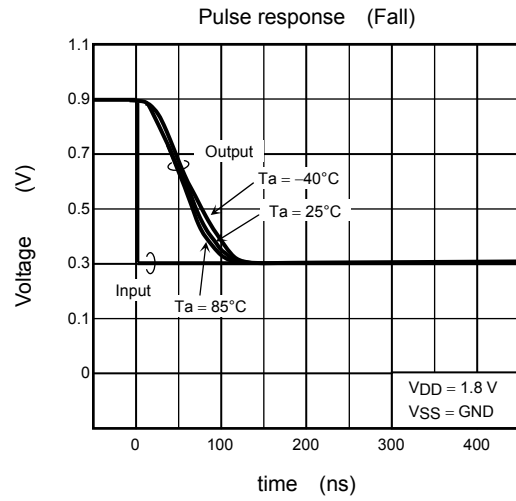
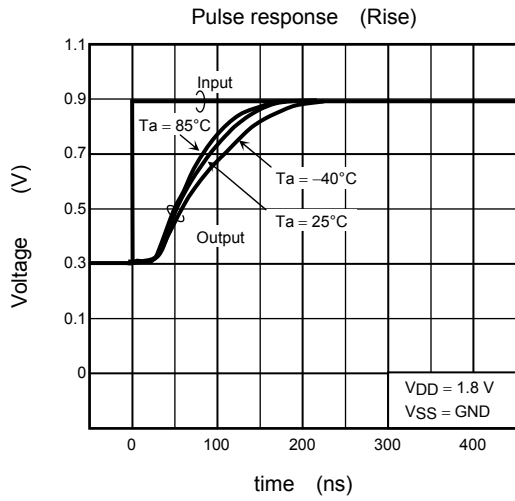


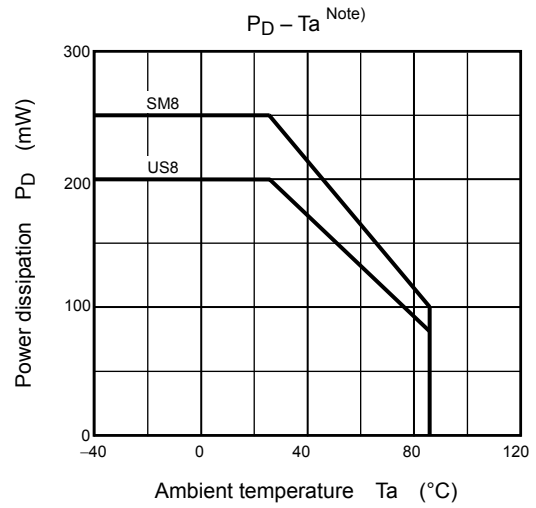
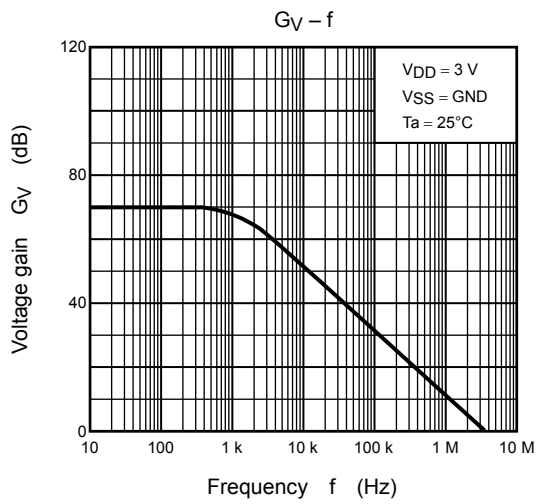
(7) I<sub>sink</sub>











Note):

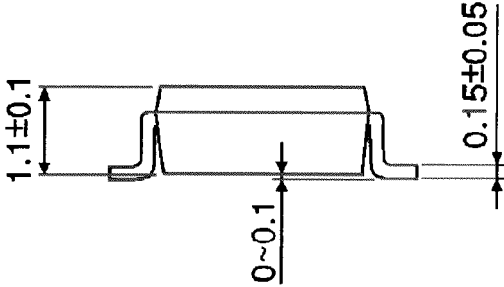
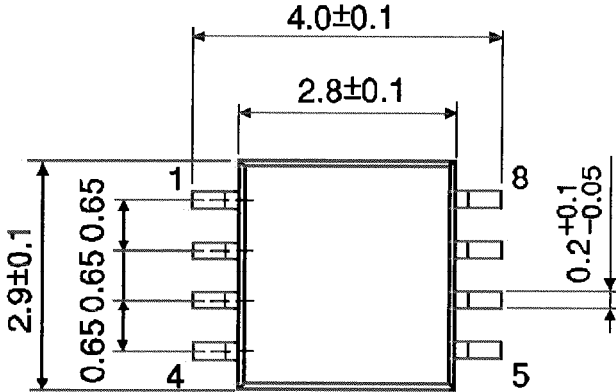
These power dissipation curves are given by measurement of only IC on the air and, in general, it become higher when mounted on PCB.

Since the power dissipation depends on mounted condition, please be sure to design.

**Package Dimensions**

SSOP8-P-0.65

Unit : mm

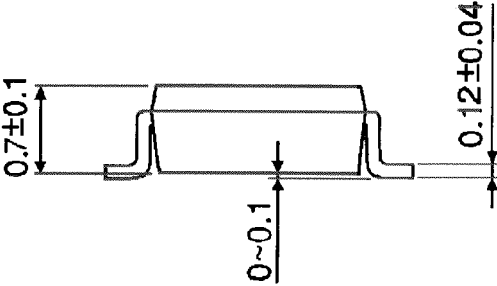
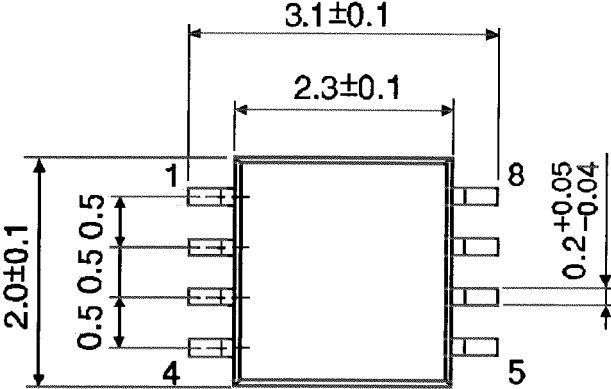


Weight: 0.021 g (typ.)

Package Dimensions

SSOP8-P-0.50A

Unit : mm



Weight: 0.01 g (typ.)

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