

TC7MB3257CFT, TC7MB3257CFK, TC7MB3257CFTG

Low Capacitance Quad 1-of-2 Multiplexer/Demultiplexer

The TC7MB3257C is a Low Capacitance CMOS Quad 1-of-2 multiplexer/demultiplexer. The low on resistance and the low capacitance of the switch allows connections to be made with minimal propagation delay time.

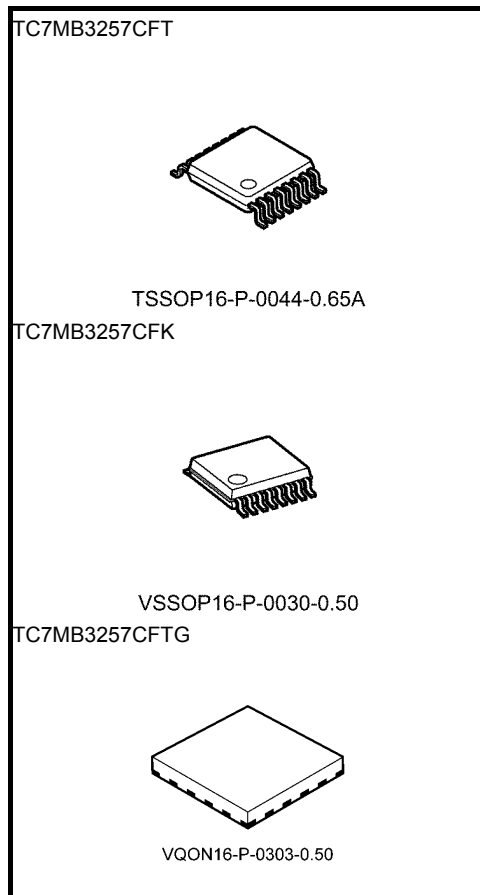
This device consists of four individual two-inputs multiplexer/demultiplexer with common select input (S) and output enable (\overline{OE}). The A inputs is connected to the B1 or B2 outputs determined by the combination both the select input (S) and output enable (\overline{OE}). When the output enable (\overline{OE}) input is held "H" level, the switches are open with regardless the state of select inputs and a high-impedance state exists between the switches.

All inputs are equipped with protection circuits against static discharge.

Features

- Operating voltage: $V_{CC} = 4.0$ to 5.5 V
- On-capacitance: $CI/O = 8.5$ pF Switch On (typ.)@ $V_{CC}=5V$
- On resistance: $R_{ON} = 3 \Omega$ (typ.) @ $V_{CC}=4.5V$, $V_{IS}=0$ V
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Compatible with TTL outputs (control inputs)
- Power-down protection for inputs (\overline{OE} , S and I/O)
- Package: TSSOP16, VSSOP16 (US16) , VQON16
- Pin compatible with the TC7MB3257FT/FK.

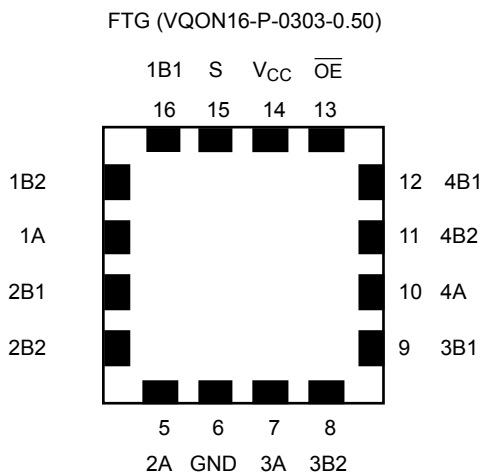
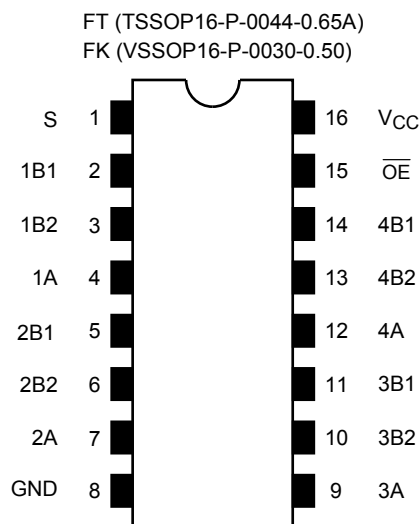
Note: When mounting VQON package, the type of recommended flux is RA or RMA.



Weight:

TSSOP16-P-0044-0.65A	: 0.06 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)
VQON16-P-0303-0.50	: 0.013 g (typ.)

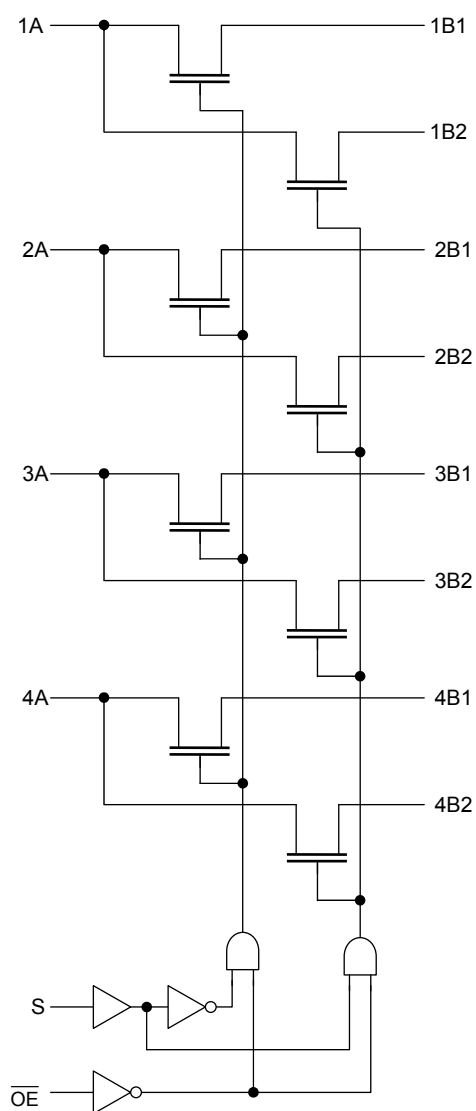
Pin Assignment (top view)



Truth Table

Inputs		Function
$\overline{\text{OE}}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC switch voltage	V_S	-0.5 to 7.0	V
Input diode current	I_{IK}	-50	mA
Continuous channel current	I_S	50	mA
Power dissipation	P_D	180	mW
DC V_{CC}/GND current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Switch voltage	V_S	0 to 5.5	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused control pin inputs must be tied to either V_{CC} or GND.

Leave unused switch I/O pins open.

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		Min	Typ.	Max	Unit	
					V _{CC} (V)				
Input voltage	“H” level	V _{IH}	—		4.5 to 5.5	2.0	—	—	V
	“L” level	V _{IL}	—		4.5 to 5.5	—	—	0.8	
Input leakage current (\overline{OE} , S)		I _{IN}	V _{IN} = 0 to 5.5 V		4.5 to 5.5	—	—	±1.0	μA
Power off leakage current		I _{OFF}	A, B, \overline{OE} = 0 to 5.5 V		0	—	—	10	μA
Off-state leakage current (switch off)		I _{SZ}	A, B = 0 to 5.5 V, \overline{OE} = V _{CC}		4.5 to 5.5	—	—	±1.0	μA
ON resistance (Note 2)	R _{ON}	V _{IS} = 0 V	I _{IS} = 30 mA	(Note1)	4.5	—	3	7	Ω
		V _{IS} = 2.4 V	I _{IS} = 15 mA	(Note1)	4.5	—	5	15	
					4.0	—	9	20	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0		5.5	—	—	10	μA
Increase in I _{CC} per input		ΔI _{CC}	V _{IN} = 3.4 V (one input)		5.5	—	—	500	μA

Note 1: Typical values are at Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch.
ON resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit
				V _{CC} (V)			
Output enable time (\overline{OE} to bus)		t _{pZL}	Figure 1, Figure 2	4.5	—	7	ns
		t _{pZH}					
Output enable time (S to bus)		t _{pZL}	Figure 1, Figure 2	4.5	—	9	ns
		t _{pZH}					
Output disable time (\overline{OE} to bus)		t _{pLZ}	Figure 1, Figure 2	4.5	—	7	ns
		t _{pHZ}					
Output disable time (S to bus)		t _{pLZ}	Figure 1, Figure 2	4.5	—	9	ns
		t _{pHZ}					

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit
				V _{CC} (V)		
Control pin input capacitance (\overline{OE} , S)		C _{IN}	V _{IN} = 0 V (Note)	5.0	5	pF
Switch OFF terminal capacitance (A port)		C _{I/O}	\overline{OE} = V _{CC} , V _{IS} = 0 V (Note)	5.0	6	pF
Switch OFF terminal capacitance (B port)		C _{I/O}	\overline{OE} = V _{CC} , V _{IS} = 0 V (Note)	5.0	4	pF
Switch ON terminal capacitance (A port)		C _{I/O}	\overline{OE} = GND, V _{IS} = 0 V (Note)	5.0	8.5	pF
Switch ON terminal capacitance (B port)		C _{I/O}	\overline{OE} = GND, V _{IS} = 0 V (Note)	5.0	8.5	pF

Note: This parameter is guaranteed by design.

AC Test Circuit

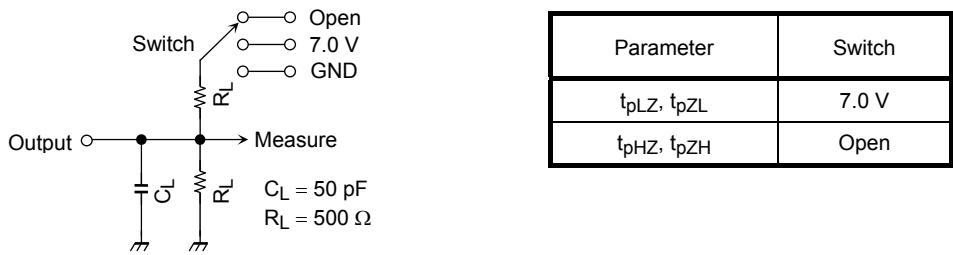


Figure 1

AC Waveform

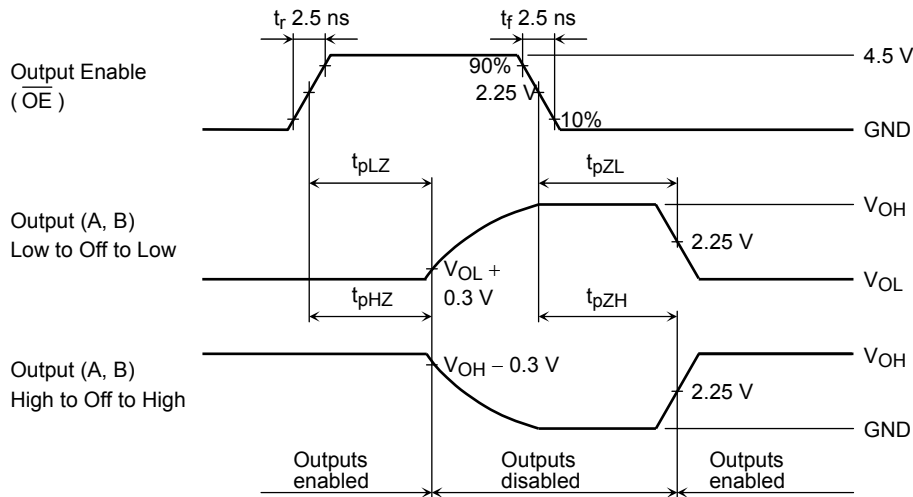
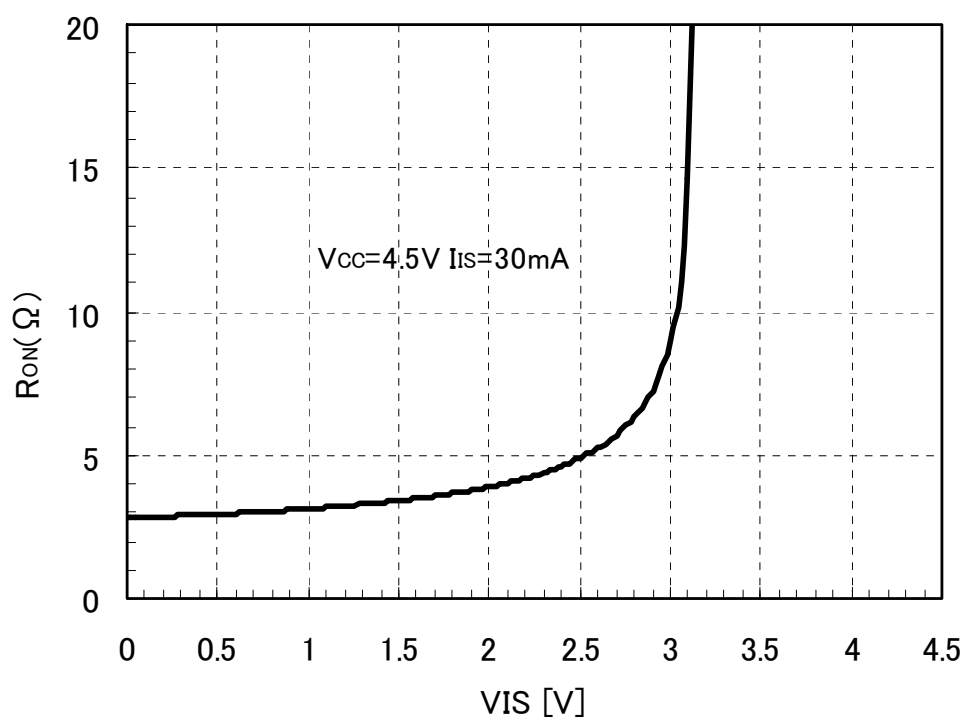


Figure 2 $t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}$

R_{ON} - V_{IS} Characteristic (Typ.) $T_a = 25^\circ\text{C}$



Rise and Fall Times (tr / tf) of the TC7MB3257C I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance (C_{I/O}) and the on-resistance (R_{ON}) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MB3257C.

The tr(out) / tf(out) values can be approximated as follows. (Figure 3 shows the test circuit.)

$$tr(out) / tf(out) \text{ (approx)} = - (C_{I/O} + C_L) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln \left(\frac{(V_{OH} - V_{OL}) - V_M}{(V_{OH} - V_{OL})} \right)$$

where, R_{DRIVE} is the output impedance of the previous-stage circuit.

Calculation example:

$$tr(out) \text{ (approx)} = - (8.5 + 15) \text{E-12} \cdot (120 + 3) \cdot \ln \left(\frac{(4.5 - 0) - 2.25}{(4.5 - 0)} \right) \approx 2.0 \text{ ns}$$

Calculation conditions:

V_{CC} = 4.5 V, C_L = 15 pF, R_{DRIVE} = 120 Ω (output impedance of the previous IC), V_M = 2.25 V (V_{CC} / 2)

Output of the previous IC = digital (i.e., high-level voltage = V_{CC}; low-level voltage = GND)

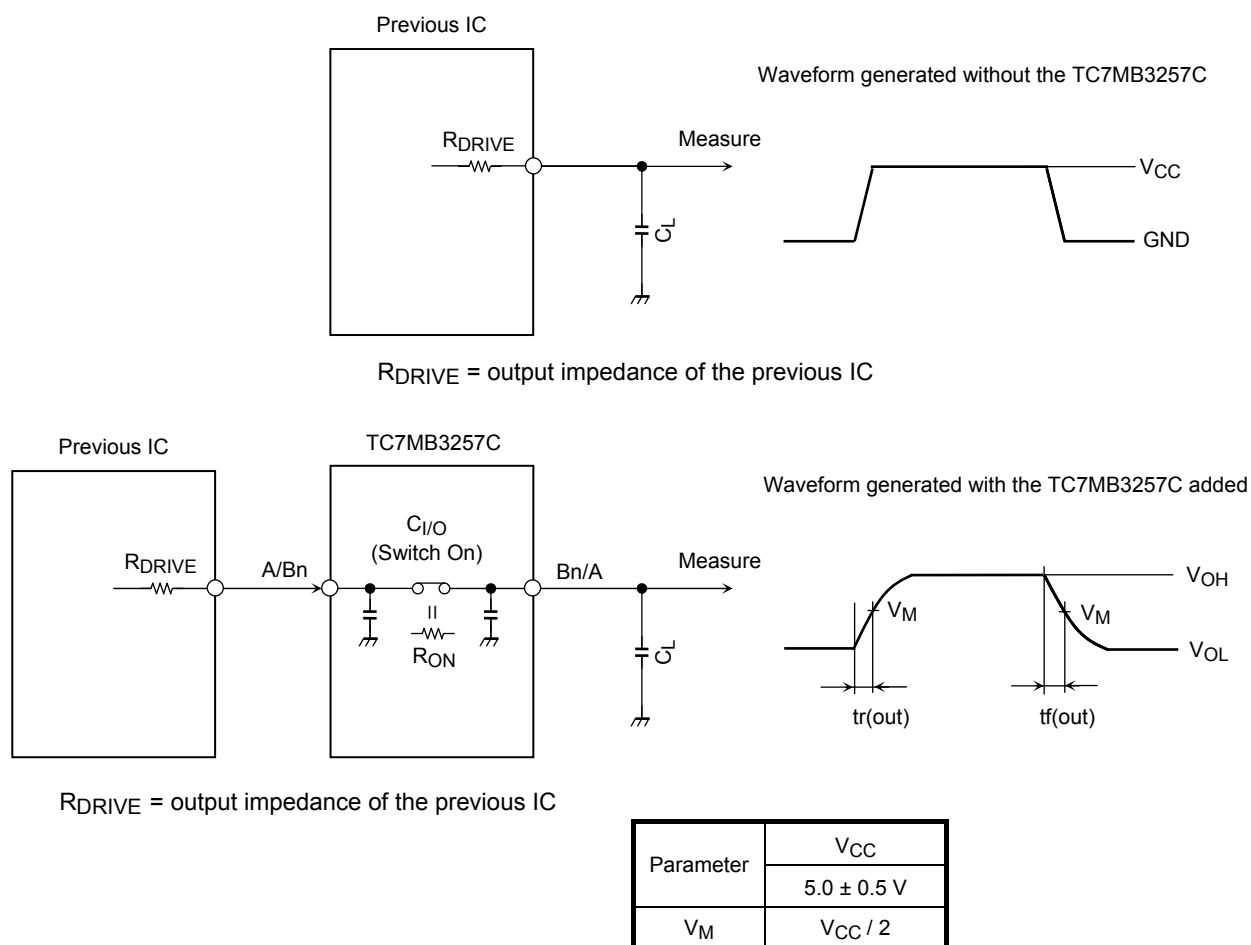
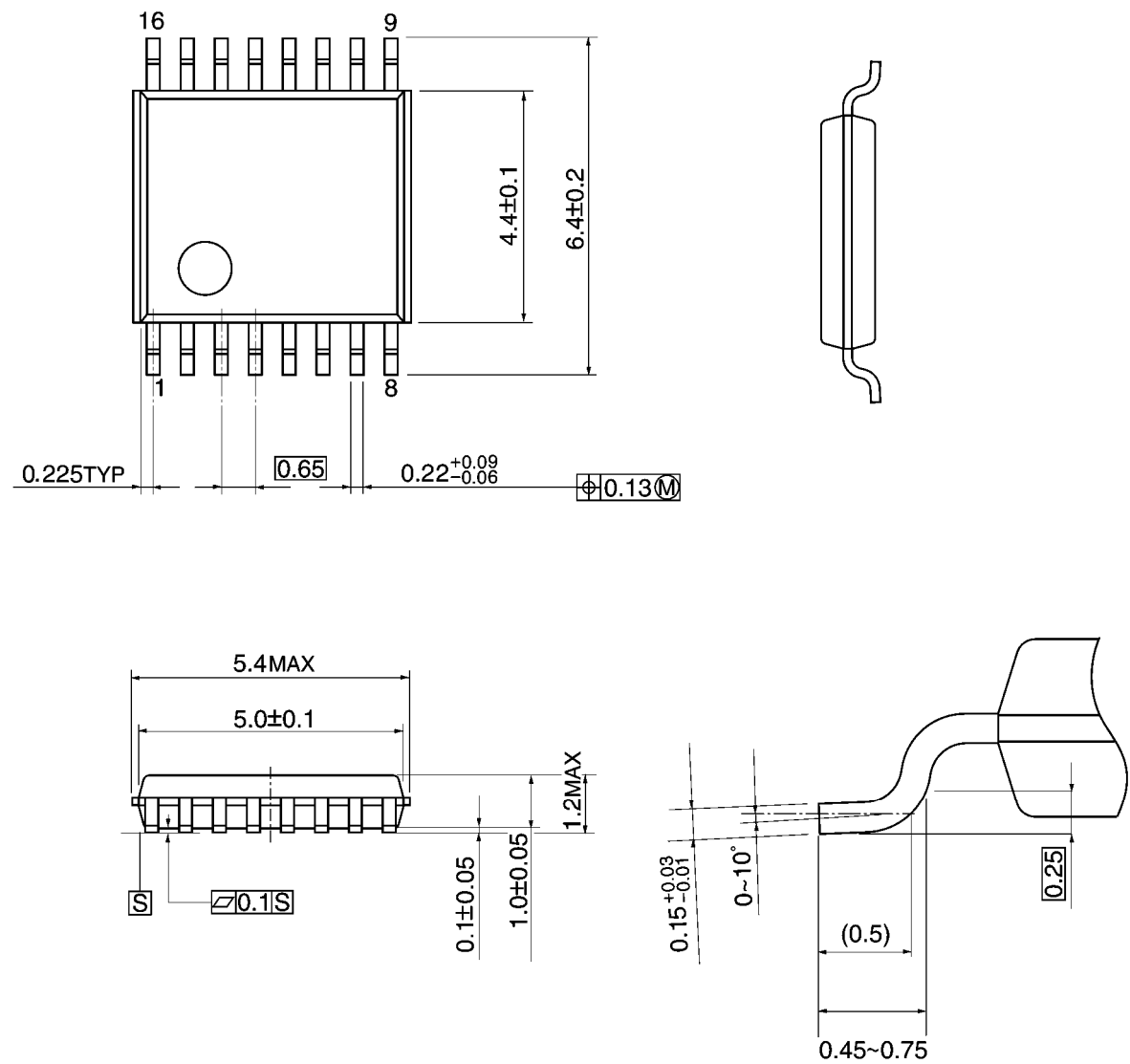


Figure 3 Test Circuit

Package Dimensions

TSSOP16-P-0044-0.65A

Unit: mm

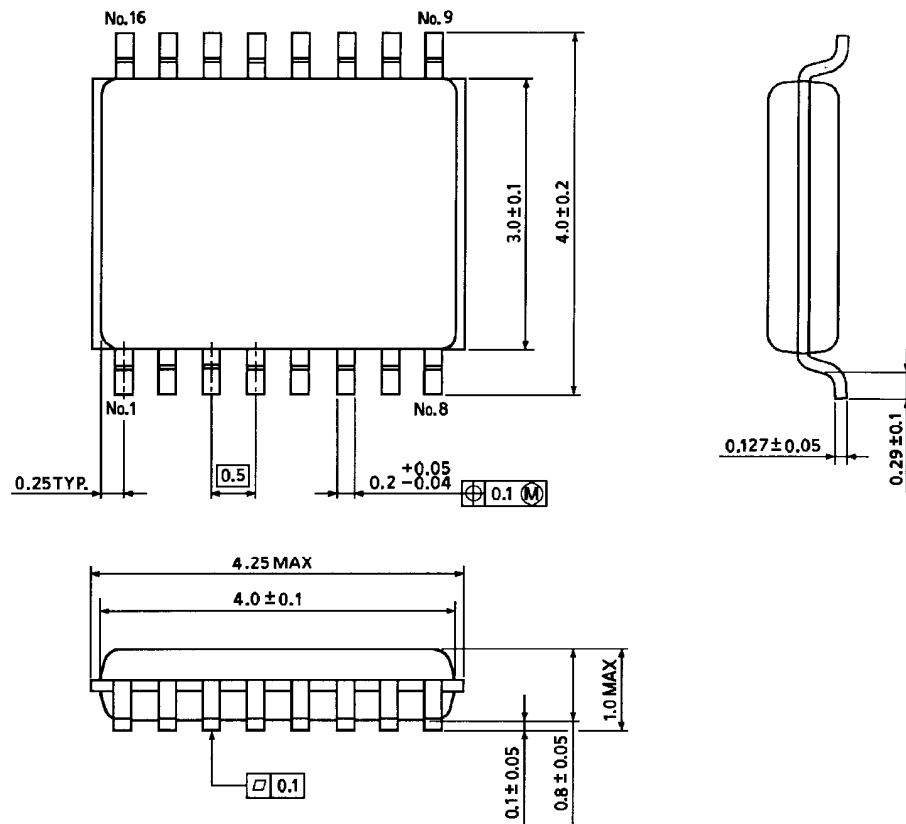


Weight: 0.06 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit : mm



Weight: 0.02 g (typ.)

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