

TC7SP3125TU, TC7SP3125WBG

Low Voltage / Low Power 1-Bit Dual Supply Bus Buffer

The TC7SP3125 is an advanced high-speed CMOS 1-bit dual supply voltage interface bus buffer fabricated with silicon gate CMOS technology.

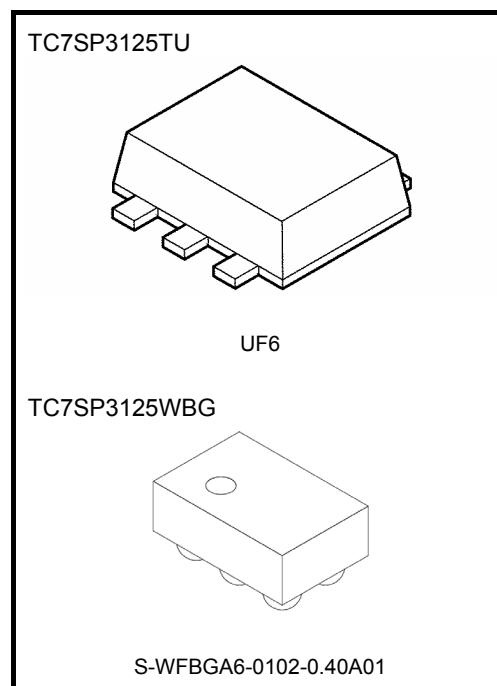
It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Designed for use as an interface between a 1.2-V, 1.5-V, 1.8-V, or 2.5-V bus and a 1.8-V, 2.5-V or 3.3-V bus in mixed 1.2-V, 1.5-V, 1.8-V or 2.5-V/1.8-V, 2.5-V or 3.3-V supply systems.

The A-input interfaces with the 1.2-V, 1.5-V, 1.8-V or 2.5-V bus, the B-output with the 1.8-V, 2.5-V, 3.3-V bus.

The enable input (\overline{OE}) can be used to disable the device so that the signal lines are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight

UF6: 0.007 g (typ.)

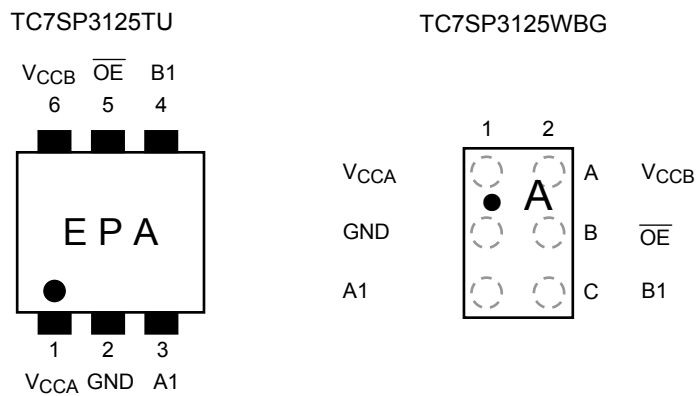
S-WFBGA6-0102-0.40A01: 0.001 g (typ.)

Features (Note)

- Level converter for interfacing 1.2-V to 1.8-V, 1.2-V to 2.5-V, 1.2-V to 3.3-V, 1.5-V to 2.5-V, 1.5-V to 3.3-V, 1.8-V to 2.5-V, 1.8-V to 3.3-V or 2.5-V to 3.3-V system.
- High-speed operation : $t_{pd} = 6.8 \text{ ns (max)}$ ($V_{CCA} = 2.5 \pm 0.2 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 7.8 \text{ ns (max)}$ ($V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 8.6 \text{ ns (max)}$ ($V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 22 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 3.3 \pm 0.3 \text{ V}$)
 $t_{pd} = 9.5 \text{ ns (max)}$ ($V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 10.5 \text{ ns (max)}$ ($V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 23 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$)
 $t_{pd} = 30 \text{ ns (max)}$ ($V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 1.8 \pm 0.15 \text{ V}$)
- Output current : $I_{OHB} / I_{OLB} = \pm 12 \text{ mA (min)}$ ($V_{CCB} = 3.0 \text{ V}$)
 $I_{OHB} / I_{OLB} = \pm 9 \text{ mA (min)}$ ($V_{CCB} = 2.3 \text{ V}$)
 $I_{OHB} / I_{OLB} = \pm 3 \text{ mA (min)}$ ($V_{CCB} = 1.65 \text{ V}$)
- Latch-up performance: -300 mA
- ESD performance: Machine model $\geq \pm 200 \text{ V}$
Human body model $\geq \pm 2000 \text{ V}$
- Ultra-small package: UF6, WCSP6
- Low current consumption: Using the new circuit significantly reduces current consumption when $\overline{OE} = \text{"H"}$.
Suitable for battery-driven applications such as PDAs and cellular phones.
- Floating A-bus is permitted. (when $\overline{OE} = \text{"H"}$)
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs.

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

Pin Assignment (top view)

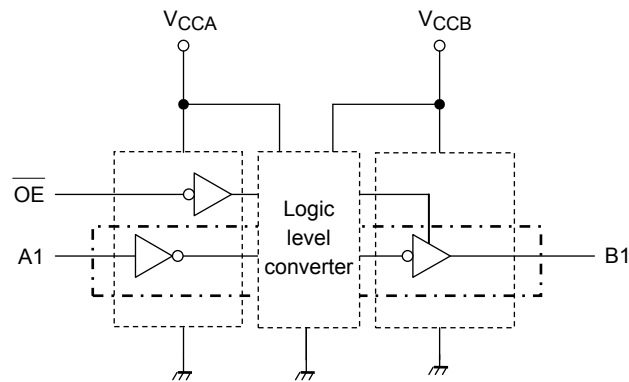


Truth Table

| Inputs | | Output |
|-----------------|----|--------|
| \overline{OE} | A1 | B1 |
| L | L | L |
| L | H | H |
| H | X | Z |

X: Don't care
Z: High impedance

Block Diagram



Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|---|-------------------|---|------|
| Power supply voltage (Note 2) | V _{CCA} | −0.5 to 4.6 | V |
| | V _{CCB} | −0.5 to 4.6 | |
| DC input voltage (A1, $\overline{\text{OE}}$) | V _{IN} | −0.5 to 4.6 | V |
| DC output voltage (B1) | V _{OUTB} | −0.5 to 4.6 (Note 3) | V |
| | | −0.5 to V _{CCB} + 0.5 (Note 4) | |
| Input diode current | I _{IK} | −25 | mA |
| Output diode current | I _{OK} | ±50 (Note 5) | mA |
| DC output current | I _{OUTB} | ±25 | mA |
| DC V _{CC} /ground current per supply pin | I _{CCA} | ±25 | mA |
| | I _{CCB} | ±50 | |
| Power dissipation | P _D | 200 (UF6) / 100 (WCSP6) | mW |
| Storage temperature | T _{stg} | −65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: Don't supply a voltage to V_{CCB} pin when V_{CCA} is in the OFF state.

Note 3: Output in OFF state

Note 4: High or Low state. I_{OUT} absolute maximum rating must be observed.

Note 5: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

| Characteristics | Symbol | Rating | Unit |
|--|-------------------|--------------------------------|------|
| Power supply voltage | V _{CCA} | 1.1 to 2.7 | V |
| | V _{CCB} | 1.65 to 3.6 | |
| Input voltage (A1, $\overline{\text{OE}}$) | V _{IN} | 0 to 3.6 | V |
| Output voltage (B1) | V _{OUTB} | 0 to 3.6 (Note 2) | V |
| | | 0 to V _{CCB} (Note 3) | |
| Output current (B1) | I _{OUTB} | ±12 (Note 4) | mA |
| | | ±9 (Note 5) | |
| | | ±3 (Note 6) | |
| Operating temperature | T _{opr} | −40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 10 (Note 7) | ns/V |

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Output in OFF state

Note 3: High or low state

Note 4: V_{CCB} = 3.0 to 3.6 V

Note 5: V_{CCB} = 2.3 to 2.7 V

Note 6: V_{CCB} = 1.65 to 1.95 V

Note 7: V_{IN} = 0.8 to 2.0 V, V_{CCA} = 2.5 V, V_{CCB} = 3.0 V

Electrical Characteristics
DC Characteristics (1.1 V ≤ V_{CCA} ≤ 2.7 V, 1.65 V ≤ V_{CCB} ≤ 3.6 V)

| Characteristics | Symbol | Test Condition | | V _{CCA} (V) | V _{CCB} (V) | Ta = -40 to 85°C | | Unit |
|----------------------------------|-------------------|---|----------------------------|-------------------------------|----------------------|---------------------------|---------------------------|------|
| | | | | | | Min | Max | |
| H-level input voltage | V _{IHA} | $\overline{\text{OE}}$, A1 | | 1.1 ≤ V _{CCA} < 1.4 | 1.65 to 3.6 | 0.65× V _{CCA} | — | V |
| | | | | 1.4 ≤ V _{CCA} < 1.65 | 1.65 to 3.6 | 0.65× V _{CCA} | — | |
| | | | | 1.65 ≤ V _{CCA} < 2.3 | 2.3 to 3.6 | 0.65× V _{CCA} | — | |
| | | | | 2.3 ≤ V _{CCA} < 2.7 | 2.7 to 3.6 | 1.6 | — | |
| L-level input voltage | V _{ILA} | $\overline{\text{OE}}$, A1 | | 1.1 ≤ V _{CCA} < 1.4 | 1.65 to 3.6 | — | 0.30× V _{CCA} | V |
| | | | | 1.4 ≤ V _{CCA} < 1.65 | 1.65 to 3.6 | — | 0.30× V _{CCA} | |
| | | | | 1.65 ≤ V _{CCA} < 2.3 | 2.3 to 3.6 | — | 0.35× V _{CCA} | |
| | | | | 2.3 ≤ V _{CCA} < 2.7 | 2.7 to 3.6 | — | 0.7 | |
| H-level output voltage | V _{OHB} | A1 = V _{IH} | I _{OHB} = -100 μA | 1.1 to 2.7 | 1.65 to 3.6 | V _{CCB} - 0.2 | — | V |
| | | | I _{OHB} = -3 mA | 1.1 to 1.65 | 1.65 | 1.25 | — | |
| | | | I _{OHB} = -9 mA | 1.1 to 2.3 | 2.3 | 1.7 | — | |
| | | | I _{OHB} = -12 mA | 1.1 to 2.7 | 3.0 | 2.2 | — | |
| L-level output voltage | V _{OLB} | A1 = V _{IL} | I _{OLB} = 100 μA | 1.1 to 2.7 | 1.65 to 3.6 | — | 0.2 | V |
| | | | I _{OLB} = 3 mA | 1.1 to 1.65 | 1.65 | — | 0.3 | |
| | | | I _{OLB} = 9 mA | 1.1 to 2.3 | 2.3 | — | 0.6 | |
| | | | I _{OLB} = 12 mA | 1.1 to 2.7 | 3.0 | — | 0.55 | |
| 3-state output OFF state current | I _{OZB} | A1 = V _{IHA} or V _{ILA} B1 = 0 to 3.6 V | | 1.1 to 2.7 | 1.65 to 3.6 | — | ±2.0 | μA |
| Input leakage current | I _{IN} | V _{IN} = 0 to 3.6 V | | 1.1 to 2.7 | 1.65 to 3.6 | — | ±1.0 | μA |
| Power-off leakage current | I _{OFF1} | V _{IN} , B1 = 0 to 3.6 V | | 0 | 0 | — | 2.0 | μA |
| | I _{OFF2} | $\overline{\text{OE}}$ = V _{CCA} | | 1.1 to 2.7 | 0 | — | 2.0 | |
| | I _{OFF3} | A1, B1 = 0 to 3.6 V | | 1.1 to 2.7 | Open | — | 2.0 | |
| Quiescent supply current | I _{CCA} | V _{IN} = V _{CCA} or GND | | 1.1 to 2.7 | 1.65 to 3.6 | — | 2.0 | μA |
| | I _{CCB} | V _{IN} = V _{CCA} or GND | | 1.1 to 2.7 | 1.65 to 3.6 | — | 2.0 | |
| | I _{CCA} | V _{CCA} < V _{IN} ≤ 3.6 V | | 1.1 to 2.7 | 1.65 to 3.6 | — | ±2.0 | |
| | I _{CCB} | V _{IN} = V _{CCA} V _{CCB} ≤ B1 ≤ 3.6 V | | 1.1 to 2.7 | 1.65 to 3.6 | — | ±2.0 | |

AC Characteristics (Ta = -40 to 85°C, Input: tr = tf = 2.0 ns)
VCCA = 2.5 ± 0.2 V, VCCB = 3.3 ± 0.3 V

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|--------------------------------------|--------------------|-----|-----|------|
| Propagation delay time (A1 → B1) | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 1.0 | 6.8 | ns |
| 3-state output enable time (\overline{OE} → B1) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 1.0 | 8.7 | |
| 3-state output disable time (\overline{OE} → B1) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 1.0 | 3.9 | |

VCCA = 1.8 ± 0.15 V, VCCB = 3.3 ± 0.3 V

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|--------------------------------------|--------------------|-----|------|------|
| Propagation delay time (A1 → B1) | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 1.0 | 7.8 | ns |
| 3-state output enable time (\overline{OE} → B1) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 1.0 | 10.7 | |
| 3-state output disable time (\overline{OE} → B1) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 1.0 | 5.2 | |

VCCA = 1.5 ± 0.1 V, VCCB = 3.3 ± 0.3 V

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|--------------------------------------|--------------------|-----|------|------|
| Propagation delay time (A1 → B1) | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 1.0 | 8.6 | ns |
| 3-state output enable time (\overline{OE} → B1) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 1.0 | 14.3 | |
| 3-state output disable time (\overline{OE} → B1) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 1.0 | 6.6 | |

VCCA = 1.2 ± 0.1 V, VCCB = 3.3 ± 0.3 V

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|--------------------------------------|--------------------|-----|-----|------|
| Propagation delay time (A1 → B1) | t _{pLH} t _{pHL} | Figure 1, Figure 2 | 1.0 | 22 | ns |
| 3-state output enable time (\overline{OE} → B1) | t _{pZL} t _{pZH} | Figure 1, Figure 3 | 1.0 | 52 | |
| 3-state output disable time (\overline{OE} → B1) | t _{pLZ} t _{pHZ} | Figure 1, Figure 3 | 1.0 | 18 | |

$V_{CCA} = 1.8 \pm 0.15 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|------------------------|--------------------|-----|------|------|
| Propagation delay time (A1 → B1) | t_{pLH} t_{pHL} | Figure 1, Figure 2 | 1.0 | 9.5 | ns |
| 3-state output enable time (\overline{OE} → B1) | t_{pZL} t_{pZH} | Figure 1, Figure 3 | 1.0 | 12.6 | |
| 3-state output disable time (\overline{OE} → B1) | t_{pLZ} t_{pHZ} | Figure 1, Figure 3 | 1.0 | 5.1 | |

 $V_{CCA} = 1.5 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|------------------------|--------------------|-----|------|------|
| Propagation delay time (A1 → B1) | t_{pLH} t_{pHL} | Figure 1, Figure 2 | 1.0 | 10.5 | ns |
| 3-state output enable time (\overline{OE} → B1) | t_{pZL} t_{pZH} | Figure 1, Figure 3 | 1.0 | 15.4 | |
| 3-state output disable time (\overline{OE} → B1) | t_{pLZ} t_{pHZ} | Figure 1, Figure 3 | 1.0 | 6.4 | |

 $V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 2.5 \pm 0.2 \text{ V}$

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|------------------------|--------------------|-----|-----|------|
| Propagation delay time (A1 → B1) | t_{pLH} t_{pHL} | Figure 1, Figure 2 | 1.0 | 23 | ns |
| 3-state output enable time (\overline{OE} → B1) | t_{pZL} t_{pZH} | Figure 1, Figure 3 | 1.0 | 54 | |
| 3-state output disable time (\overline{OE} → B1) | t_{pLZ} t_{pHZ} | Figure 1, Figure 3 | 1.0 | 17 | |

 $V_{CCA} = 1.2 \pm 0.1 \text{ V}$, $V_{CCB} = 1.8 \pm 0.15 \text{ V}$

| Characteristics | Symbol | Test Condition | Min | Max | Unit |
|--|------------------------|--------------------|-----|-----|------|
| Propagation delay time (A1 → B1) | t_{pLH} t_{pHL} | Figure 1, Figure 2 | 1.0 | 30 | ns |
| 3-state output enable time (\overline{OE} → B1) | t_{pZL} t_{pZH} | Figure 1, Figure 3 | 1.0 | 55 | |
| 3-state output disable time (\overline{OE} → B1) | t_{pLZ} t_{pHZ} | Figure 1, Figure 3 | 1.0 | 17 | |

Capacitive Characteristics (Ta=25°C)

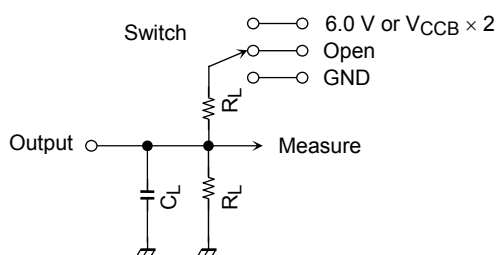
| Characteristics | Symbol | Test Condition | | | Typ. | Unit |
|---|------------------|------------------------------|----------------------|----------------------|------|------|
| | | | V _{CCA} (V) | V _{CCB} (V) | | |
| Input capacitance | C _{IN} | $\overline{\text{OE}}$, A1 | 2.5 | 3.3 | 7 | pF |
| Output capacitance | C _{OUT} | B1 | 2.5 | 3.3 | 8 | pF |
| Power dissipation capacitance (Note) | C _{PDA} | $\overline{\text{OE}}$ = "L" | 2.5 | 3.3 | 3 | pF |
| | | $\overline{\text{OE}}$ = "H" | 2.5 | 3.3 | 0 | |
| | C _{PDB} | $\overline{\text{OE}}$ = "L" | 2.5 | 3.3 | 13 | |
| | | $\overline{\text{OE}}$ = "H" | 2.5 | 3.3 | 0 | |

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(\text{opr})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per bit)}$$

AC Test Circuit



| Parameter | Switch |
|-------------------------------------|---|
| t _{pLH} , t _{pHL} | Open |
| t _{pLZ} , t _{pZL} | 6.0 V @ V _{CCB} =3.3±0.3V |
| | V _{CCB} × 2 @ V _{CCB} =2.5±0.2V |
| | @ V _{CCB} =1.8±0.15V |
| t _{pHZ} , t _{pZH} | GND |

| Symbol | V _{CCB} (output) | |
|----------------|----------------------------|--------------|
| | 3.3 ± 0.3 V 2.5 ± 0.2 V | 1.8 ± 0.15 V |
| R _L | 500 Ω | 1 kΩ |
| C _L | 30 pF | 30 pF |

Figure 1

The diagram illustrates the timing characteristics of a CMOS inverter. The input signal (A1) is a square wave with a rise time $t_r = 2.0 \text{ ns}$ and a fall time $t_f = 2.0 \text{ ns}$. The input voltage levels are V_{IH} (high) and V_{IL} (low). The output signal (B1) is also a square wave, but with a different shape due to the inverter's characteristics. The output voltage levels are V_{OH} (high) and V_{OL} (low). The output signal shows a delay time t_{pLH} (propagation delay from low to high) and a delay time t_{pHL} (propagation delay from high to low). The output signal also shows a rise time t_r and a fall time t_f . The input signal is labeled with 90% and 10% levels, and the output signal is labeled with V_{IM} and V_{OM} levels.

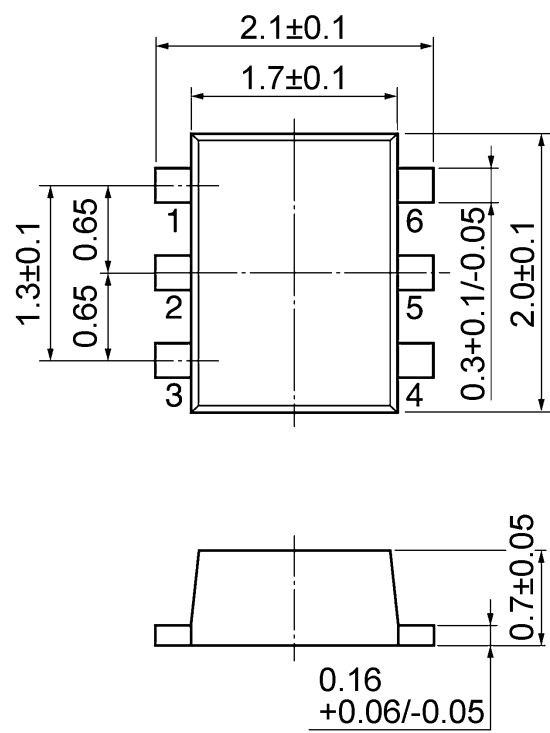
Timing diagram for the 74VHC125 tri-state buffer. The diagram shows three signals: Output Enable Control (\overline{OE}), Output (B1) Low to off to Low, and Output (B1) High to Off to High. The OE signal has a rise time (t_r) and fall time (t_f) of 2.0 ns. The output signal shows the transition from Low to High when OE is asserted. Key parameters include propagation delay (t_{pLZ} , t_{pLH} , t_{pHZ} , t_{pZH}), output voltage levels (V_{IM} , V_{OM} , V_{OH} , V_{OL}), and the output voltage swing (V_X , V_Y).

| | Symbol | V _{CCA} , V _{CCB} | | |
|--------|-----------------|-------------------------------------|-----------------------------|----------------------------|
| | | 3.3 ± 0.3 V | 2.5 ± 0.2 V 1.8 ± 0.15 V | 1.5 ± 0.1 V 1.2 ± 0.1 V |
| Input | V _{IH} | - | V _{CCA} | V _{CCA} |
| | V _{IM} | - | V _{CCA} / 2 | V _{CCA} / 2 |
| Output | V _{OM} | V _{OH} / 2 | V _{OH} / 2 | - |
| | V _X | V _{OL} + 0.3 V | V _{OH} + 0.15 V | - |
| | V _Y | V _{OH} - 0.3 V | V _{OH} - 0.15 V | - |

Package Dimensions

UF6

Unit: mm

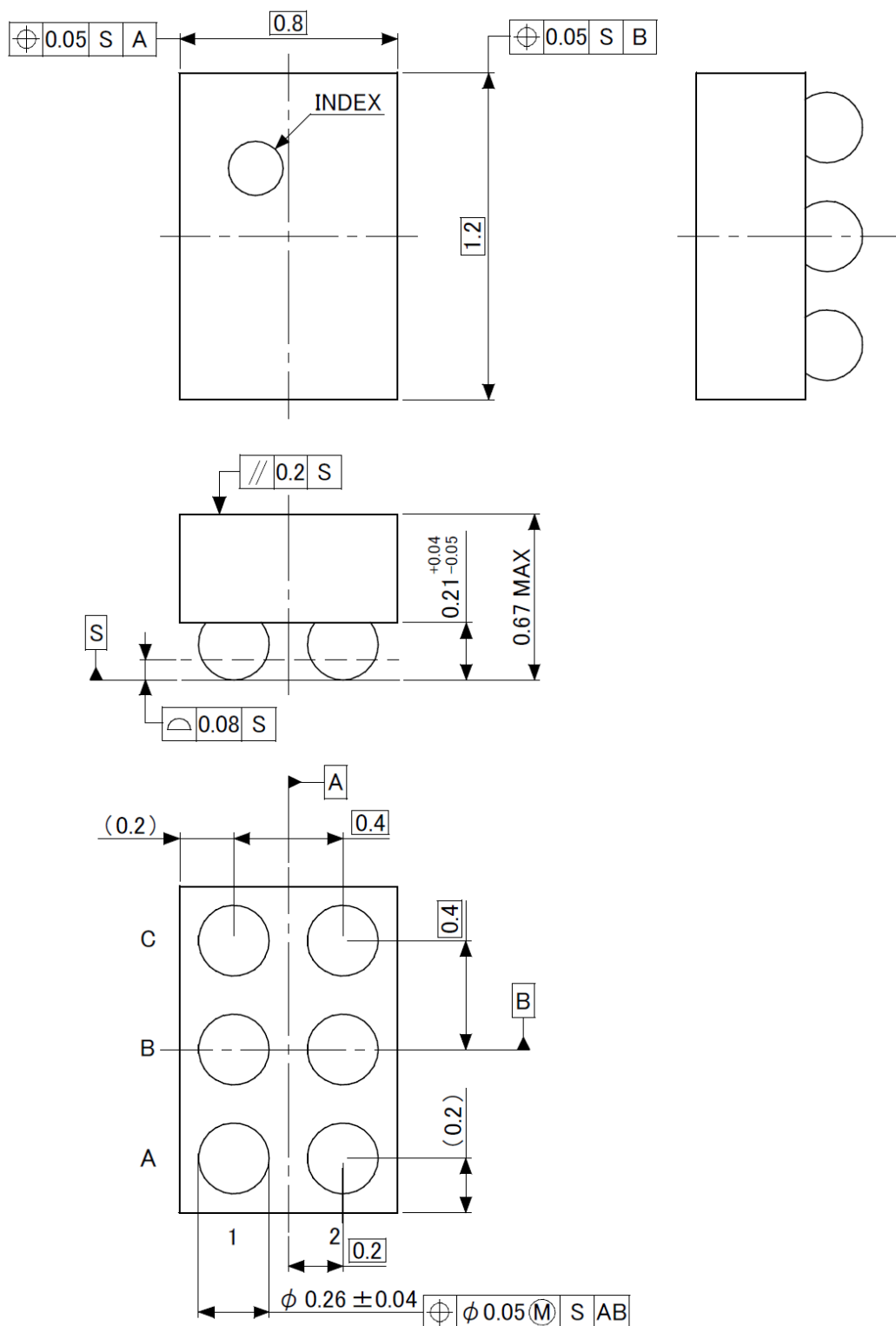


Weight: 0.007 g (typ.)

Package Dimensions

S-WFBGA6-0102-0.40A01

“Unit : mm”



Weight: 0.001 g (typ.)

The resins used in this product include no flame retardants.

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