AAT2612

SwitchReg™

Step-Down DC/DC Converter With Three High PSRR LDOs

General Description

The AAT2612 is a multiple rail power management IC. It integrates a 600mA high-frequency switching-converter and three 300mA linear regulators. The switching power supply is a highly-integrated monolithic step-down converter operating at 1.5MHz, achieving high efficiency with small external components. The three linear regulators are high PSRR low dropout regulators (LDOs) providing accurate regulation and excellent transient response.

The step down converter is programmable with external feedback resistors, and the three LDOs are fixed voltage outputs of six combinations for 1.8V, 2.8V, 3.0V and 3.3V. Integrated over-current or over-temperature protection circuitry becomes active as appropriate, when either fault occurs, and the AAT2612 recovers automatically when the fault is removed.

The AAT2612 is available in a Pb-free, thermally enhanced 20-pin TQFN33 package.

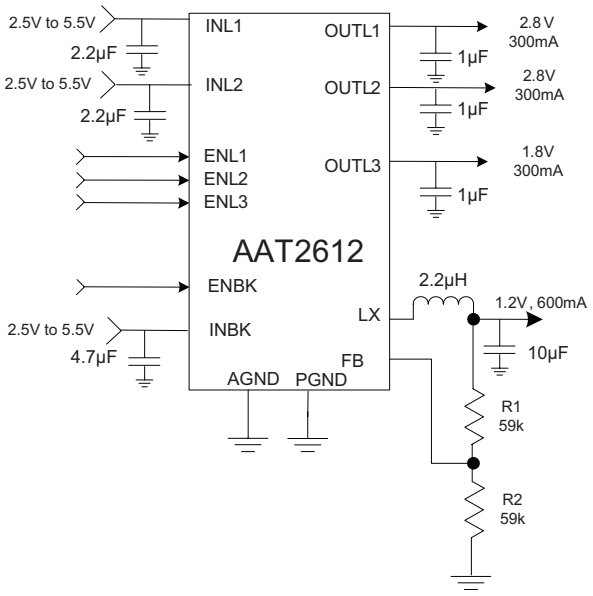
Features

- Current Mode Control DC/DC Converter:
  - Programmable Output Up to 600mA
  - 1.5MHz Switching Frequency
  - Up to 90% Efficiency
  - Integrated Switching Power FETS
  - Integrated Compensation Network
  - Internal Current Limit
- 3 Low Dropout Regulators with Separate Enable Pins:
  - 300mA per Channel
  - High PSRR
  - Factory Programmable Output
- Integrated Soft-Start
- Over-Current Protection
- Over-Thermal Protection
- TQFN33-20 Package

Applications

- Cellular Phones
- I/O Power
- Memory Power
- Processor Core Power
- Smart Handheld Devices

Typical Application

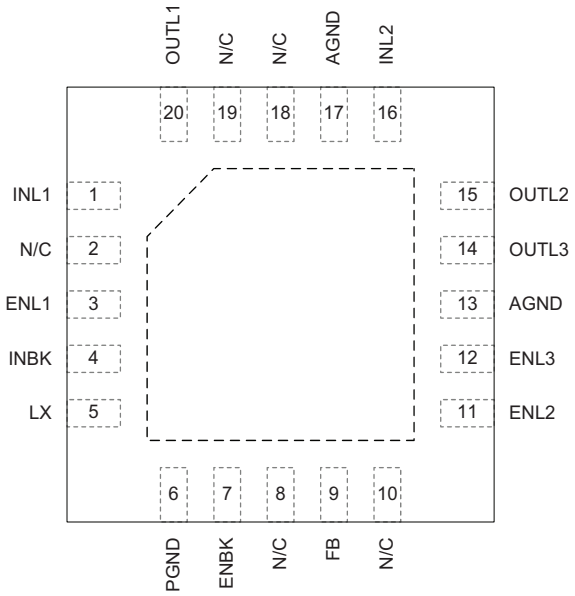


Pin Descriptions

Pin #	Symbol	Function	Description
1	INL1	I	Power input for LDO1. Connect a 2.2µF capacitor between this pin and ground.
2, 8, 10, 18, 19	N/C		Not Connected
3	ENL1	I	Active high enable pin. When pulled high, LDO1 regulates its output to the programmed voltage value.
4	INBK	I	Power input pin for the switching converter. Connect a 4.7µF capacitor between ground and INBK.
5	LX	I/O	DC/DC step-down converter switching node. Connect LX to the terminal of the inductor.
6	PGND		DC/DC converter power ground.
7	ENBK	I	Active high step-down DC/DC converter enable pin.
9	FB	I	DC/DC converter output feedback pin. Connect to a resistor divider for an adjustable output voltage.
11	ENL2	I	Active high enable pin. When pulled high, LDO2 regulates its output to the programmed voltage value.
12	ENL3	I	Active high enable pin. When pulled high, LDO3 regulates its output to the programmed voltage value.
13,17	AGND		Analog ground.
14	OUTL3	O	LDO3 output. Connect a 1µF capacitor between the pin and ground.
15	OUTL2	O	LDO2 output. Connect a 1µF capacitor between the pin and ground.
16	INL2	I	Power input for LDO2/3. Connect a 2.2µF capacitor between the pin and ground.
20	OUTL1	O	LDO1 output. Connect a 1µF capacitor between the pin and ground.
EP	GND		Exposed pad.

Pin Configuration

TQFN33-20
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
	INL1, INL2, INBK, OUTL1, OUTL2, OUTL3	-0.3 to 6.0	V
	ENL1, ENL2, ENL3	-0.3 to 6.0	
	ENBK, FB	-0.3 to V_{INBK}	
	LX to PGND	-0.3 to V_{INBK}	
	PGND to AGND, AGND to AGND	-0.3 to +0.3	
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_S	Storage Temperature Range	-65 to 150	
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec.)	300	

Thermal Information[2]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance[3]	50	°C/W
P_D	Maximum Power Dissipation	2	W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied.
2. Mounted on an FR4 board.
3. Thermal Resistance measured with the device on multi-layer evaluation board in a thermal oven. The amount of power dissipation which will cause the thermal shutdown to activate will depend on the ambient temperature and the PC board layout ability to dissipate the heat. De-rate 30mW/°C above 70°C.

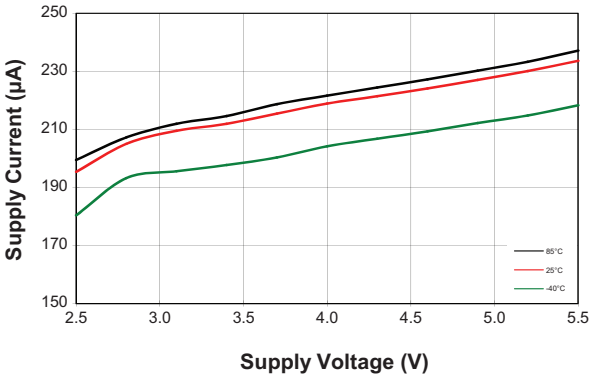
Electrical Characteristics[1]

V_{INBK} = V_{INL1} = V_{INL2} = 3.6V, L = 2.2µH, $C_{INL1, 2}$ = 2.2µF, C_{INBK} = 4.7µF, C_{OUTBK} = 10µF, $C_{OUTL1, 2, 3}$ = 1µF, T_A= 25°C unless otherwise noted.

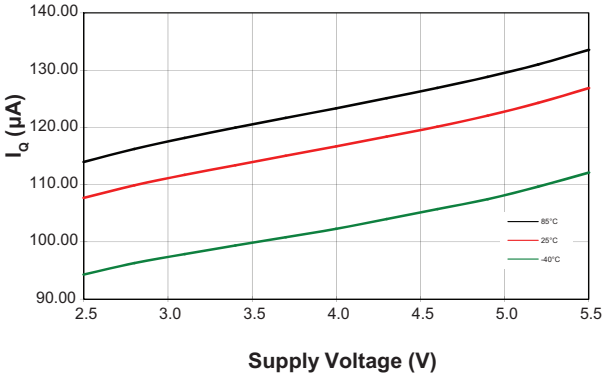
Symbol	Description	Conditions			Min	Typ	Max	Units
PMU Operation								
V_{IN}	Input Voltage				2.5		5.5	V
UVLO	Under-Voltage Lockout	Rising				1.9		V
		Hysteresis				150		mV
T_{SD}	Thermal Shutdown	Threshold				140		°C
		Hysteresis				15		°C
I_Q	Quiescent Current	V_{ENBK} > 1.5V, $V_{ENL1,2,3}$ >1.5V, no load				220	420	µA
Logic Control								
V_{IH}	Input Logic High Threshold	ENL1, ENL2, ENL3, ENBK			1.5		V_{INBK}	V
V_{IL}	Input Logic Low Threshold	ENL1, ENL2, ENL3, ENBK					0.4	V
DC-DC Step-Down Converter								
I_{SHDN}	Shutdown Current from INBK Pin	V_{ENBK} < 0.4V, $V_{ENL\ 1,\ 2,\ 3}$ < 0.4V				0.1	1	µA
I_Q	Quiescent Current	$V_{ENL\ 1,\ 2,\ 3}$ < 0.4V , V_{ENBK} >1.5V , I_{OUTB} = 0mA				120	280	µA
I_{LIM}	P-Channel Current Limit	V_{INBK} = 2.7V to 5.5V			800			mA
V_{OUT}	Output Voltage Range				0.9		85%·V_{INBK}	V
V_{FB_ACC}	Feedback Voltage Accuracy	T_A = -40°C to 85°C			0.585	0.600	0.615	V
f_{SW}	Operating Switching Frequency					1.5		MHz
$R_{DS(ON)H}$	High-Side Switch On Resistance	I_{OUTB} = 200mA				230		mΩ
		I_{OUTB} = 200mA, V_{INBK} = 2.5V				280		
$R_{DS(ON)L}$	Low-Side Switch On Resistance	I_{OUTB} = 200mA				180		mΩ
		I_{OUTB} = 200mA, V_{INBK} = 2.5V				220		
LDO								
I_{SHDN}	Shutdown Current	V_{ENBK} = V_{ENL} < 0.4V					1	µA
I_{LIM}	Output Current Limit	R_{LOAD} = 1Ω				450	600	mA
V_{DROP}	Dropout Voltage	I_{OUTL} = 300mA					500	mV
V_{OUTL_ACC}	Output Voltage Accuracy	T_A = -40°C to 85°C, 1mA load			-3		3	%
$\Delta V_{OUTL}/\Delta I_{OUTL}$	Load Regulation	1mA < I_{OUTL} < 300mA				0.3	0.6	%
$\Delta V_{OUTL}/\Delta V_{INL}$	Line Regulation	V_{INL1} = V_{INL2} = 2.7V to 5.5V					0.2	%/V
PSRR	Power Supply Rejection Ratio	$C_{OUT1,2,3}$ = 1µF, V_{INL} = $V_{OUTL1,2,3}$ + 1V	f = 100Hz	I_{OUT} = 10mA		75		dB
				I_{OUT} = 150mA		75		
			f = 1kHz	I_{OUT} = 10mA		70		
				I_{OUT} = 150mA		70		
			f = 10kHz	I_{OUT} = 10mA		50		
				I_{OUT} = 150mA		50		
V_{OUTL_TC}	Output Voltage Temperature Coefficient					100		ppm/°C

Typical Characteristics

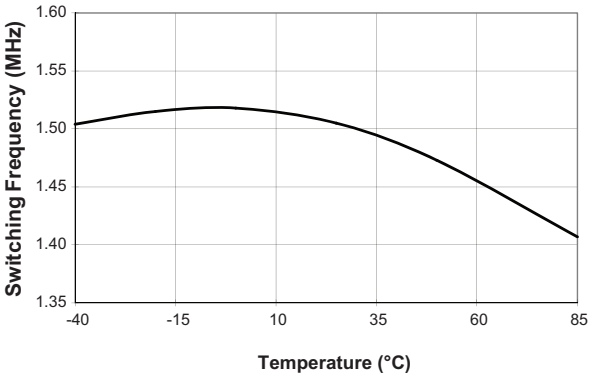
Supply Current vs Supply Voltage
(V_{ENB}, V_{ENL}> 1.5V)



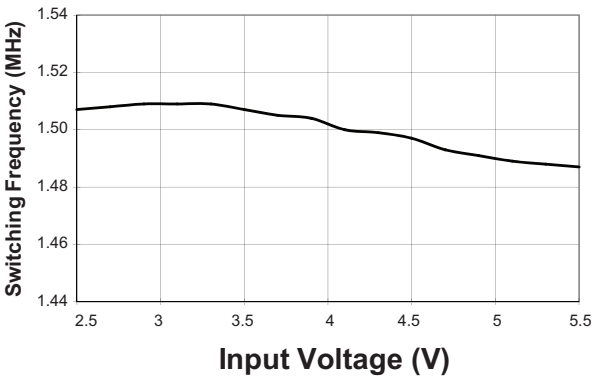
Buck Quiescent Current vs Supply Voltage
(V_{OUT}= 1.2V, V_{ENB}> 1.5V,V_{ENL}< 0.4V)



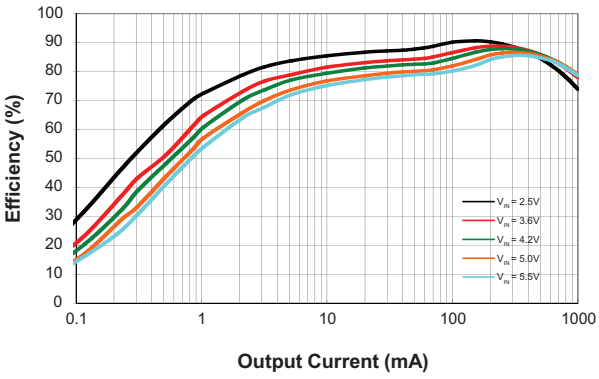
Switching Frequency vs Temperature
(V_{INB} = 3.6V, I_{OUT} = 600mA)



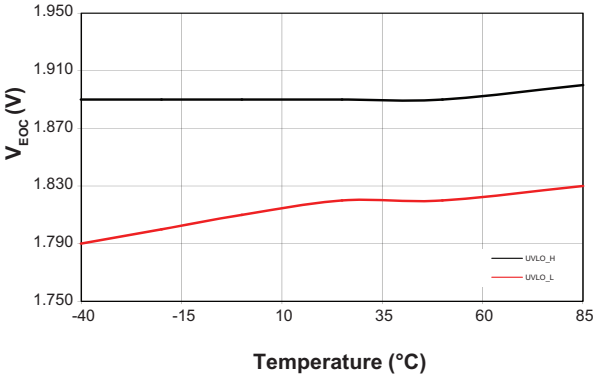
Switching Frequency vs Input Voltage
(V_{OUTB} = 1.2V, I_{OUTB} = 600mA)



Buck Efficiency vs Output Current
(V_{OUT} = 1.2V; L = 2.2µH)

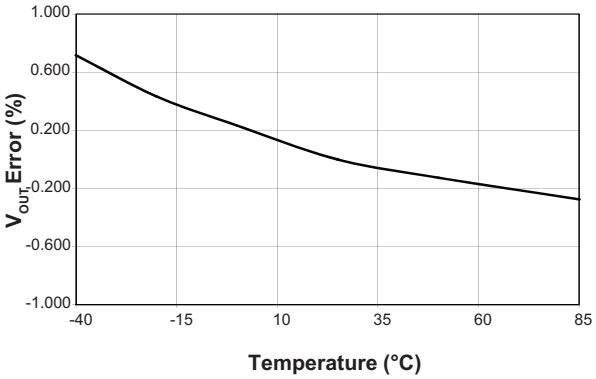


UVLO Volatge vs Temperature

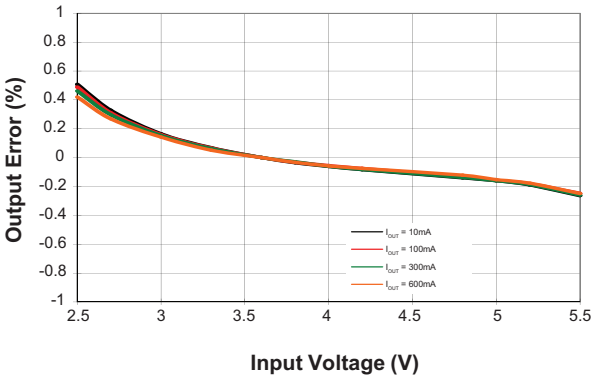


Typical Characteristics

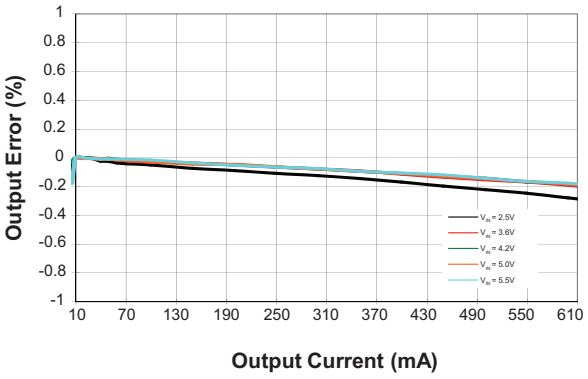
Buck Output Voltage vs Temperature
(V_{INB} = 3.6V; V_{OUTB} = 1.2V; L = 2.2µH)



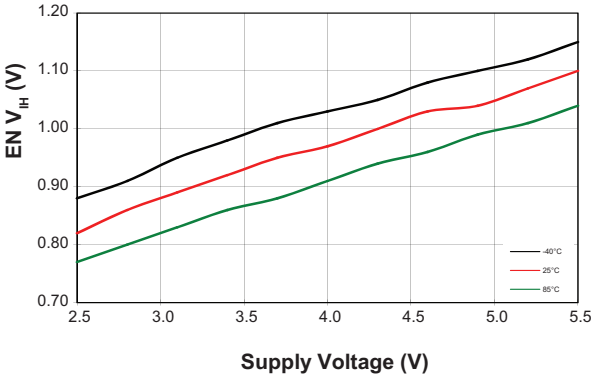
Buck Line Regulation
(V_{OUT} = 1.2V; L = 2.2µH)



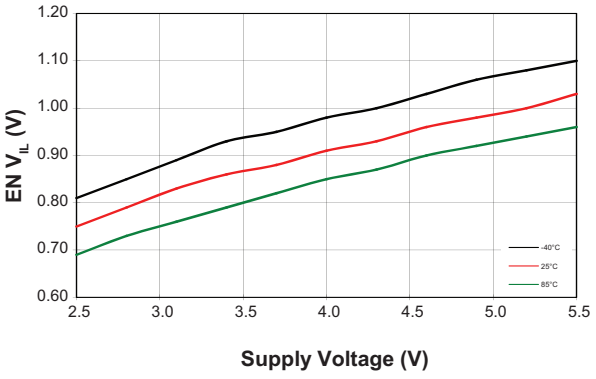
Buck Load Regulation
(V_{OUT} = 1.2V; L = 2.2µH)



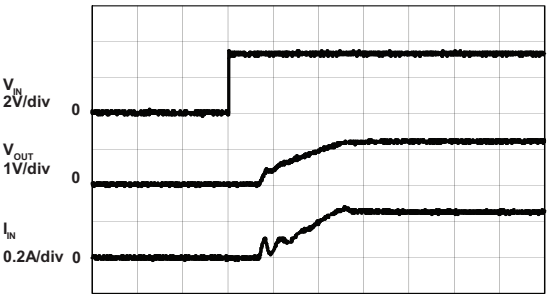
EN V_{IH} vs Supply Voltage



EN V_{IL} vs Supply Voltage

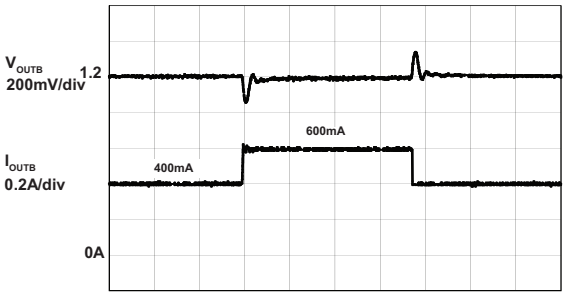


Softstart
(V_{IN} = 3.6V; V_{OUTB} = 1.2V; I_{OUTB} = 600mA)



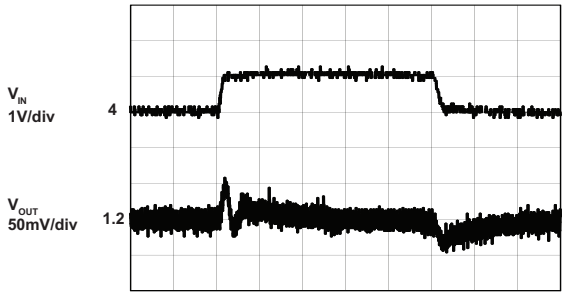
Typical Characteristics

Buck Load Transient
(V_{IN} = 3.6V, V_{OUTB} = 1.2V, C_{INB} = 10µF, C_{OUTB} = 10µF)

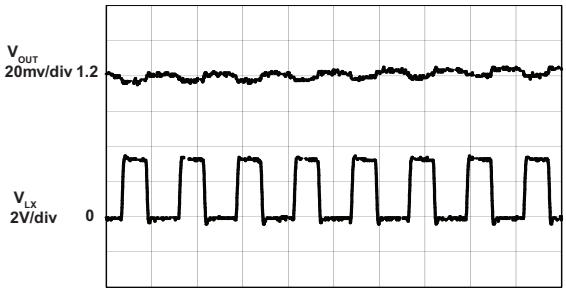


Time 40 µS/div

Buck Line Transient
(V_{INB} = 4V to 5V, I_{OUTB} = 600mA)

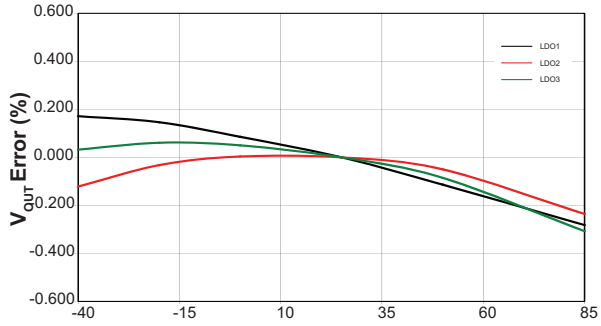


Output Ripple
(V_{IN} = 3.6V; V_{OUT} = 1.2V; I_{OUT} = 600mA; C_{INB} = 4.7µF)



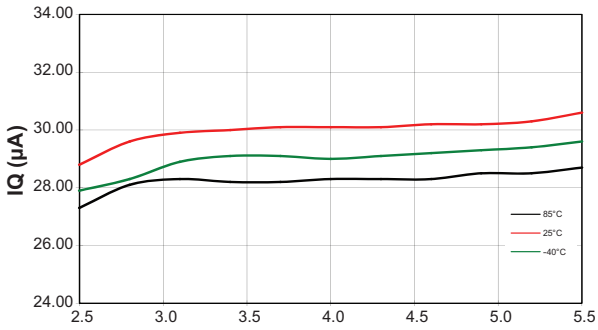
Time 0.4 µS/div

LDO Output Voltage vs Temperature
(V_{IN} = 3.6V)



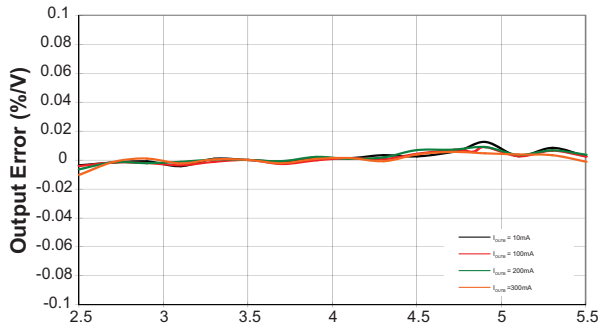
Temperature (°C)

LDO Quiescent Current vs Supply Voltage
(Single Channel)



Supply Voltage (V)

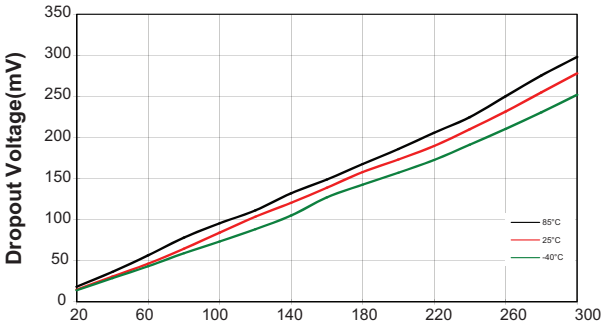
LDO Line Regulation
(V_{OUTL} = 1.8V)



Input Voltage (V)

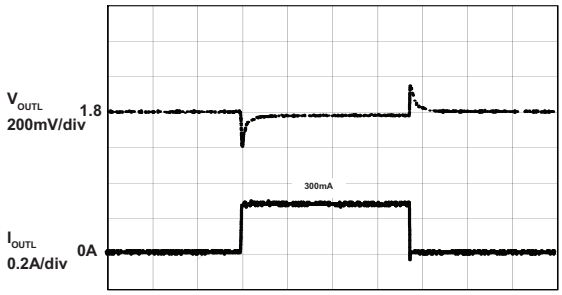
Typical Characteristics

Dropout Voltage vs Load Current
(V_{OUT} = 2.8V)



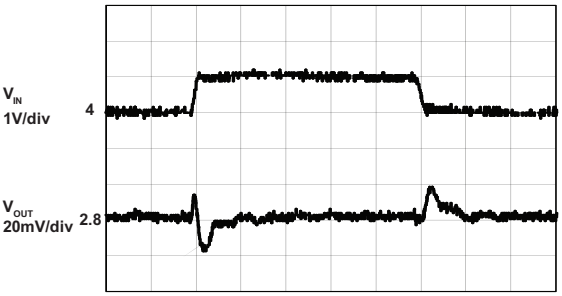
Load Current (mA)

LDO Load Transient
(V_{IN} = 3.6V, V_{OUTL} = 1.8V, C_{INL} = 2.2µF, C_{OUTL} = 1µF)



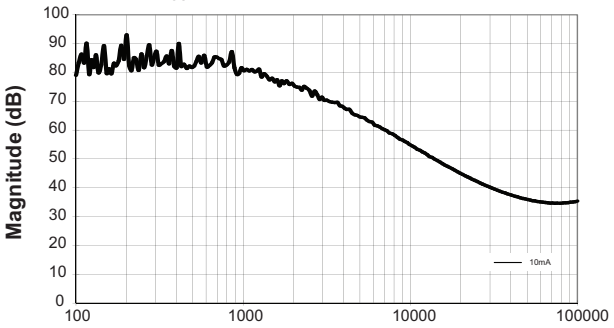
Time 100 µS/div

LDO Line Transient
(V_{INB} = 4V to 5V, I_{OUTL} = 300mA)



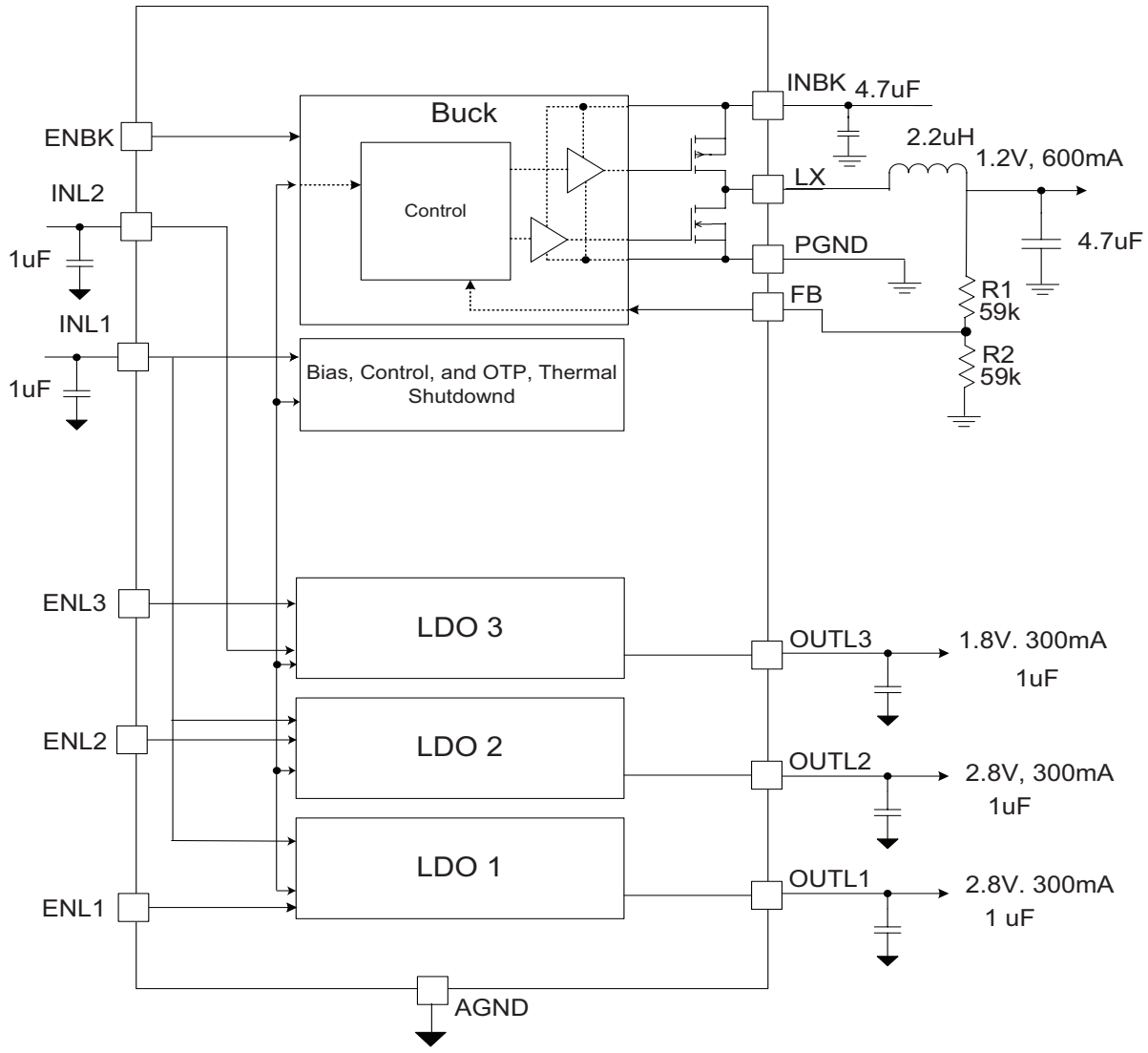
Time 20 µs/div

LDO1 Power Supply Rejection Ratio, PSRR
(I_{OUT1} = 10mA, BW = 100~100KHz)



Frequency (Hz)

Block Diagram



Functional Description

The AAT2612 is a compact power management solution. It integrates a step-down converter with three high PSRR low-dropout regulators to provide power from a wall adapter, USB port, or a single-cell Lithium Ion/Polymer battery or dual cell alkaline battery.

The AAT2612 uses fixed-frequency peak current control architecture. Light load mode is used to enhance light load efficiency. Compensation is integrated to reduce the number of external components and achieve excellent transient response and load/line regulation.

The ideal 1.5MHz switching frequency allows the use of smaller output filter components for improved power density, reduced external component size, and optimized output voltage ripple.

The AAT2612 has four separate enable pins to control buck converter and three LDO regulator outputs' startup. Also see the "Enable Function" section in the Applications Information section of this datasheet.

Synchronous Step-Down Converter

The AAT2612 contains one high performance 600mA, 1.5MHz synchronous step-down converter. The step-down converter operates to ensure high efficiency performance over all load conditions.

The input voltage range is from 2.5V to 5.5V, and the output voltage is programmable from 85% of V_{IN} to as low as 0.9V with external resistor divider. Power devices are sized for 600mA current capability while maintaining over 85% efficiency at full load. High efficiency is maintained at lower currents

A high DC gain error amplifier with internal compensation controls the output. It provides excellent transient response and load/line regulation. The converter has soft start control to limit inrush current.

Apart from the resistor divider and input capacitor, only a small L-C filter is required at the output side for the step-down converter to operate properly. Typically, a 2.2µH inductor and a 10µF ceramic capacitor are recommended for low output voltage ripple and small component size.

Control Loop

The converter is a peak current mode step-down converter. The inner, wide bandwidth loop controls the inductor peak current. The inductor current is sensed through the P-channel MOSFET (high side) and is also used for short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak inductor current to force a constant output voltage for all load and line conditions. The voltage feedback resistive divider is external and the error amplifier reference voltage is 0.6V. The voltage loop has a high DC gain making for excellent DC load and line regulation. The internal voltage loop compensation is located at the output of the transconductance voltage error amplifier.

Soft-Start

Soft start increases the inductor current limit point linearly when the input voltage or enable input is applied. It limits the current surge seen at the input and eliminates output voltage overshoot.

Current Limit and Over-Temperature Protection

For overload conditions the peak input current is limited. As load impedance decreases and the output voltage falls closer to zero, more power is dissipated internally, raising the device temperature. Thermal protection completely disables switching when internal dissipation becomes excessive, protecting the device from damage. The junction over-temperature threshold is 140°C with 15°C of hysteresis.

LDO Regulator

The advanced circuit design of the linear regulator is specifically optimized for very fast start-up and shutdown timing. This proprietary LDO is also tailored for superior transient response characteristics. These traits are particularly important for applications which require fast power supply timing.

The high-speed turn-on capability is enabled through the implementation of a fast start control circuit, which accelerates the power up behavior of fundamental control and feedback circuits within the LDO regulator. Fast turn-off time response is achieved by an active output pull down circuit, which is enabled when the LDO regulator is placed in the shutdown mode. This active fast shutdown circuit has no adverse effect on normal device operation. The LDO regulator output has been specifically optimized to function with low cost, low ESR ceramic capacitors. However, the design will allow for operation over a wide range of capacitor types.

The regulator comes with complete short circuit and thermal protection. The combination of these two internal protection circuits gives a comprehensive safety system to guard against extreme adverse operating conditions.

Application Information

Step-down Converter

Input Capacitor

Select a 4.7uF to 10uF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor value and size, determine the acceptable input ripple voltage level (V_{pp}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot f_S}$$

$$D = \frac{V_O}{V_{IN}}$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot f_S}$$

Where C_{IN} is the input capacitance, V_{IN} is the input voltage, V_O is the output voltage, f_S is the switching frequency, I_O is the output current, ESR is the equivalent series resistor of output capacitor, and D is the duty cycle.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$I_{RMS} = \frac{I_O}{2}$$

The maximum input voltage ripple also appears at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2612. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize parasitic inductances, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitors (C1, C2, and C3) is shown in the evaluation board layout in Figure 2.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors can also result in the loop phase and gain measurements. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic capacitor should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A typical 4.7µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot f_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

Output Inductor

For most designs, the AAT2612 operates with inductor values of 2.2µH to 4.7µH. Inductors with low inductance values are physically smaller but generate higher inductor current ripple leading to higher output voltage ripple. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Where ΔI_L is inductor ripple current. Large value inductors result in lower ripple current and small value inductors result in high ripple current. Choose inductor ripple current approximately 30% of the maximum load current 0.6A, or

$$\Delta I_L = 180mA$$

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. The DC current rating of the inductor should be at least equal to the maximum load current plus half the inductor ripple current to prevent core saturation (0.6A + 180mA).

Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Feedback Resistor Selection

The Buck output voltage on the AAT2612 is adjustable with external resistors R1 and R2 which program the output to regulate at a voltage in the range of 0.9V to 0.85 · V_{INBK}. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. The maximum value of R1 should be below 1Mohm to keep reference voltage normal and avoid noise coupling.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{V_{OUT}}{0.6V} - 1\right) \cdot R2$$

Table 1 shows the standard 1% metal film resistor values for different step-down output voltages

V_{OUT} (V)	R2 = 59kΩ, R1 (kΩ)
1.2	59
2.8	216
3.3	265.5
3.6	259
4.2	354

Table 1: V_{OUT} Resistor Selection

Enable Function

The AAT2612 features one buck output enable/disable function for buck converter. This pin (ENBK) is active high and is compatible with CMOS logic. To assure the buck output will switch on, the ENBK turn-on control level must be greater than 1.5V. The buck converter will go into the disable shutdown mode when the voltage on the ENBK pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the buck output in a continuously on state.

Low Dropout Regulator

Input Capacitor

Typically, a 2.2µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the LDO is physically located any distance more than one or two centimeters from the input power source, a C_{IN} capacitor will be needed for stable operation. C_{IN} should be located as closely to the device V_{INL} pin as practically possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the power supply ripple rejection.

Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN} as there is no specific capacitor ESR requirement. For better performance, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between pins VOUT and GND. The C_{OUT} capacitor connection to the LDO regulator ground pin should be made as direct as practically possible for maximum device performance. The AAT2612 LDOs have been specifically designed to function with very low ESR ceramic capacitors. Although the device is intended to operate with these low ESR capacitors, it is stable over a very wide range of capacitor ESR, thus it

will also work with some higher ESR tantalum or aluminum electrolytic capacitors. For best performance, ceramic capacitors are recommended.

The value of C_{OUT} typically ranges from 1µF to 10µF. 1µF is sufficient for most operating conditions.

Enable Function

The AAT2612 features three LDO regulator enable/disable function for LDO1/2/3 respectively. These pins (ENL1, ENL2, and ENL3) are active high and are compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state.

Short-circuit and Thermal Protection

The AAT2612 LDOs are protected by both current-limiting and over-temperature protection circuitry. The internal short-circuit current limiting circuit is designed to activate when the output load demand exceeds the maximum rated output. If a short-circuit condition were to continually draw more than the current limit threshold, the LDO regulator's output voltage would drop to a level necessary to supply the current demanded by the load. Under short-circuit or other over-current operating conditions, the output voltage would drop and the AAT2612's die temperature would rapidly increase. Once the regulator's power dissipation capacity has been exceeded and the internal die temperature reaches approximately 140°C, the system thermal protection circuit will become active. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over-temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 140°C trip point.

The interaction between the short-circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

No-Load Stability

The AAT2612 LDO is designed to maintain output voltage regulation and stability under operational no-load conditions. This is an important characteristic for applications where the output current may drop to zero. An output capacitor is required for stability under no-load operating conditions. Refer to the Output Capacitor section of this datasheet for recommended typical output capacitor values.

Internal Power Supply

The AAT2612 internal circuitry uses INL1 as the internal power supply. The buck output will have no output when INL1 is not connected to power.

Thermal Calculations

There are three types of losses associated with the AAT2612 step-down converters: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, with continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{BUCK} = I_O^2 \cdot \left(R_{DS(ON)P} \cdot \frac{V_O}{V_{IN}} + R_{DS(ON)N} \cdot \left[1 - \frac{V_O}{V_{IN}}\right]\right) + t_{SW} \cdot f_S \cdot I_O \cdot V_{IN} + I_Q \cdot V_{IN}$$

Where I_Q is the step-down converter quiescent current, t_{sw} is the switching time, $R_{DS(ON)P}$ and $R_{DS(ON)N}$ are the high side and low side switching MOSFETs' on-resistance. V_{IN}, V_O and I_O are the input voltage, the output voltage and the load current.

Since $R_{DS(ON)}$, quiescent current and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

For all the LDOs,

$$P_{D(MAX)} = (V_{IN} - V_{OUT}) \cdot I_{OUT(MAX)}.$$

The total power losses of both step-down converter and LDOs can be expressed as

$$P_{TOTAL} = P_{BUCK} + P_{D(MAX)}.$$

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the package.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_A$$

Layout Considerations

The suggested PCB layout for the AAT2612 is shown in Figures 2(a) - 2(d). The following guidelines are recommended to ensure a proper layout:

1. Connect the input capacitors (C1, C2, C3) and output capacitors (C5, C6, C7, C8) as close as possible to the pins (INL1, INL2, INBK, VOUT) and power ground (AGND, PGND) to minimize any parasitic inductance in the switched current path which generates a large voltage spike during the switching interval.
2. Keep the power traces (GND, LX, and INBK) short, direct, and wide to allow large current flow. Place

sufficient multiple-layer pads when needed to change the trace layer.

3. Connect the output capacitor C8 and inductor L1 as close as possible to the device. Keep the connection of L1 to the LX pins as short as possible and route no signal lines under the inductor.
4. Separate the feedback traces or FB pin (Pin 9) from any power trace and connect as close as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation.
5. Keep the resistance of the trace from the load returns to PGND to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
6. Connect the ground pin of the exposed pad to AGND internal plane with multiple vias to decrease the effect of large power ground PGND noise on the analog ground.
7. Connect the ground pins of LDO output capacitors to AGND.

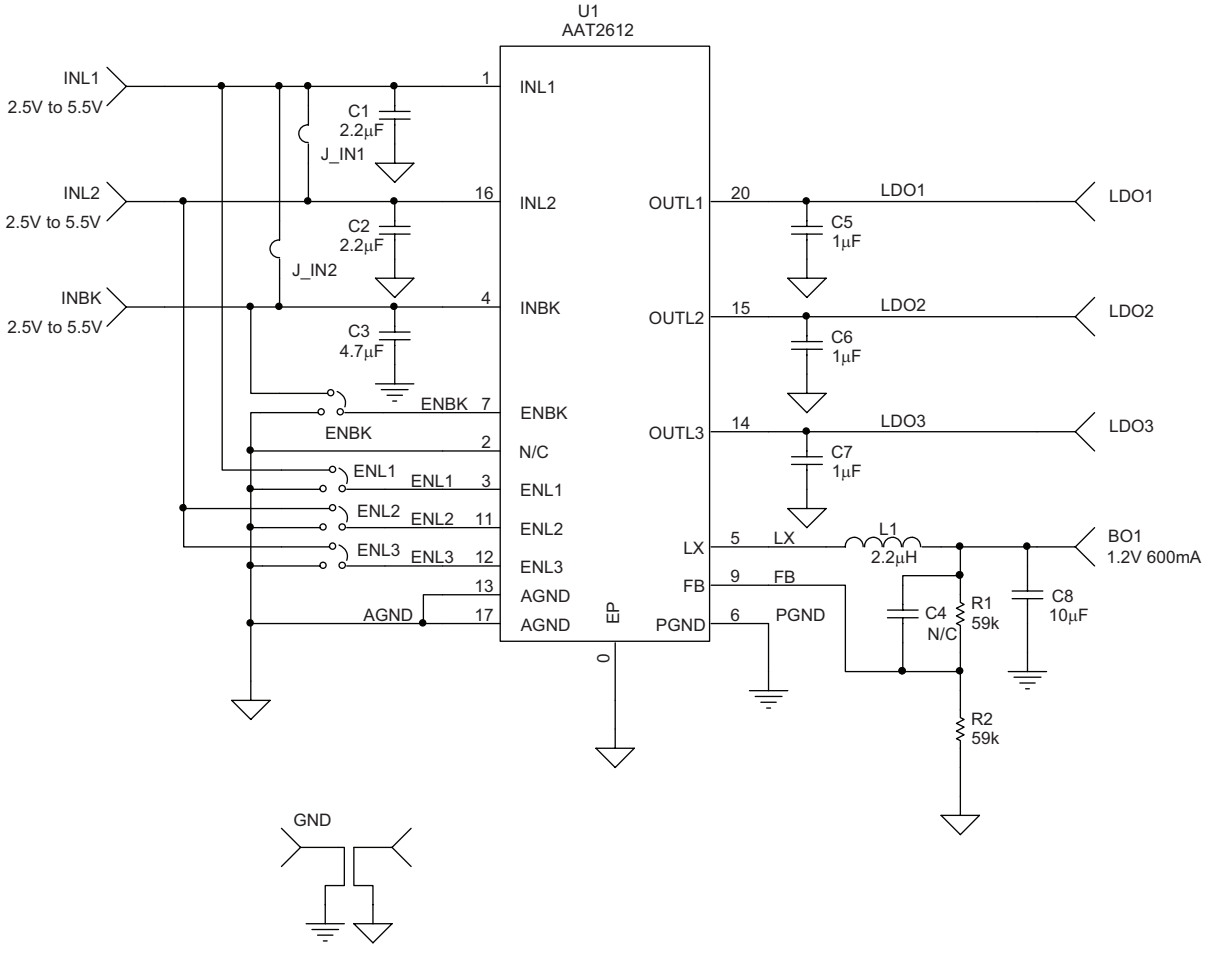
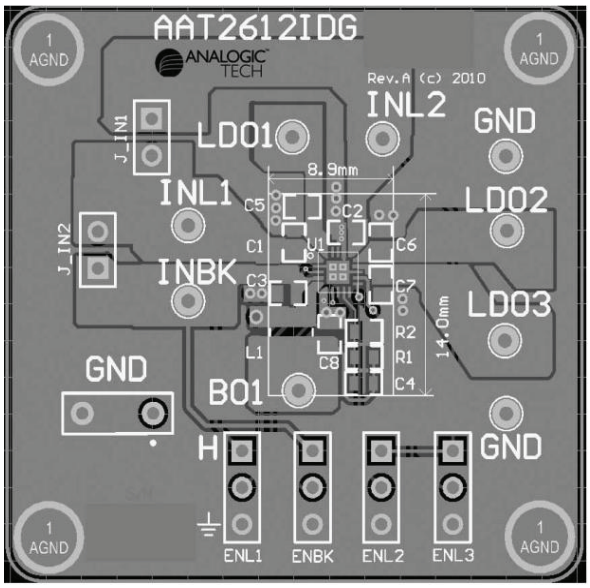
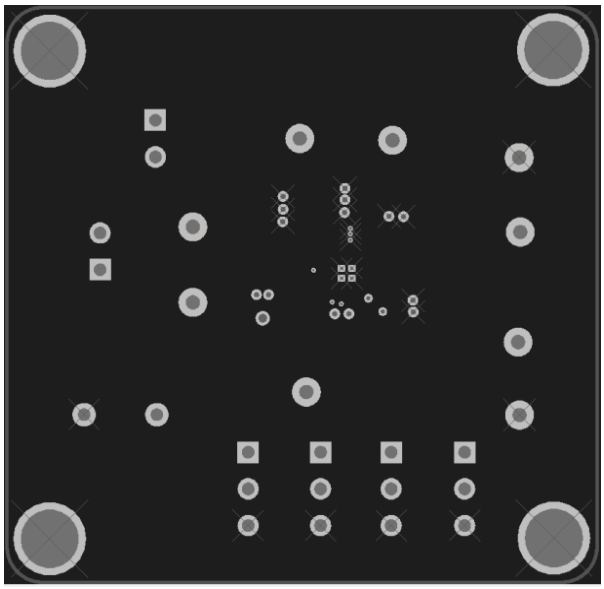


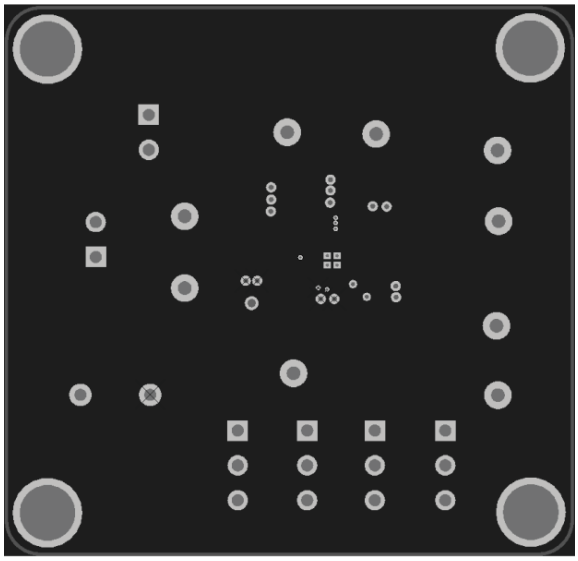
Figure 1: AAT2612IDG Evaluation Board Schematic.



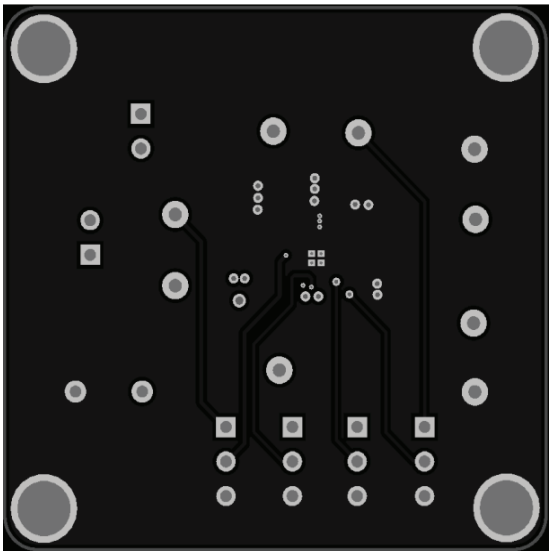
a: Top Side



b: Internal Plane 1 (AGND)



c: Internal Plane 2 (PGND)



d: Bottom Side

Figure 2: AAT2612IDG Evaluation Board Layout.

Component	Part Number	Description	Manufacturer
U1	AAT2612	Step-Down DC/DC Converter with Three High PSRR LDOs	AnalogicTech
C1, C2	GRM188R71A225KE15	Cap Ceramic 2.2µF 0603 X7R 10V 10%	Murata
C3	GRM188R60J475KE19	Cap Ceramic 4.7µF 0603 X5R 6.3V 10%	
C8	GRM188R60J106ME47	Cap Ceramic 10µF 0603 X5R 6.3V 10%	
C4, C5, C6, C7	GRM188R71C105KA12	Cap Ceramic 1µF 0603 X7R 6.3V 10%	
L1	LQH3NPN2R2MM0	2.2µH, 73mΩ, 1.25A, 20%	
R1, R2	RC0603FR-0759KL	Res, 59kΩ, 1/10W, 1%, 0603, SMD	Yageo

Table 2: AAT2612IDG Evaluation Board Bill of Materials (BOM).

Manufacturer	Part Number	L (µH)	Max DCR (mΩ)	Saturation Current (A)	Size WxLxH (mm)
Murata	LQH3NP2R2NG0	2.2	140	1.27	3.0x3.0x0.9
	LQH3NP3R3NG0	3.3	180	0.85	
	LQH3NP4R7NG0	4.7	260	0.8	
Coilcraft	LPA3015-222MLC	2.2	110	1.1	3.1x3.1x1.5
	LPA3015-332MLC	3.3	130	1.1	
	LPA3015-472MLC	4.7	200	0.9	

Table 3: Surface Mount Inductors.

Manufacturer	Part Number	Value (µF)	Voltage (V)	Tolerance	Temp. Co.	Case
Murata	GRM188R70J105K	1	6.3	10%	X7R	0603
	GRM188R70J106K	10	6.3	10%	X7R	0603
	GRM188R71A225K	2.2	10	10%	X7R	0603
	GRM188R71A475K	4.7	10	10%	X7R	0603
AVX	06036C105KAT	1	6.3	10%	X7R	0603
	06036C106KAT	10	6.3	10%	X7R	0603
	0603ZC225KAT	2.2	10	10%	X7R	0603
	0603ZC475KAT	4.7	10	10%	X7R	0603
KEMET	C0603C105K9RAC	1	6.3	10%	X7R	0603
	C0603C106K9RAC	10	6.3	10%	X7R	0603
	C0603C225K8RAC	2.2	10	10%	X7R	0603
	C0603C475K8RAC	4.7	10	10%	X7R	0603

Table 4: Surface Mount Capacitors.

Ordering Information

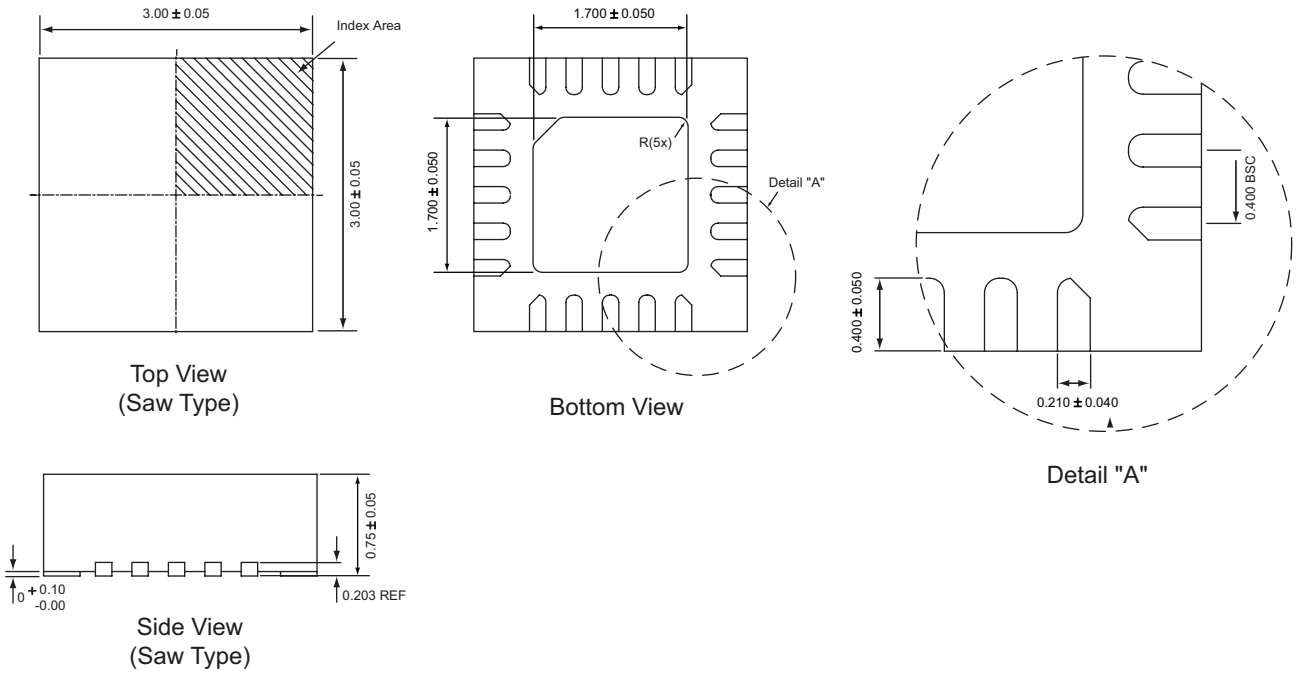
DC-DC Step-Down (V)	LDO1 (V)	LDO2 (V)	LDO3 (V)	Part Marking[1]	Part Number (Tape and Reel)[2, 3]
Adj	2.8	2.8	1.8	S2XYY	**AAT2612IDG-1-T1**
Adj	2.8	1.8	1.8	TBD	AAT2612IDG-2-T1
Adj	2.8	2.8	2.8	TBD	AAT2612IDG-3-T1
Adj	2.8	1.8	3.0	TBD	AAT2612IDG-4-T1
Adj	2.8	1.8	3.3	T5XYY	AAT2612IDG-5-T1
Adj	3.0	1.8	3.3	T6XYY	AAT2612IDG-6-T1

Pb-free

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/aboutus/quality.php.

Package Information

TQFN33-20[4]



All dimensions in millimeters.

1. A = assembly house code, Y = year, W = week.
2. Available exclusively outside of the United States and its territories.
3. Sample stock is generally held on part numbers listed in **BOLD**.
4. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
3230 Scott Boulevard, Santa Clara, CA 95054
Phone (408) 737-4600
Fax (408) 737-4611