Using SLG59H1401C and SLG59H1403C in PowerMUX and OR'ing Applications

This application note describes how to use Renesas SLG59H1401C and SLG59H1403C in PowerMUX and OR'ing applications. Corresponding oscilloscope captures of operational behavior are included.

Contents

1. Terms and Definitions

OV	Over Voltage
PowerMux	Power Multiplexer

2. References

Website: Load Switches | Renesas

[1] SLG59H1401C Datasheet

[2] SLG59H1403C Datasheet

3. Introduction

If an application requires two or more power sources, it requires a switching solution. Without the load switch, there is a danger of a power failure, a short circuit, and a loss of power. This issue is related to almost all portable devices that have an internal battery and a USB connector for charging. There is a need to switch between the battery and the external power supply. To do this, PowerMUX (Power Multiplexer) devices are typically used.

This application note shows the application solution of manual and automatic switching between two power sources using Renesas' High Voltage GreenFET™ SLG59H1401C or SLG59H1403C devices. The main difference between SLG59H1401C and SLG59H1403C is the maximum operating voltage range: up to 6 V for SLG59H1401C while up to 22 V for SLG59H1403C [1][2].

4. Power MUX General Concept

Power multiplexers or PowerMux are devices that provide a seamless transition between two or more power inputs. They are typically used in applications like computers, digital cameras, modems, cell phones, etc. It also may be used in battery management systems and peripheral power interface systems.

In general, PowerMux devices switch between 2 input power supplies to one common output supply rail and thus provide a continuous supply to the device. A simplified block diagram of PowerMux is illustrated in Figure 1.

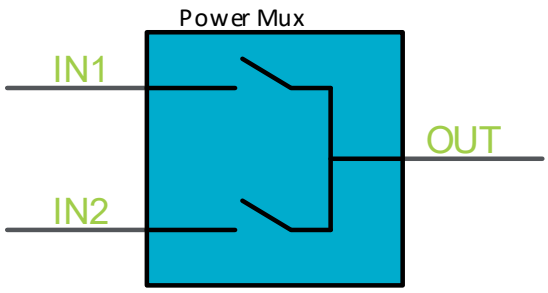

Figure 1: Power Mux Simplified Block Diagram

From a technical standpoint, PowerMux is typically implemented by controlling MOSFET's RDS_{ON} resistance because MOSFETs have high off isolation, which is important to prevent back-feeding power between two inputs.

From a controlling standpoint, the output power rail can be chosen manually or automatically.

A manual PowerMux is one in which each path is individually controlled by an external signal (logic or microcontroller). An example of Manual PowerMux with two enable inputs is shown in Figure 2 and such a method is generally used when there is a microcontroller that can decide under what conditions to enable each input. Renesas' SLG59H1401C and SLG59H1403C devices can be easily used in PowerMux applications, its detailed operation is described below.

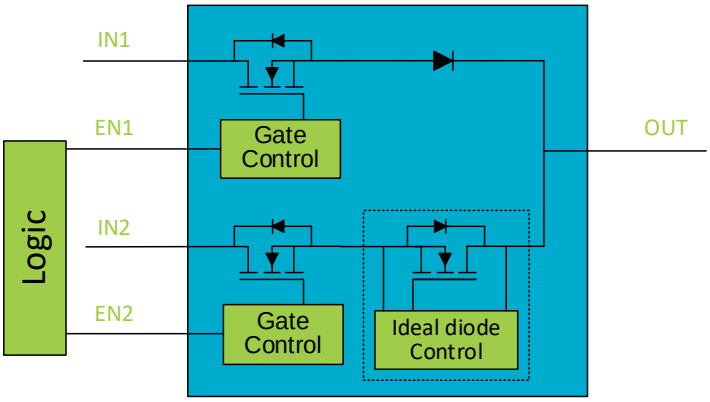

Figure 2: Manual PowerMux

4.1 Introduction to SLG59H1401C and SLG59H1403C

The SLG59H1401C and SLG59H1403C are specially designed for OR'ing or manual Power MUX applications. The parts have two 3 A rated load switches with common output that are well suited for a variety of systems having multiple power sources from 2.8 V and up to 6 V for SLG59H1401C and up to 22 V for SLG59H1403C. The devices will automatically detect, select, and seamlessly transition between available inputs. Additionally, manual switching between two power rails is also allowed.

The pin configuration for SLG59H1401C and SLG59H1403C is shown in Figure 3.

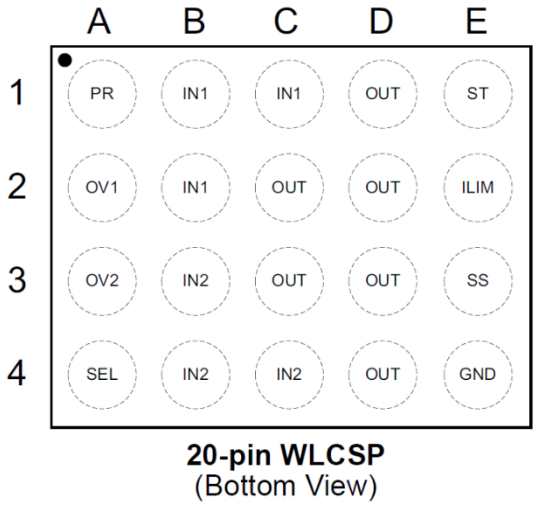

Figure 3: Pin configuration for SLG59H1401C and SLG59H1403C

The following list provides more detail on the function of each pin:

- **IN1** and **IN2** pins are the Input terminal of the load switch's Channel 1 and Channel 2 respectively. Capacitors at IN1 and IN2 should be rated at a voltage higher than the maximum input voltage ever present for each Channel respectively.
- **OUT** pin is the output terminal of the device.
- **GND** pin is a Ground connection. Connect this pin to the system analog or power ground plane.
- **PR** pin is an analog input that sets the priority to Channel 1. PR is compared to internal reference voltage V_{REF}. Connect to GND if not required.
- **SEL** pin is an analog input dedicated to overriding the priority and manually selecting IN2. SEL is compared to internal reference voltage V_{REF}. Connect to GND if not required.
- **OV1** (Over Voltage) and **OV2** pins are analog inputs which together with an external resistor divider for each pin, are used to set the overvoltage threshold for Channel 1 and Channel 2 respectively. OV1 and OV2 are compared to an internal reference voltage V_{REF}. If $V_{OV1} \geq V_{REF}$ or $V_{OV2} \geq V_{REF}$, Channel 1 or Channel 2 is turned off and returns to normal operation once $V_{OV1} < V_{REF}$ or $V_{OV2} < V_{REF}$. Connect to GND if not used.
- **ILIM** pin is dedicated to the Current Limit level. A 1%-tolerance resistor connected between ILIM and GND sets the load switch's active current limit for both channels. Please refer to the Setting the SLG59H1401C's and SLG59H1403C's Active Current Limit section in the datasheets.
- **SS pin** should be connected to a low-ESR, stable dielectric, ceramic surface-mount capacitor, that is connected to GND. This capacitor sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1401C and SLG59H1403C parts.
- **ST** is an open-drain, active LOW output that shows which channel is chosen. When asserted HIGH, IN1 is selected. When asserted LOW, IN2 is selected. Connect to GND if not required.

For more electrical characteristics please see SLG59H1401C and SLG59H1403C datasheets.

4.2 Using SLG59H1401C and SLG59H1403C in PowerMUX Applications

When using the SLG59H1401C or SLG59H1403C in a manual power rail selection application, an external voltage $V_{PR} > V_{REF}$ should be applied at the PR pin. PR is commonly connected to IN1 with an external resistor divider to provide a stable high logic level, and to prevent automatic switching of the output to a higher voltage when $V_{SEL} < V_{REF}$. If $V_{PR} > V_{REF}$ and $V_{SEL} < V_{REF}$, then IN1 will be selected on output and by toggling $V_{SEL} > V_{REF}$, IN2 will be selected on output.

OV1 and OV2 with external resistors connected to IN1 and IN2 respectively can be configured to additionally provide overvoltage protection.

A typical voltage divider, illustrated in Figure 4, is used to set the overvoltage threshold for OV1 and OV2, V_{PR} and V_{SEL} levels.

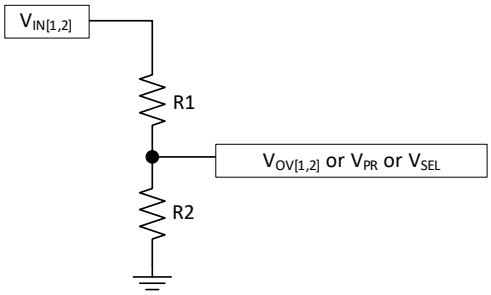

Figure 4: Voltage Divider Scheme

For voltage divider calculation, use the equation below:

$R1 = \frac{R2*(V_{IN[1,2]} - V_{REF})}{V_{REF}}$, where:

R1 - calculated resistor value in kΩ.

R2 – resistor closes to ground. Recommended R2 value is 5 kΩ.

$V_{IN[1,2]}$ - V_{IN1} or V_{IN2} voltage at which protection should be triggered;
V_{REF} - Internal voltage reference for OV1, OV2, PR, and SEL pins. $V_{OV[1,2]}$, V_{PR}, V_{SEL} - Internal voltage reference for OV1, OV2, PR, and SEL pins. Based on the datasheet, the typical value is 1.06 V.

Note: In the case of using SLG59H1403C in 22 V applications, please make sure that during the OVP event, the voltage on OV1, OV2, PR, and SEL pins do not exceed the Absolute Maximum Ratings.

The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the signal on the ST pin is high, IN1 will be at the output, or the output is Hi-Z. If the ST signal is low, IN2 will be at the output.

The following application scope shots below demonstrate the switchover behavior of the SLG59H1401C device for V_{IN1} = 5 V, V_{IN2} = 3.3 V. Overvoltage thresholds for OV1 are set at 5.74 V, and for OV2 are set to 3.74 V. A typical connection diagram for these conditions is illustrated in Figure 5.

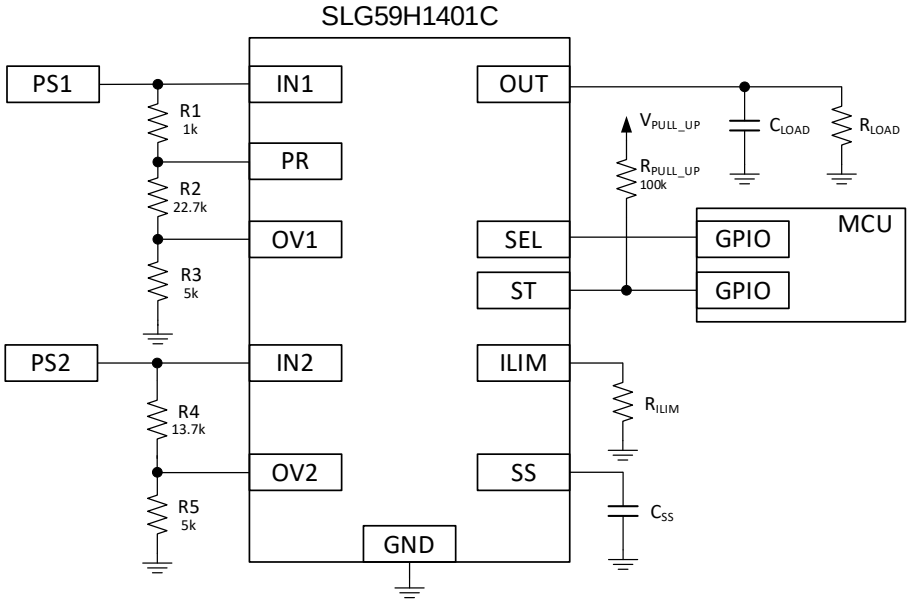

Figure 5: Connection Diagram of Using SLG59H1401C in PowerMUX Applications

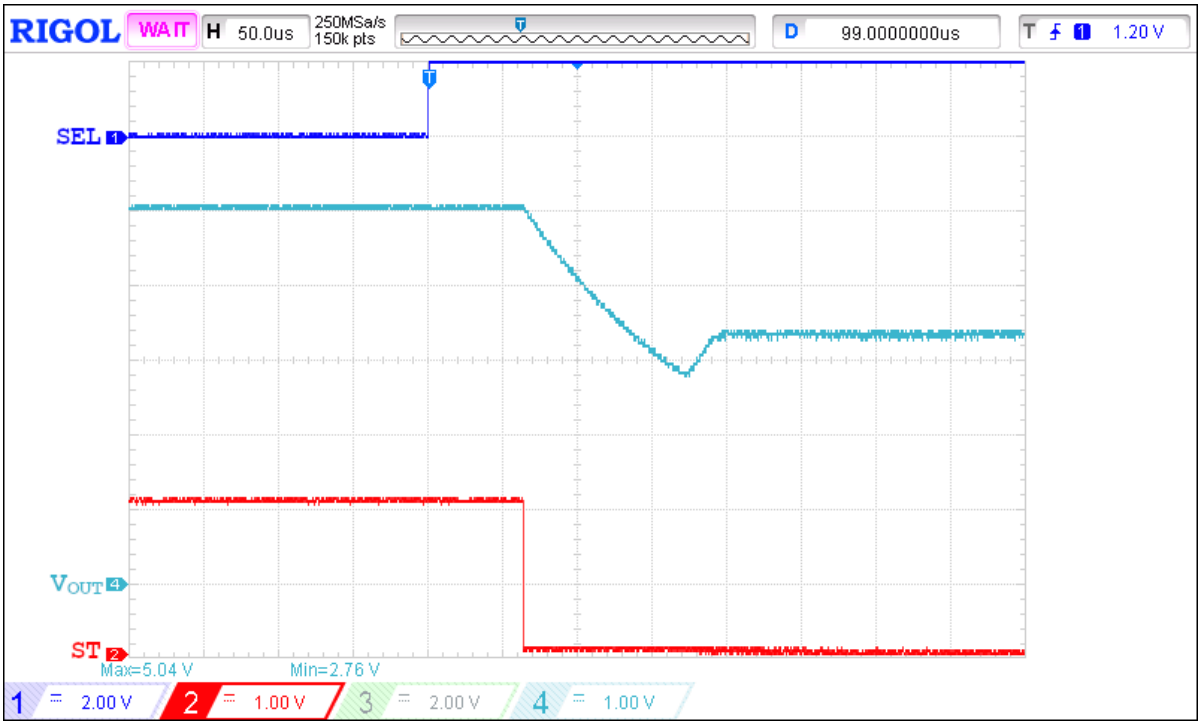

Figure 6: Switchover operation waveform for V_{IN1} = 5 V, V_{IN2} = 3.3 V, C_{SS} = 220 nF, PR = Low, SEL = Low → High, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

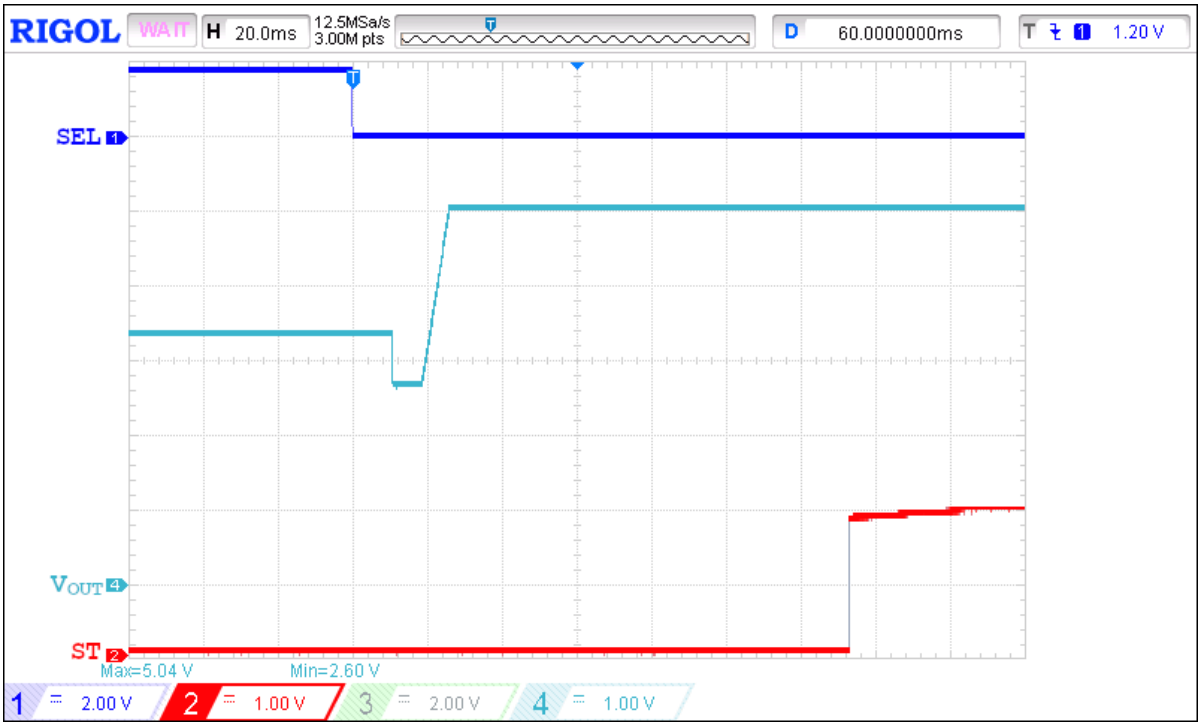

Figure 7: Switchover operation waveform for V_{IN1} = 5 V, V_{IN2} = 3.3 V, C_{SS} = 220 nF, PR = Low, SEL = High → Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

Similar application scope shots below demonstrate the switchover behavior of the SLG59H1401C device for V_{IN1} = 3.3 V, V_{IN2} = 5 V. Overvoltage thresholds for OV1 are set at 3.74 V, and for OV2 are set at 5.74 V. A typical connection diagram for these conditions is illustrated in Figure 8.

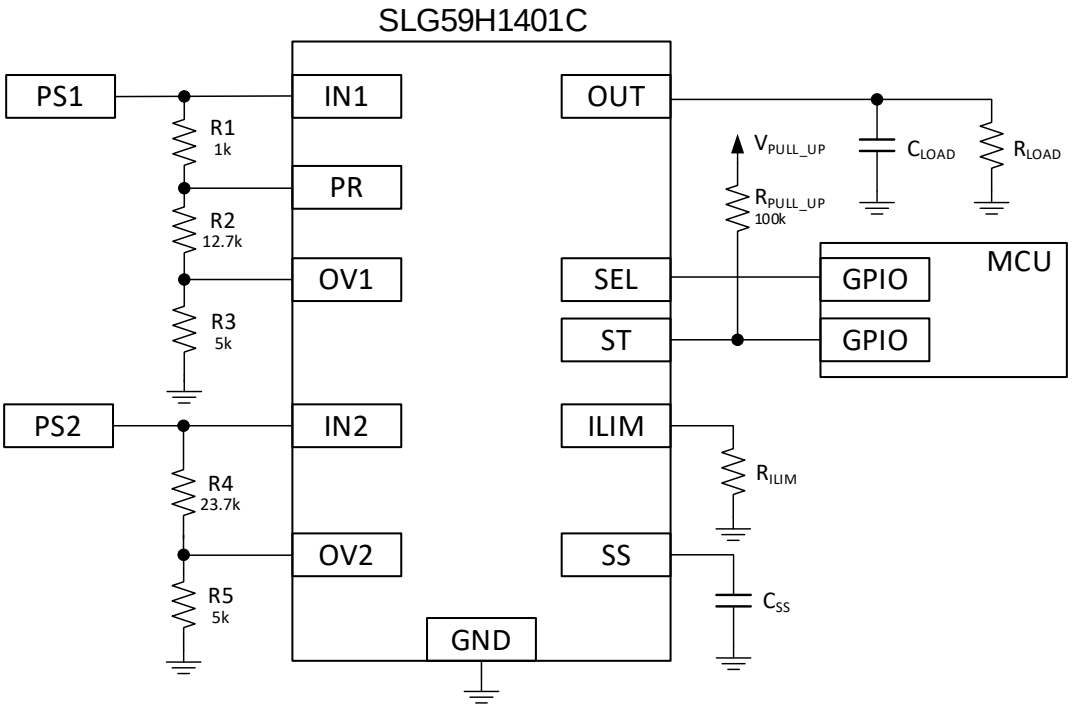

Figure 8: Connection diagram of using SLG59H1401C in PowerMUX applications for V_{IN1} = 3.3 V, V_{IN2} = 5 V and overvoltage protection settings at OV1 = 3.74 V, OV2 = 5.74 V

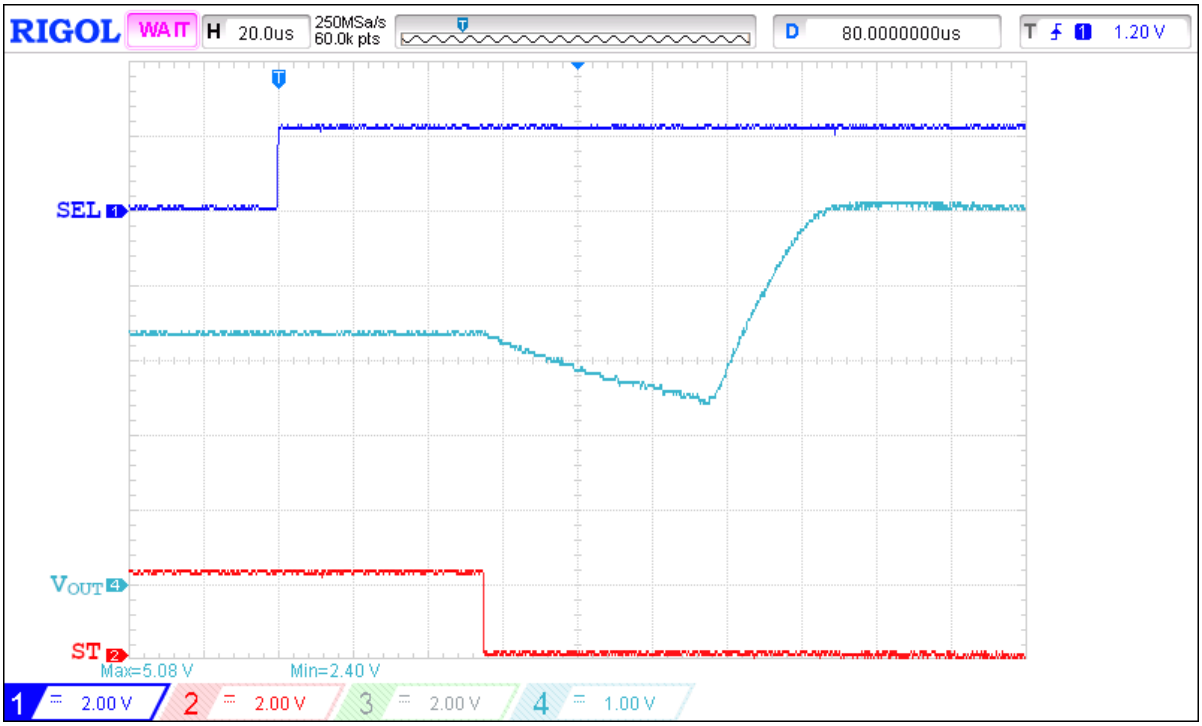

Figure 9: Switchover operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, C_{SS} = 220 nF, PR = High, SEL = Low → High, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

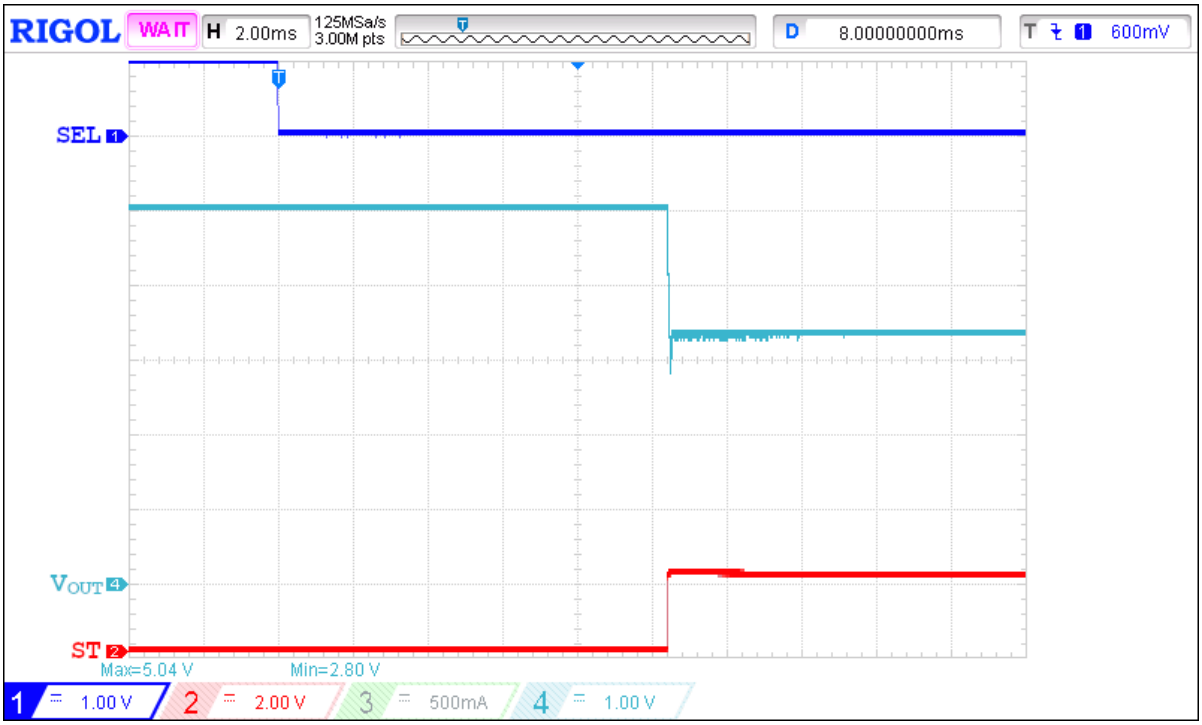

Figure 10: Switchover operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, C_{SS} = 220 nF, PR = High, SEL = High → Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

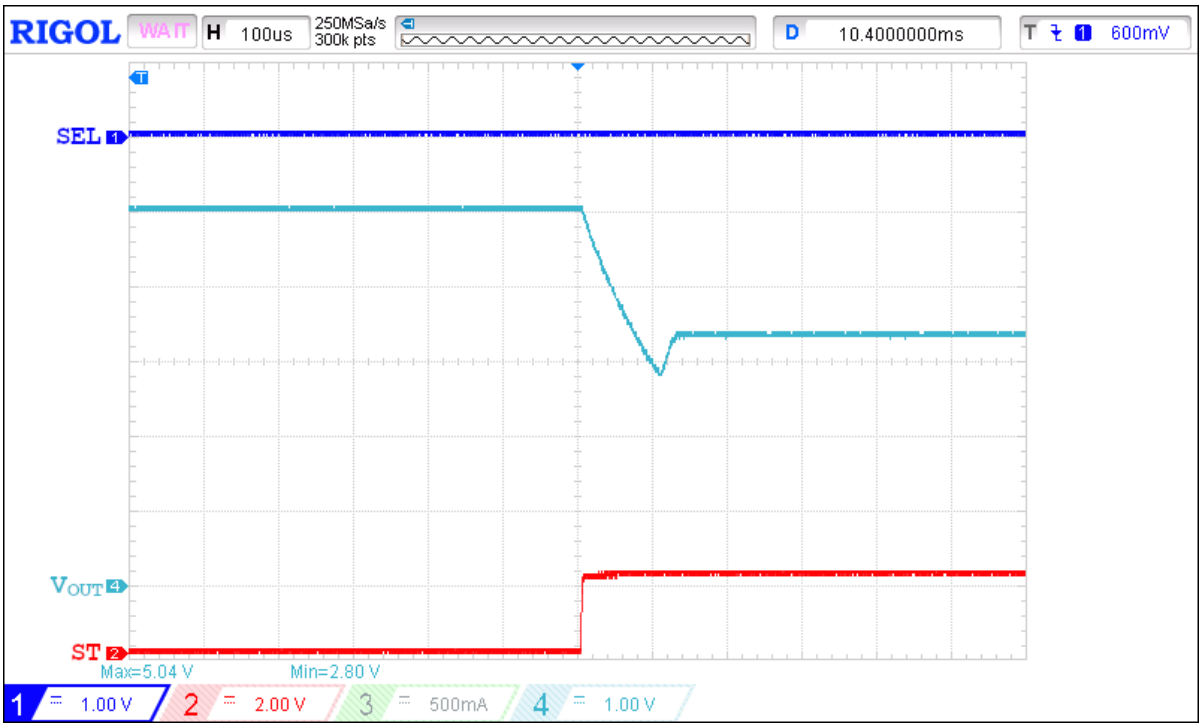

Figure 11: Switchover operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, C_{SS} = 220 nF, PR = High, SEL = High → Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

When a wider input voltage range is required for the PowerMUX application SLG59H1403C should be used. Similar application scope shots below demonstrate the switchover behavior of the SLG59H1403C device for V_{IN1} = 12 V, V_{IN2} = 20 V. Overvoltage thresholds for OV1 are set at 14.2 V, and for OV2 are set to 21 V. A typical connection diagram for these conditions is illustrated in Figure 12 and switchover waveforms are shown in

Figure 13, Figure 14 and Figure 15. Please note that in this connection diagram logic High is applying to the PR pin from the external pull-up resistor and not through IN1 like in SLG59H1401C Diagram. This is because the Absolute Maximum input voltage of the PR pin is 6 V.

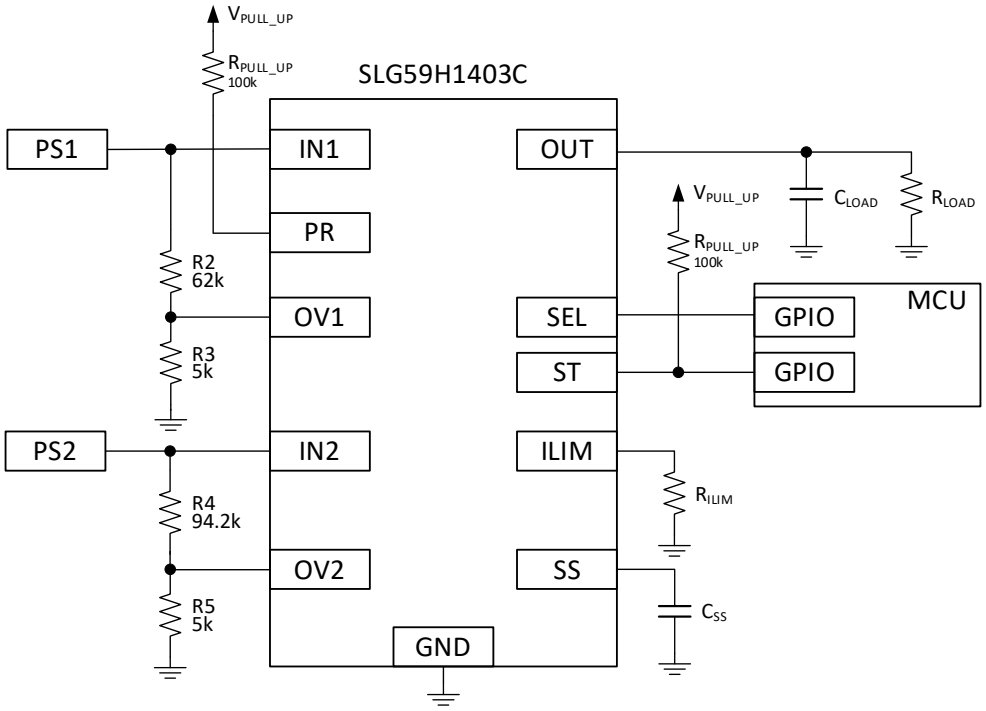

Figure 12: Connection diagram of using SLG59H1403C in PowerMUX applications for V_{IN1} = 12 V, V_{IN2} = 20 V and overvoltage protection settings at OV1 = 14.2 V, OV2 = 21 V

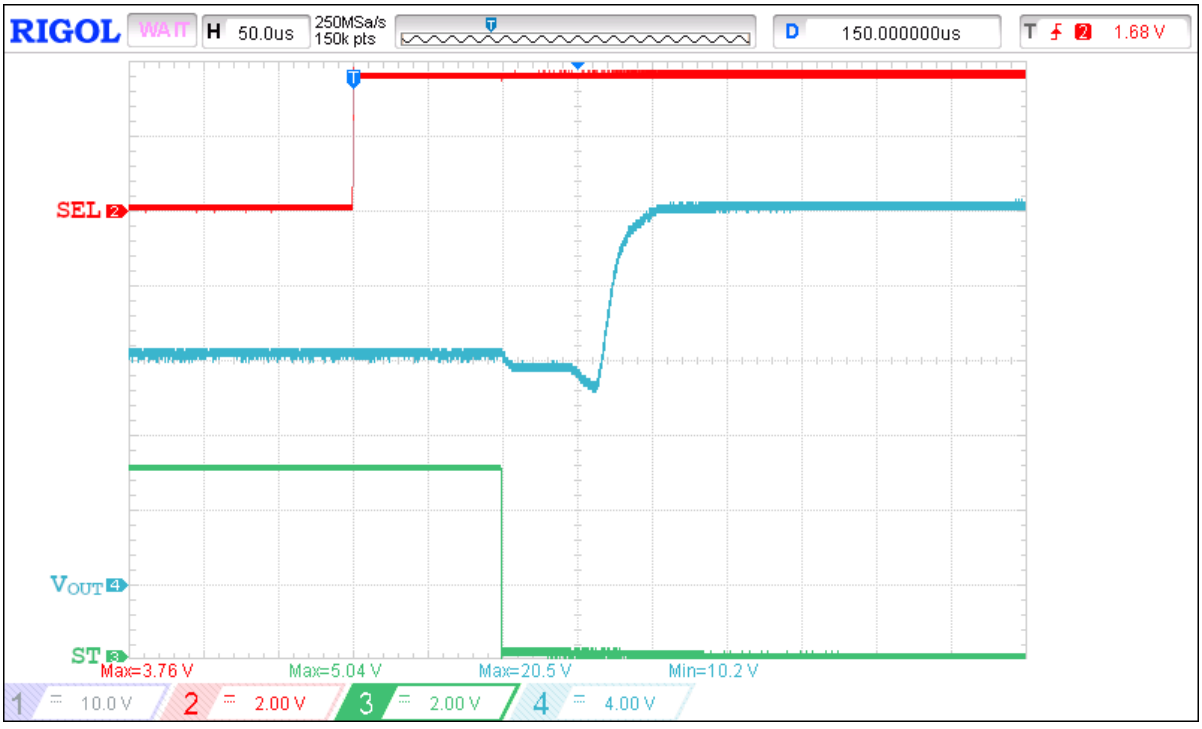

Figure 13: Switchover operation waveform for V_{IN1} = 12 V, V_{IN2} = 20 V, C_{SS} = 220 nF, PR = High, SEL = Low → High, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

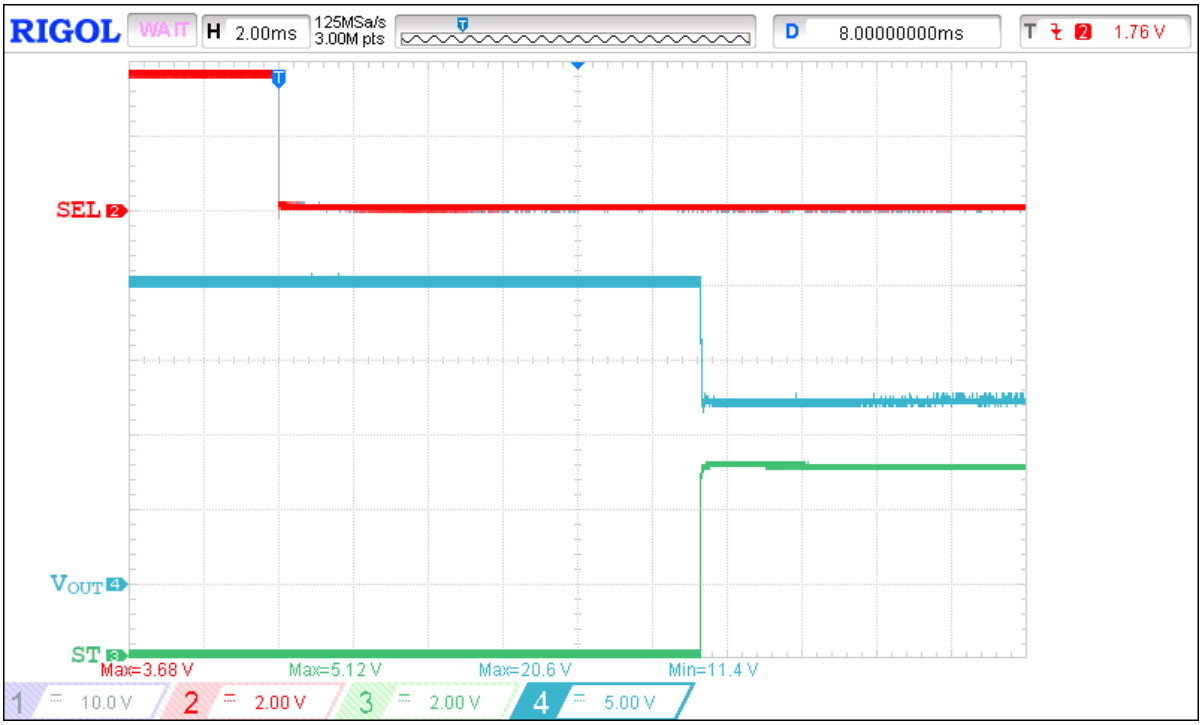

Figure 14: Switchover operation waveform for V_{IN1} = 12 V, V_{IN2} = 20 V, C_{SS} = 220 nF, PR = High, SEL = High → Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

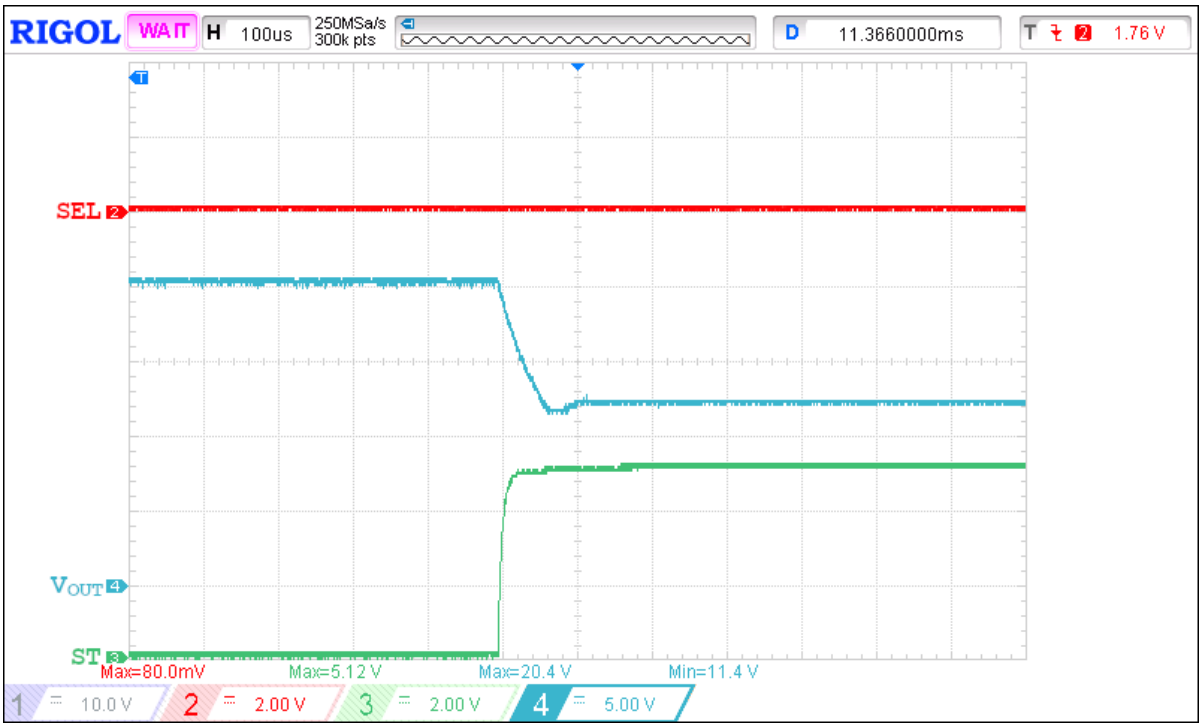

Figure 15: Switchover operation waveform for V_{IN1} = 12 V, V_{IN2} = 20 V, C_{SS} = 220 nF, PR = High, SEL = High → Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

4.3 Using SLG59H1401C and SLG59H1403C in PowerMUX applications with priority

In some applications, there is the main power rail and a backup power rail. Sometimes input voltage from the main power rail may not completely disappear but slightly be out of range and in this case system itself must switch to a backup power rail without interrupting the whole device operation and once the main power rail becomes valid again, the system should recover to that power rail automatically.

SLG59H1401C and SLG59H1403C device support such operation mode. The main and lower voltage level power rail should be connected to the IN1 input. Through an external voltage divider connected to the PR pin, a low voltage threshold for V_{IN1} can be set. If V_{SEL} = 0 V and $V_{PR} > V_{REF}$ then IN1 will be selected on output and if $V_{PR} < V_{REF}$ then the backup input IN2 will be on output. Anytime, if V_{SEL} manually set > V_{REF}**, then IN2 will be on output as well.**

Note: when $V_{PR} < V_{REF}$ and $V_{SEL} < V_{REF}$, SLG59H1401C and SLG59H1403C will operate in V_{COMP} mode, and the highest voltage level power rail will be on output. If both input voltages are equal, priority will be on the IN2 power rail. Also make sure that the voltage on the OV1, OV2, PR, and SEL pin is not higher than the absolute maximum rating.

A typical connection diagram for this operation mode is illustrated in Figure 16 and it's typical switchover behavior for V_{IN1} = 3.3 V and V_{IN2} = 5.5 V is illustrated in Figure 17 and Figure 18. Overvoltage thresholds for OV1 is set at 3.74 V, and for OV2 is set to 5.74 V.

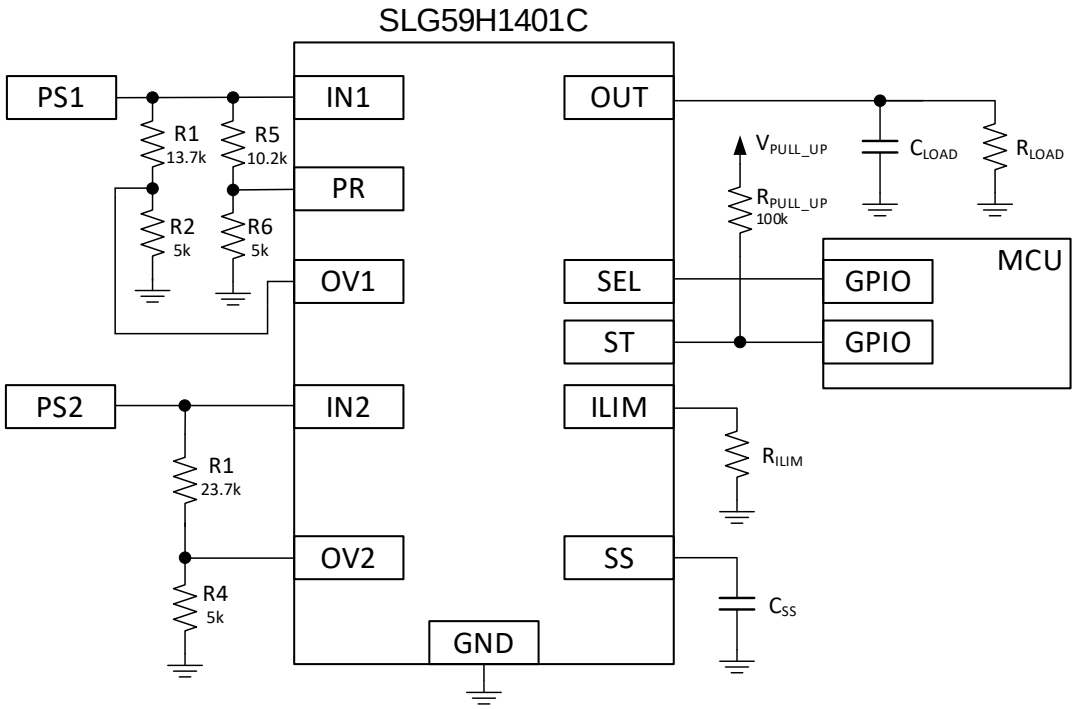

Figure 16: Connection diagram of using SLG59H1401C in PowerMUX applications with priority

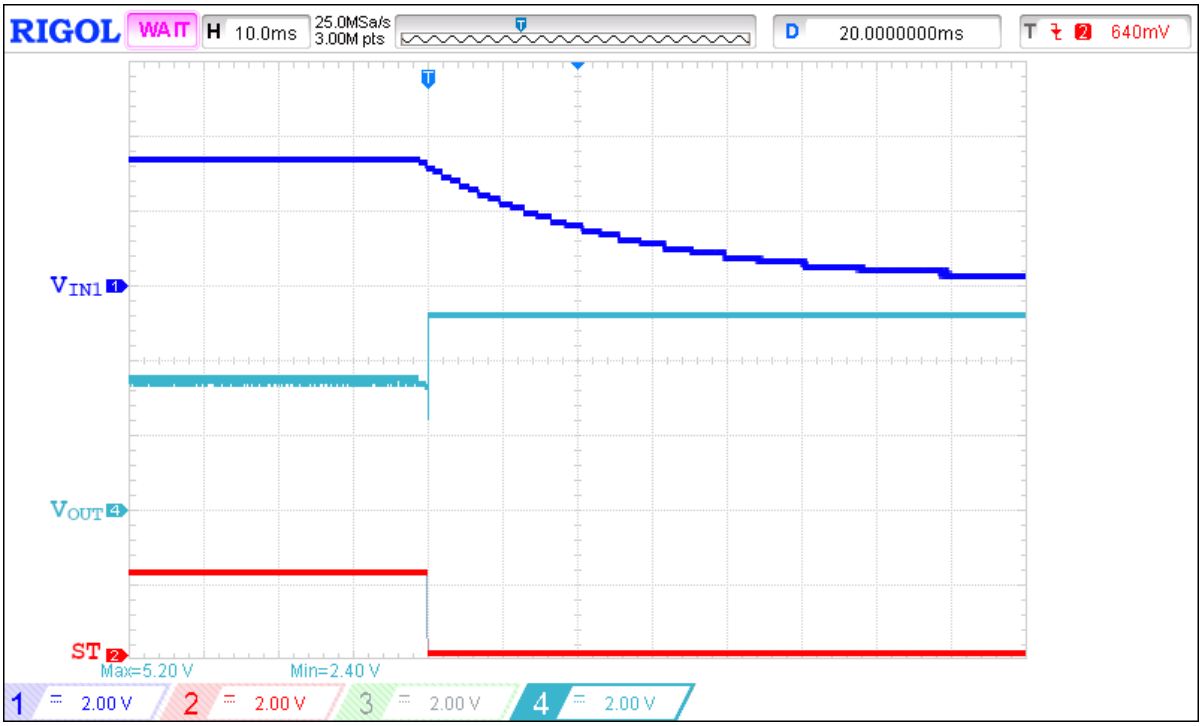

Figure 17: Switchover operation waveform when V_{IN1} is falling from 3.3 V to 0 V and V_{IN2} = 5 V, C_{SS} = 220 nF, SEL = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

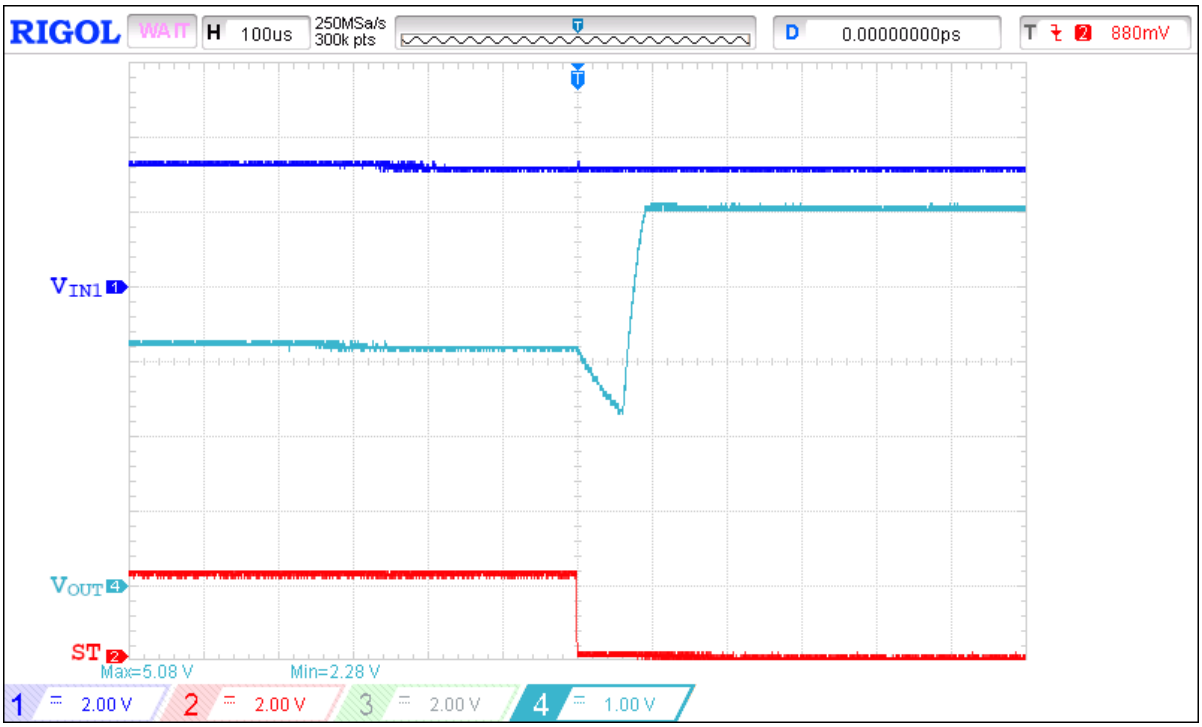

Figure 18: Switchover operation waveform when V_{IN1} is falling from 3.3 V to 0 V and V_{IN2} = 5 V, C_{SS} = 220 nF, SEL = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

When PowerMUX applications with priority required from 2.8 V to 22 V voltage range the Renesas SLG59H1403C should be used. A typical connection diagram for this operation mode is illustrated in Figure 19 and it's typical switchover behavior for V_{IN1} = 12 V and V_{IN2} = 20 V are illustrated in Figure 20 and Figure 21. The threshold level for PR is 10 V and Overvoltage thresholds for OV1 is set at 14.2 V, and for OV2 is set to 21 V.

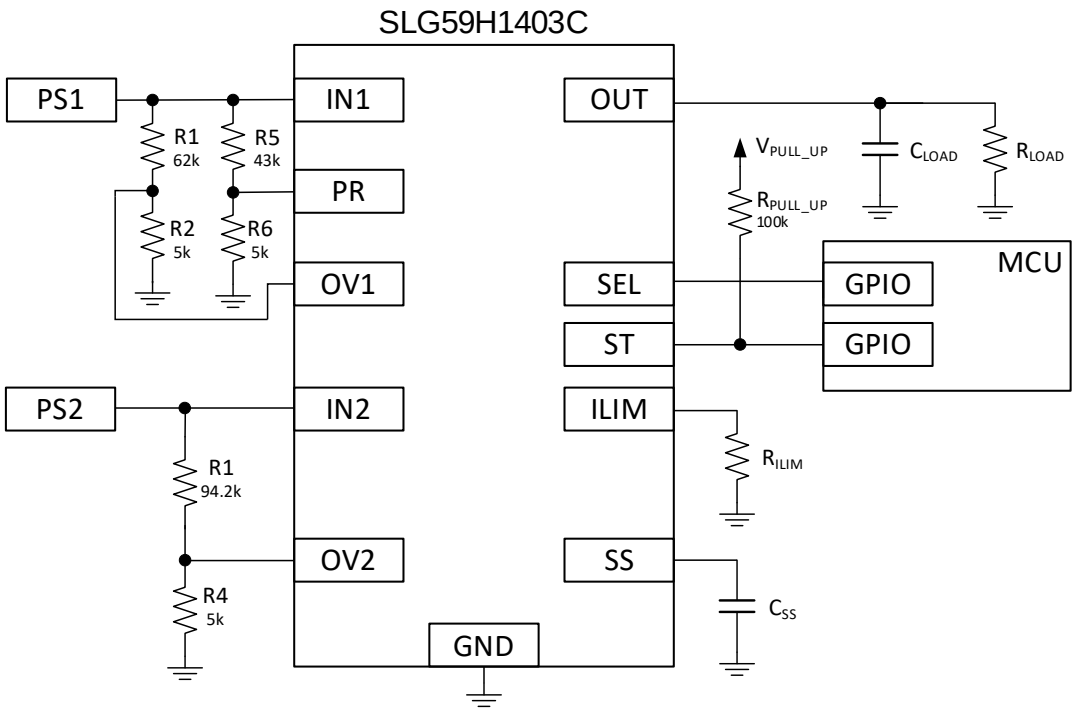

Figure 19: Connection diagram of using SLG59H1403C in PowerMUX applications with priority

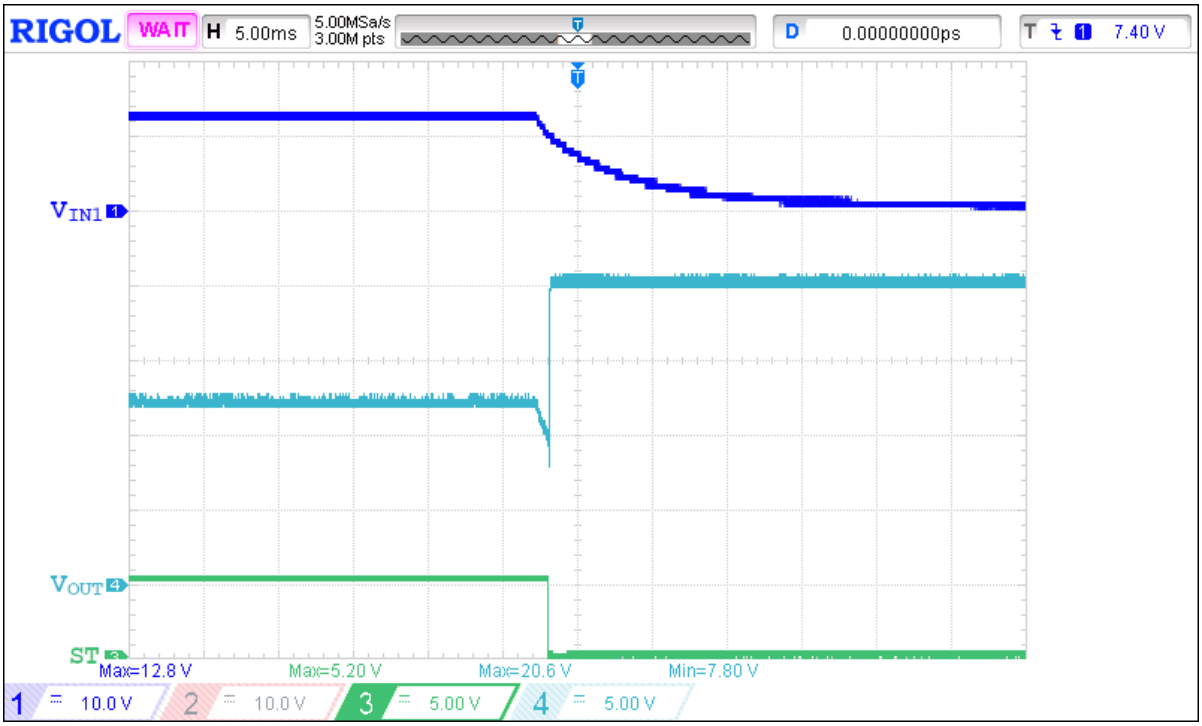

Figure 20: Switchover operation waveform when V_{IN1} is falling from 12 V to 0 V and V_{IN2} = 20 V, C_{SS} = 220 nF, SEL = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

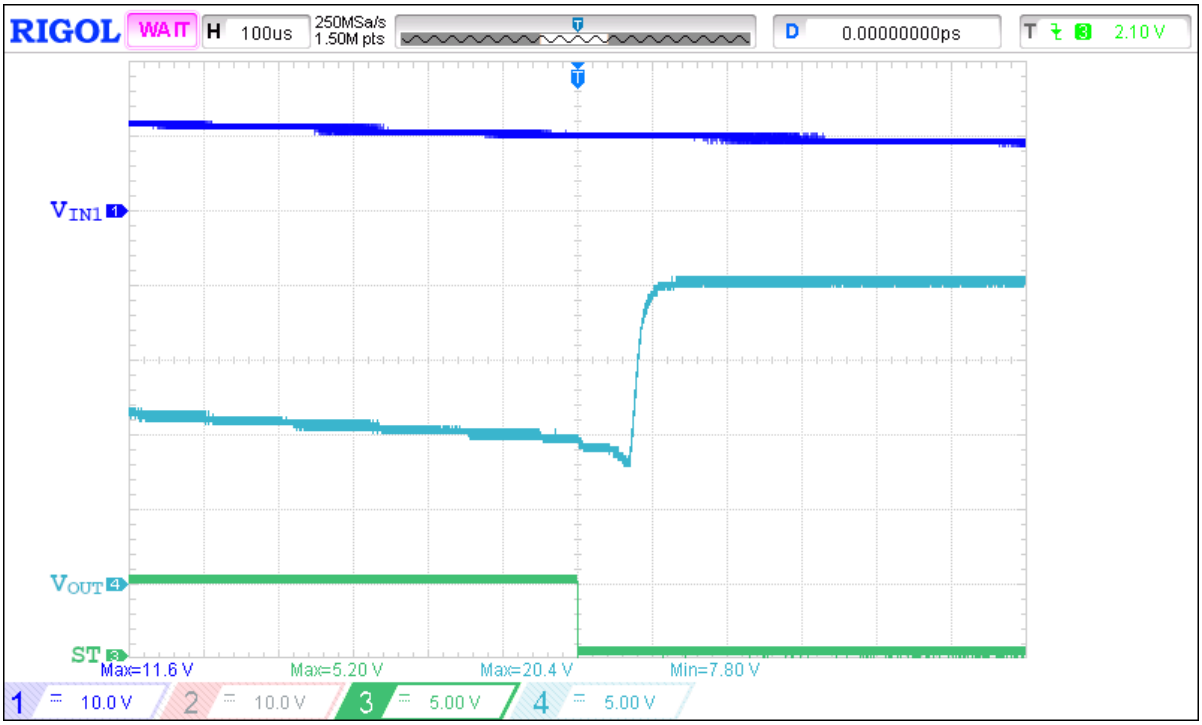

Figure 21: Switchover operation waveform when V_{IN1} is falling from 12 V to 0 V and V_{IN2} = 20 V, C_{SS} = 220 nF, SEL = Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

5. OR'ing Concept

In the event, that a power rail to the system from two power supplies should be chosen automatically when one of the power rail fails, an OR`ing application function is used. Unlike the Power Mux system, switching between power supplies occurs automatically without using a microcontroller or other digital control signals.

The minimum requirement for such a system is reverse current blocking for each input path to prevent current flow into the power supply with lower voltage. This can be accomplished using any combination of diodes or ICs which behave like a diode (such as an ideal diode controller). A simple realization of such an OR'ing solution is illustrated in Figure 22.

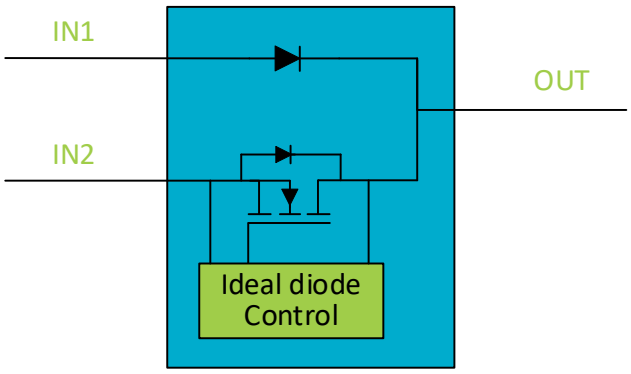

Figure 22: Simple OR`ing concept realization

A Schottky or silicon diode will result in a voltage drop of around 0.3 V or 0.6 V, respectively. Using an ideal diode controller will result in a much lower voltage drop and there will be a parasitic body diode that will block reverse current when the switch detects reverse current or is disabled.

5.1 Using SLG59H1401C and SLG59H1403C in OR'ing applications

In this case, SLG59H1401C or SLG59H1403C is configured for OR'ing two power rails and if both of them are valid, then the higher voltage is passed to the output. If one of the power rails suddenly disappears, then the

output is automatically switched to the other available power rail. If both power rails have equal voltage levels, then based on the V_{COMP} spec, IN2 has a higher priority and will be switched to OUT. If V_{IN2} falls below the V_{COMP} Hysteresis threshold, then IN1 will switch back to OUT. A typical V_{COMP} priority source selection diagram is illustrated in Figure 23 while actual V_{COMP} and Hysteresis values are provided in the EC table of SLG59H1401C and SLG59H1403C datasheets. The easiest way to set part in OR'ing mode is PR and SEL pins should be connected to GND.

Similarly, as for PowerMux mode, OV1 and OV2 with external resistors connected to IN1 and IN2 respectively can be configured to additionally provide overvoltage protection.

The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the ST pin is high, IN1 is on the output, or the output is Hi-Z. If the ST pin is low, IN2 is on the output.

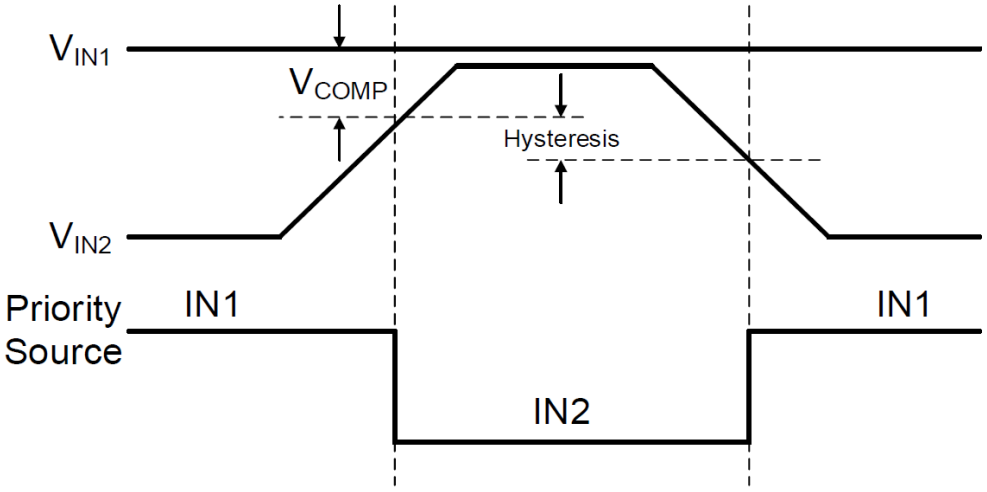

Figure 23: V_{COMP} Priority Source Selection diagram

A typical connection diagram for using SLG59H1401C in the OR'ing application is illustrated in

Figure 24 while its typical switchover behavior for V_{IN1} = 3.3 V and V_{IN2} = 5.5 V is illustrated in Figure 25. Overvoltage thresholds for OV1 are set at 3.74 V, and for OV2 are set to 5.74 V.

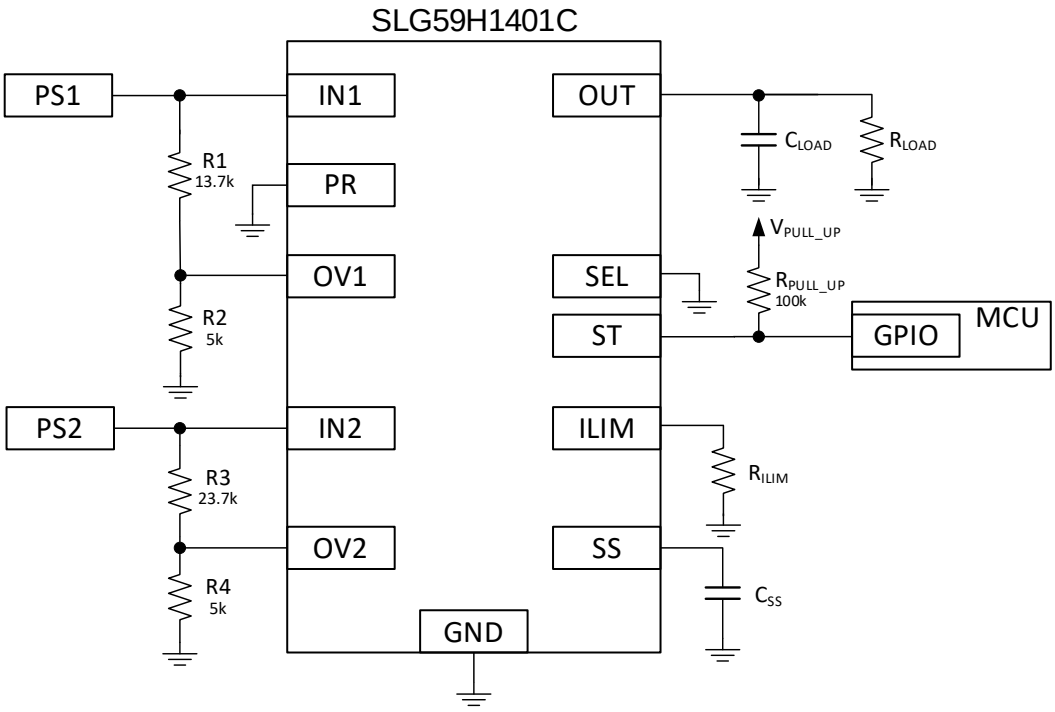

Figure 24: Connection diagram of using SLG59H1401C in OR'ing applications for V_{IN1} = 3.3 V, V_{IN2} = 5 V and overvoltage protection settings at OV1 = 3.74 V, OV2 = 5.74 V

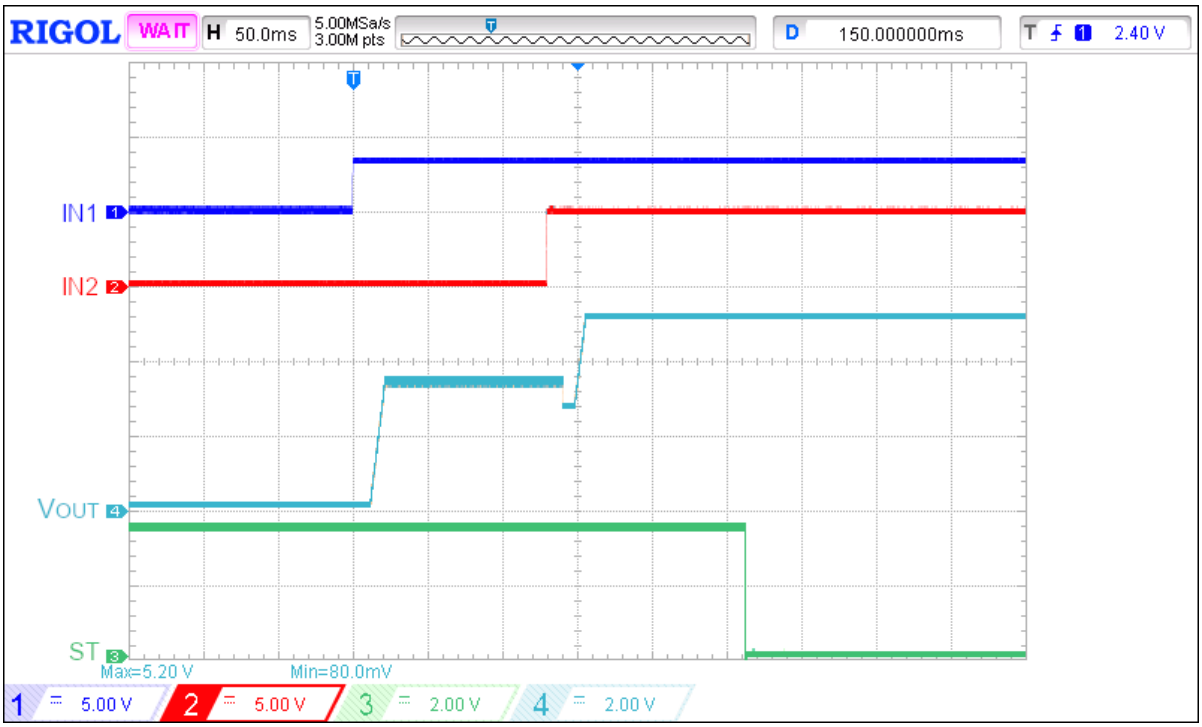

Figure 25: Higher voltage level priority turn on operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

Similar connection diagram for using SLG59H1401C in OR'ing application but for V_{IN1} = 5 V and V_{IN2} = 3.3 V is illustrated in Figure 26 and its typical switchover behavior is illustrated in figures from Figure 27 to Figure 32. Overvoltage thresholds for OV1 are set at 5.74 V, and for OV2 are set at 3.74 V.

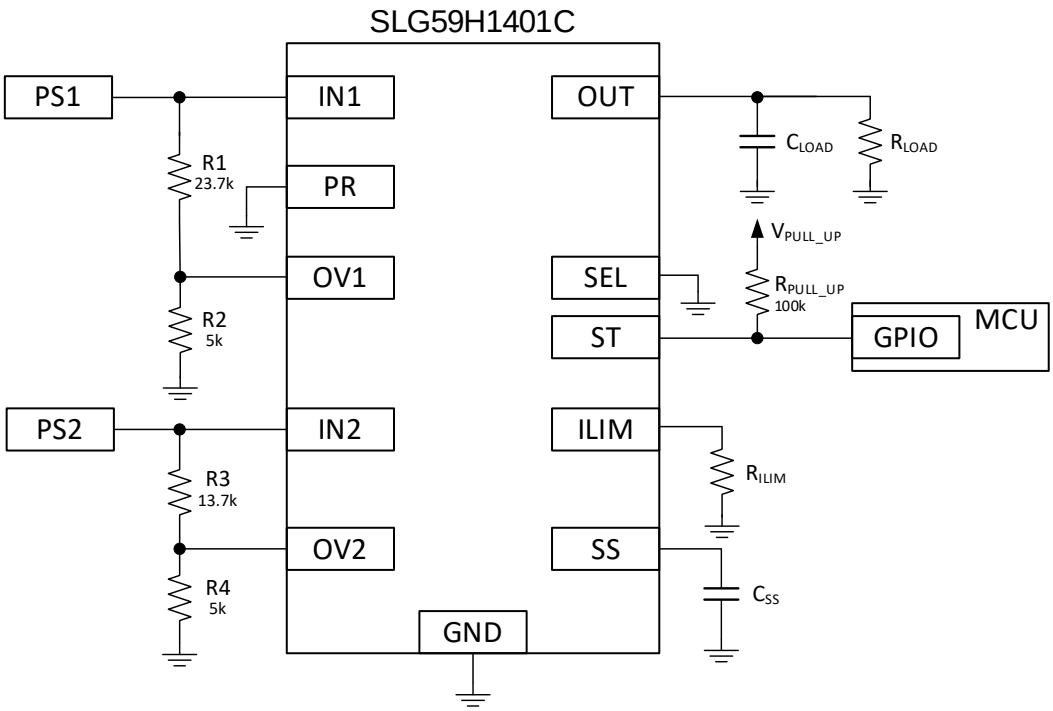

Figure 26: Connection diagram of using SLG59H1401C in OR'ing applications for V_{IN1} = 5 V, V_{IN2} = 3.3 V and overvoltage protection settings at OV1 = 5.74 V, OV2 = 3.74 V

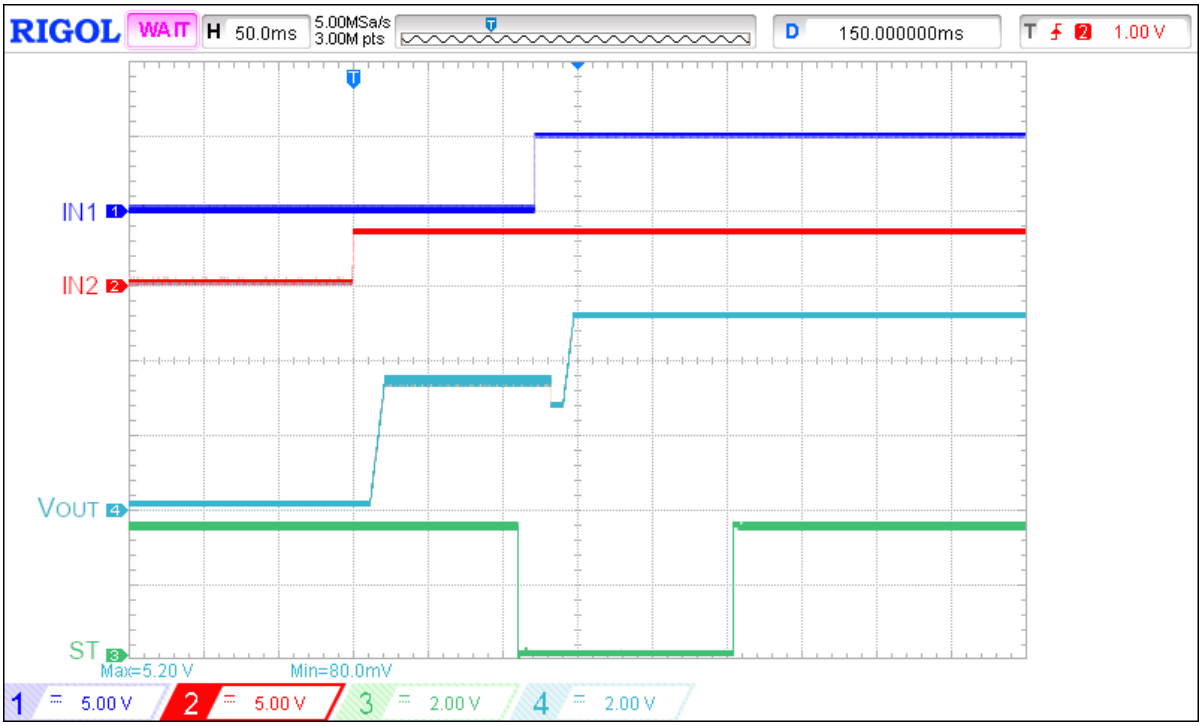

Figure 27: Higher voltage level priority operation waveform when V_{IN1} is applied after first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

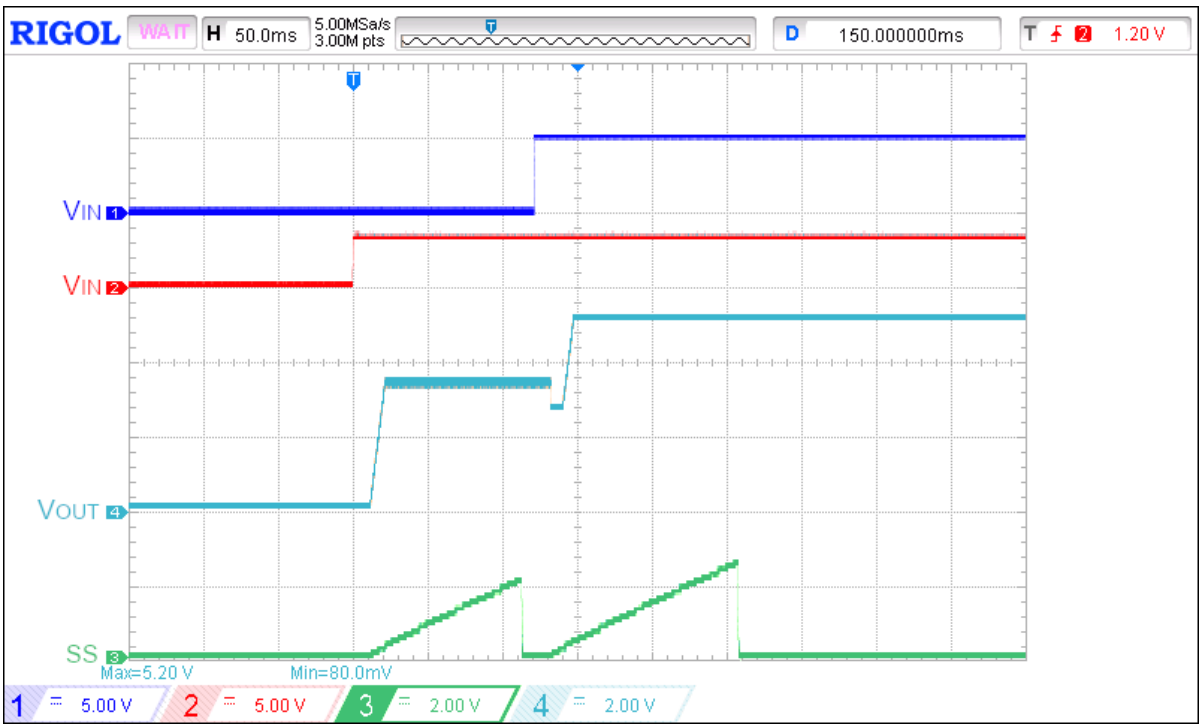

Figure 28: Higher voltage level priority operation waveform when V_{IN1} is applied after first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

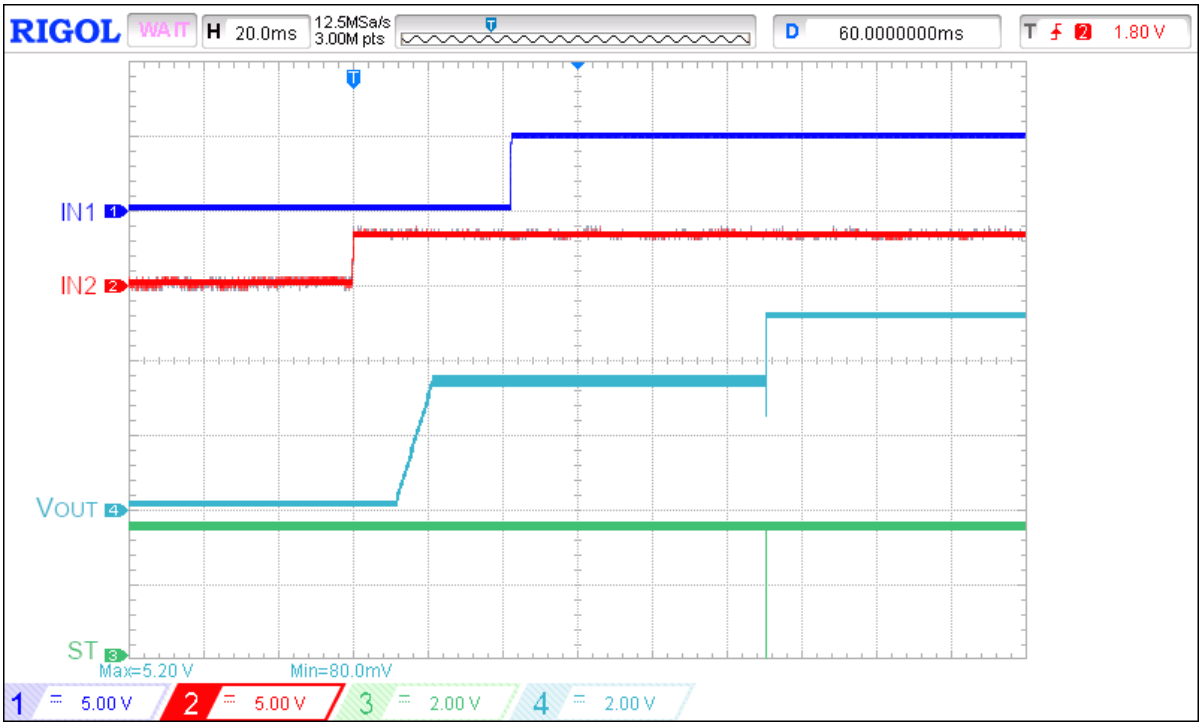

Figure 29: Higher voltage level priority operation waveform when V_{IN1} is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

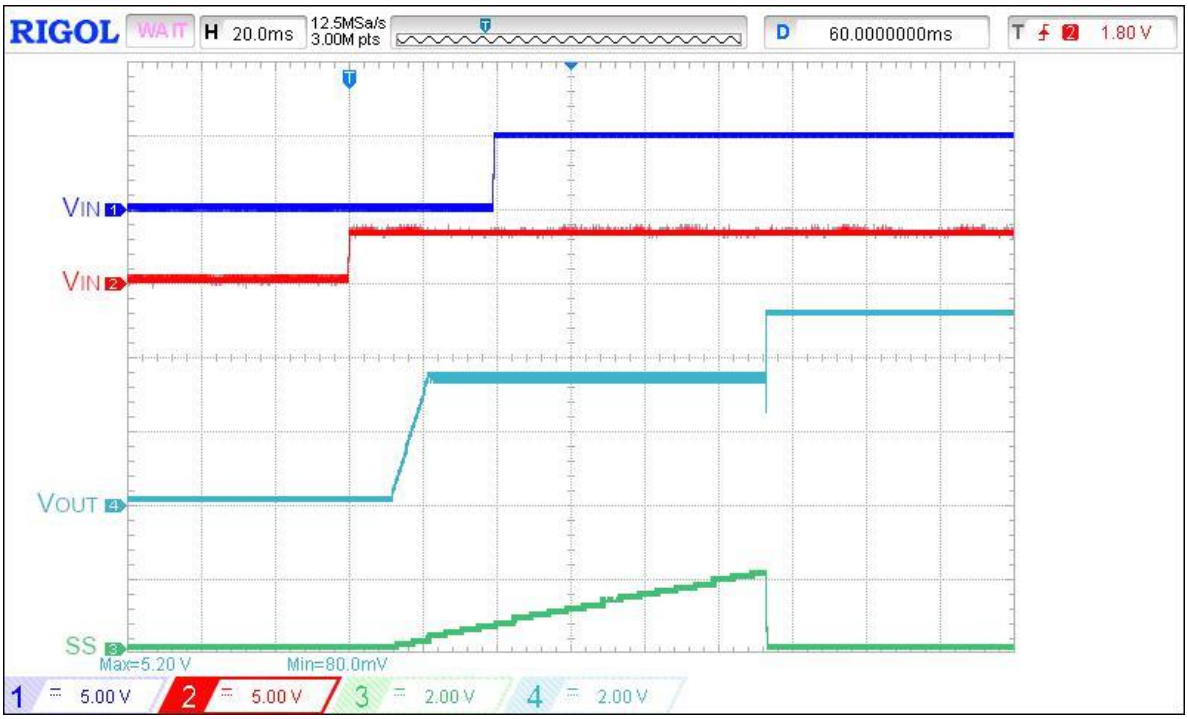

Figure 30: Higher voltage level priority operation waveform when V_{IN1} is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

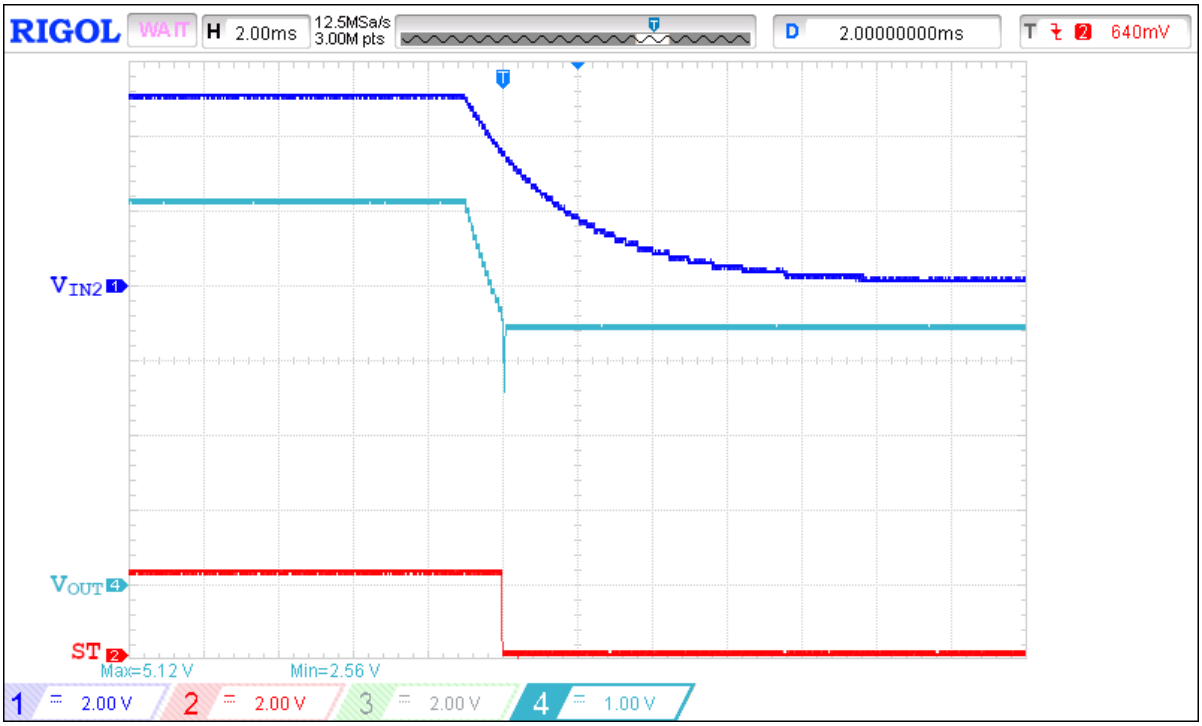

Figure 31: Higher voltage level priority operation waveform when V_{IN2} is falling from 3.3 V to 0 V and V_{IN1} = 5 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

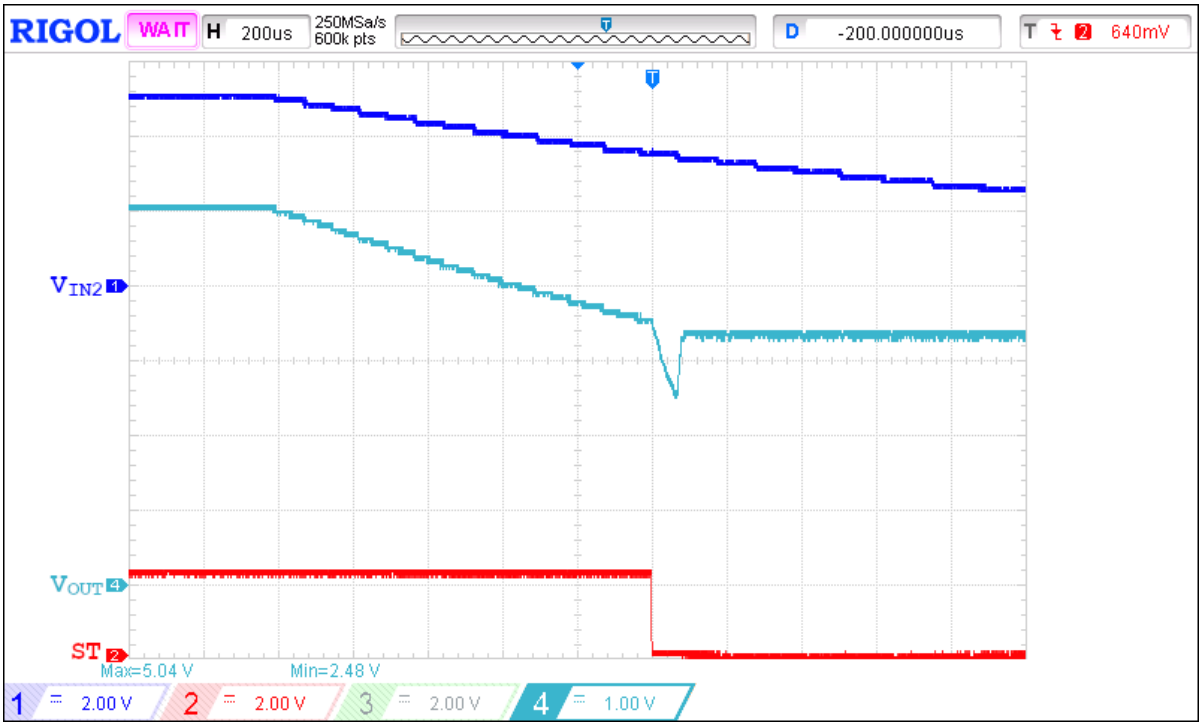

Figure 32: Higher voltage level priority operation waveform when V_{IN2} is falling from 3.3 V to 0 V and V_{IN1} = 5 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

For applications that require a voltage range from 2.8 V to 22 V Renesas' SLG59H1403C should be used. A typical connection diagram for this part is illustrated in Figure 33 w while its typical switchover behavior for V_{IN1} = 12 V and V_{IN2} = 20 V is illustrated in Figure 34, Figure 35 and Figure 36. Overvoltage thresholds for OV1 are set at 14.2 V, and for OV2 are set at 21 V.

Note: For SLG59H1403C it is not necessary to wait until the SS pin goes down before applying a second voltage to get a soft start during switchover.

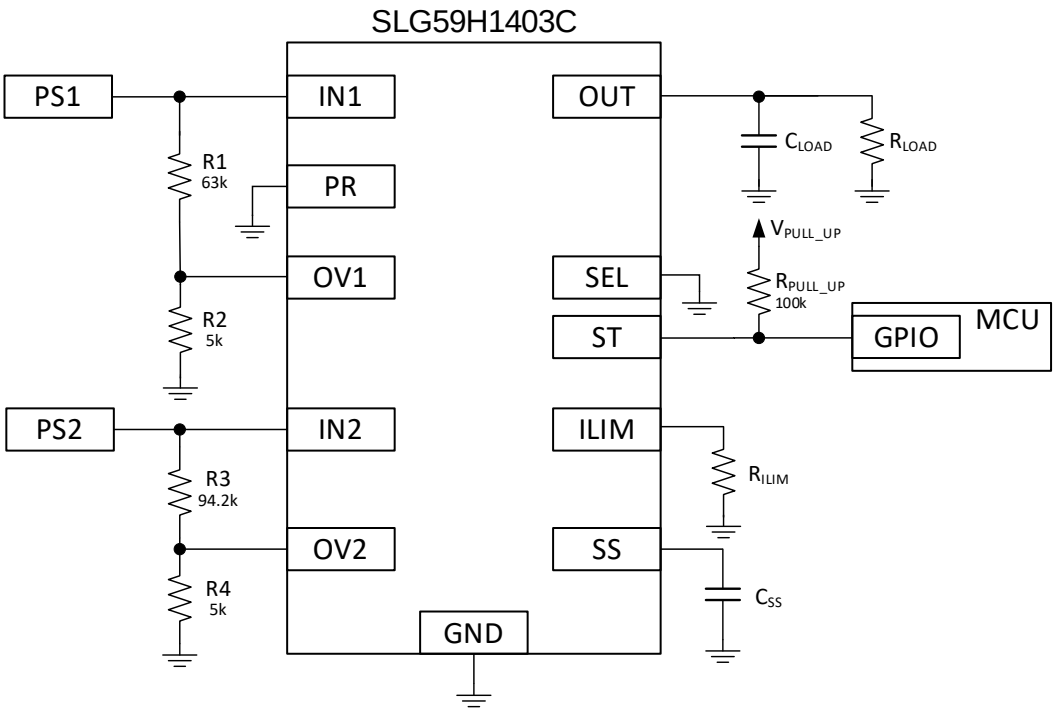

Figure 33: Connection diagram of using SLG59H1403C in OR'ing applications for V_{IN1} = 12 V, V_{IN2} = 20 V and overvoltage protection settings at OV1 = 14.2 V, OV2 = 21 V

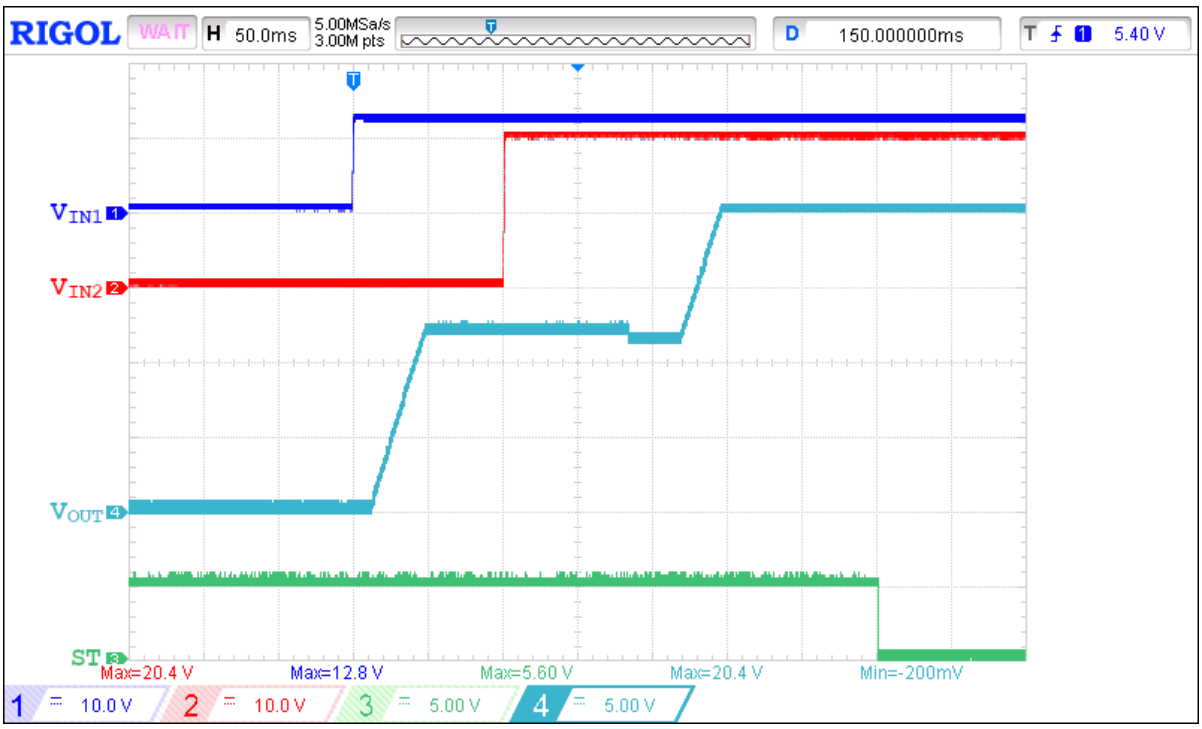

Figure 34: Higher voltage level priority turn on operation waveform for V_{IN1} = 12 V, V_{IN2} = 20 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

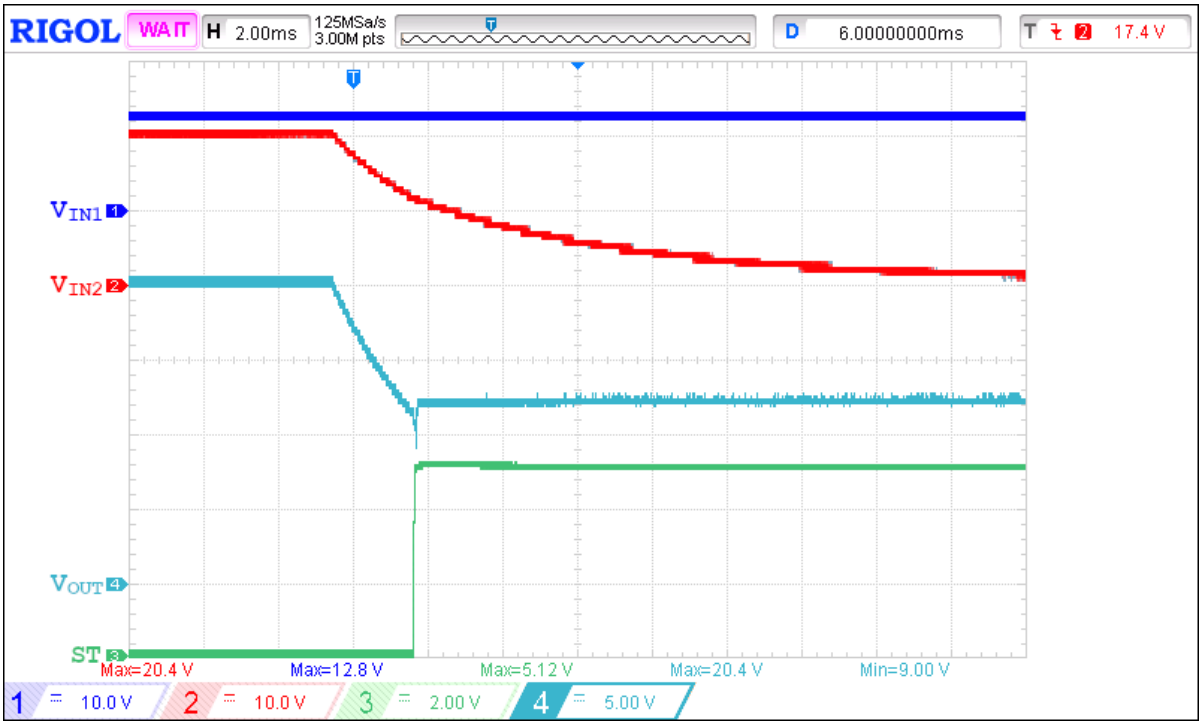

Figure 35: Higher voltage level priority operation waveform when V_{IN2} is falling from 20 V to 0 V and V_{IN1} = 12 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

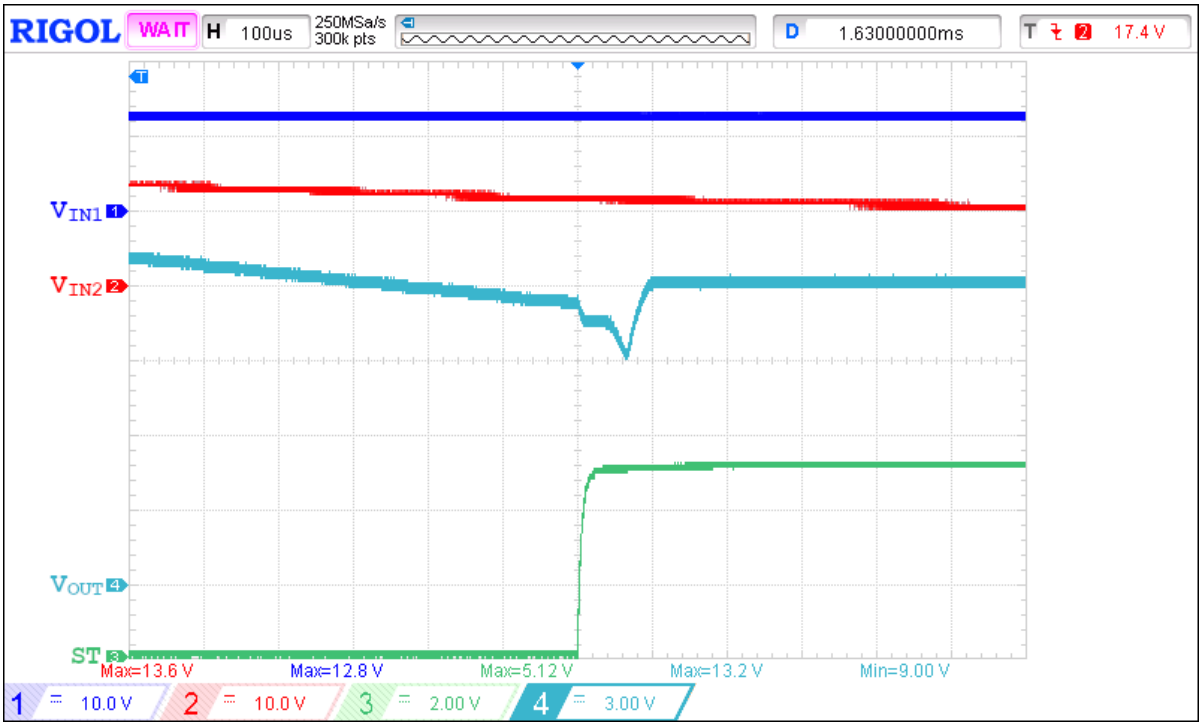

Figure 36: Higher voltage level priority operation waveform when V_{IN2} is falling from 20 V to 0 V and V_{IN1} = 12 V, SEL = Low, PR = Low, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

5.2 Using SLG59H1401C and SLG59H1403C in OR'ing applications with IN2 power rail priority

Many systems that have main and backup power rails require automatic switchover from the main voltage to the backup if the voltage at the main power rail drops below or above the specified value. In the connection diagram illustrated in Figure 37, the IN2 power rail is set as the main and IN1 as a backup.

R5 and R6 resistors, connected to the PR pin sets the minimum operating voltage for the IN1 power rail while R3 and R4 resistors, connected to the SEL pin sets the minimum operating voltage for the IN2 power rail. Thus, minimum operating voltages for V_{IN1} and V_{IN2} have been configured to 3 V and 5 V respectively.

Traditionally, OV1 and OV2 through resistive dividers are connected to IN1 and IN2 respectively to provide additional overvoltage protection.

Typical switchover behavior for V_{IN1} = 3.3 V and V_{IN2} = 5.5 V is illustrated in Figure 38. Overvoltage thresholds for OV1 are set at 3.74 V, and for OV2 are set to 5.74 V.

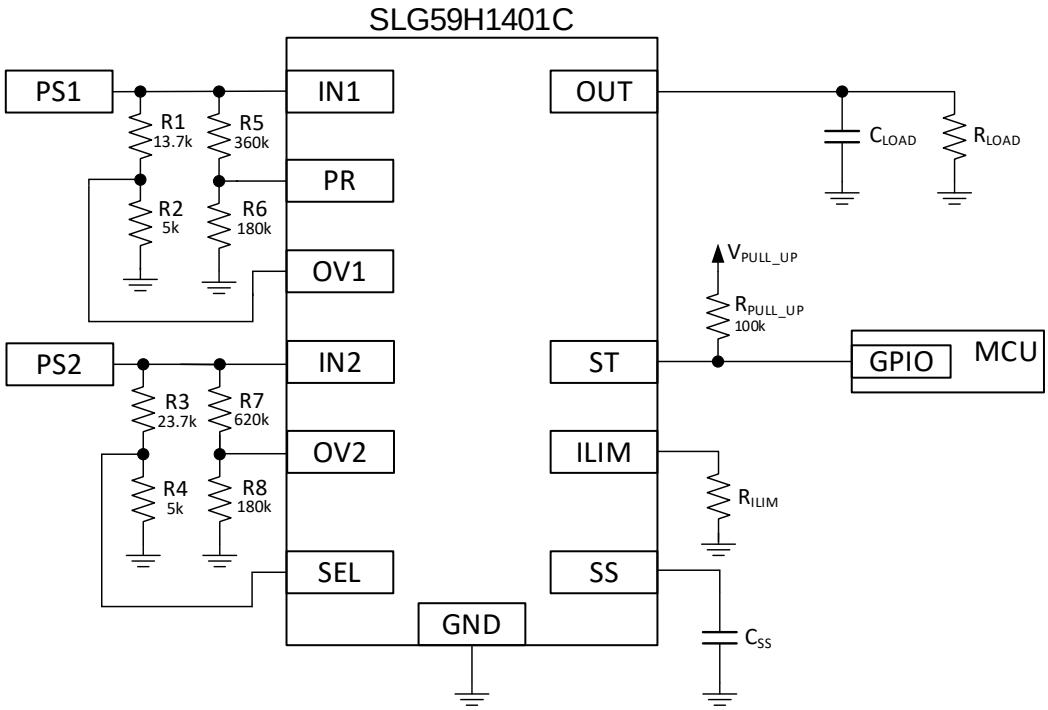

Figure 37: Connection diagram of using SLG59H1401C in OR'ing applications with IN2 power rail priority for V_{IN1} = 3.3 V, V_{IN2} = 5 V, and overvoltage protection settings at OV1 = 3.74 V, OV2 = 5.74 V

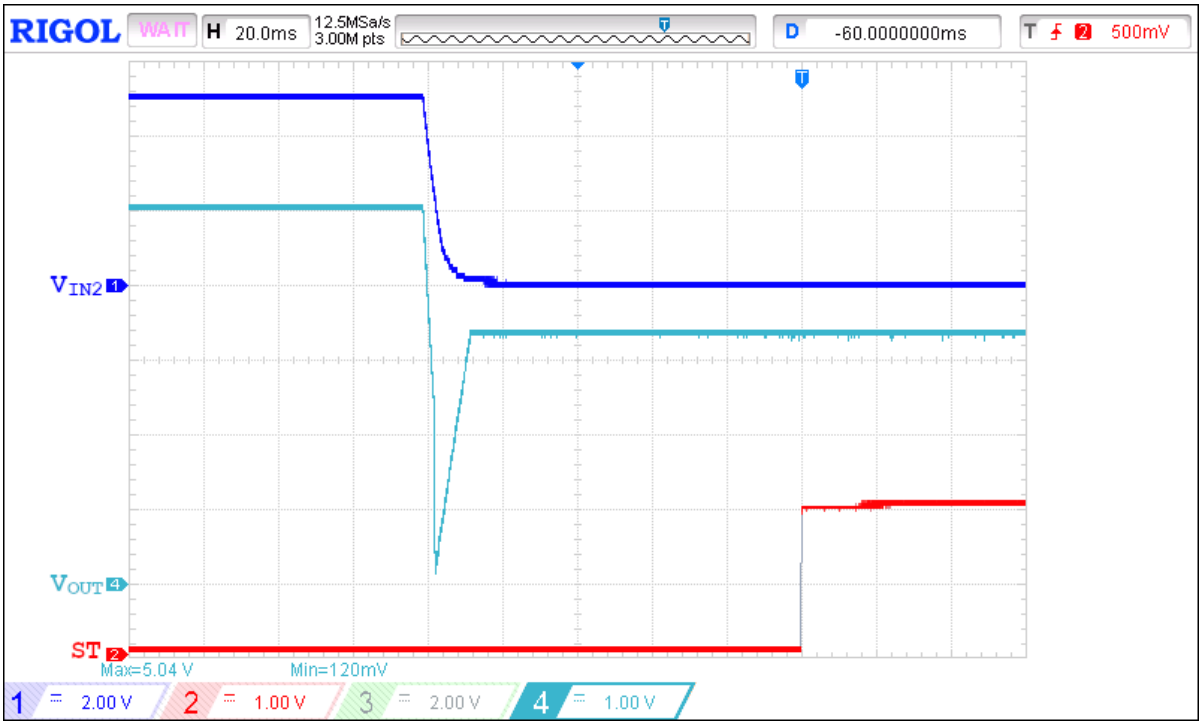

Figure 38: Higher voltage level priority operation waveform when V_{IN2} is falling from 5 V to 0V and V_{IN1} = 3.3 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

As can be seen, the output voltage is strongly dropped during the switchover caused by the internal switching delay of the chip. To compensate for this droop, a larger output capacitor should be considered. As an example, a similar switchover operation diagram with increased C_{LOAD} to 100 µF is illustrated in Figure 39.

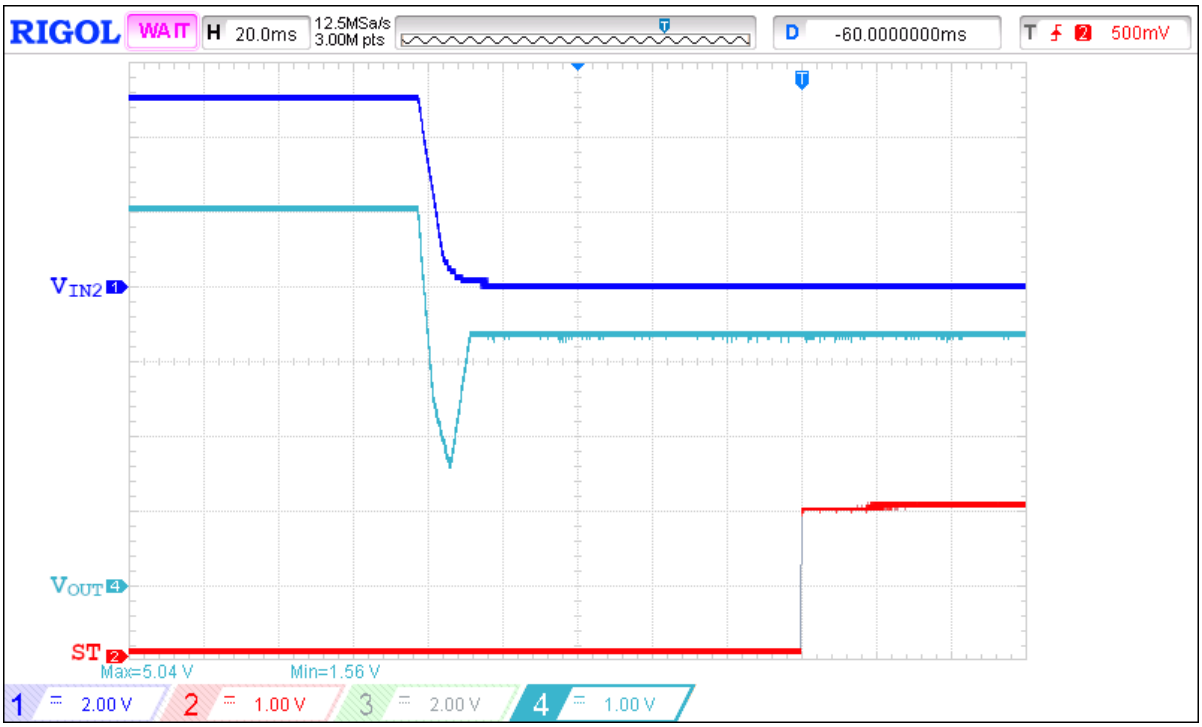

Figure 39: Higher voltage level priority operation waveform when V_{IN2} is falling from 5 V to 0V and V_{IN1} = 3.3 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 100 µF

When applications with a priority that requires a wider operating voltage range from 2.8 V to 22 V the Renesas' SLG59H1403C should be used. A typical connection diagram for this operation mode is illustrated in Figure 40 and its typical switchover behavior for V_{IN1} = 12 V and V_{IN2} = 20 V is illustrated in Figure 41 and Figure 42. The threshold level for PR is set at 10 V and for SEL is set to 18.1 V. As overvoltage protection, the threshold for OV1 is set at 14.2 V, and for OV2 is at 21 V.

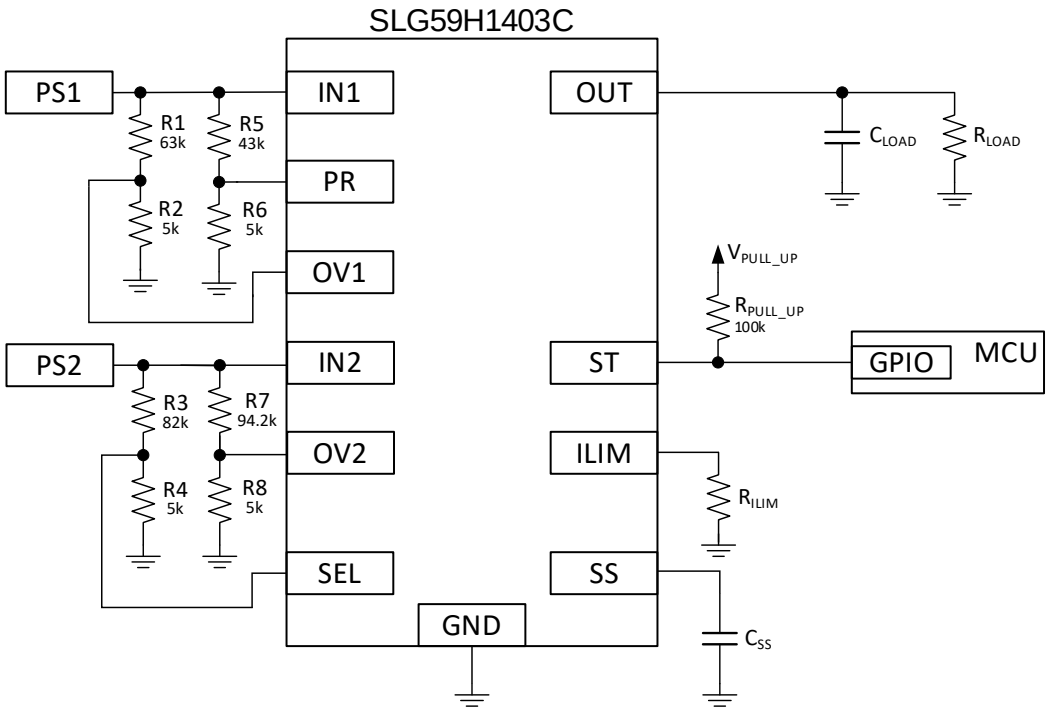

Figure 40: Connection diagram of using SLG59H1403C in OR'ing applications with IN2 power rail priority for V_{IN1} = 12 V, V_{IN2} = 20 V, and overvoltage protection settings at OV1 = 14.2 V, OV2 = 21 V

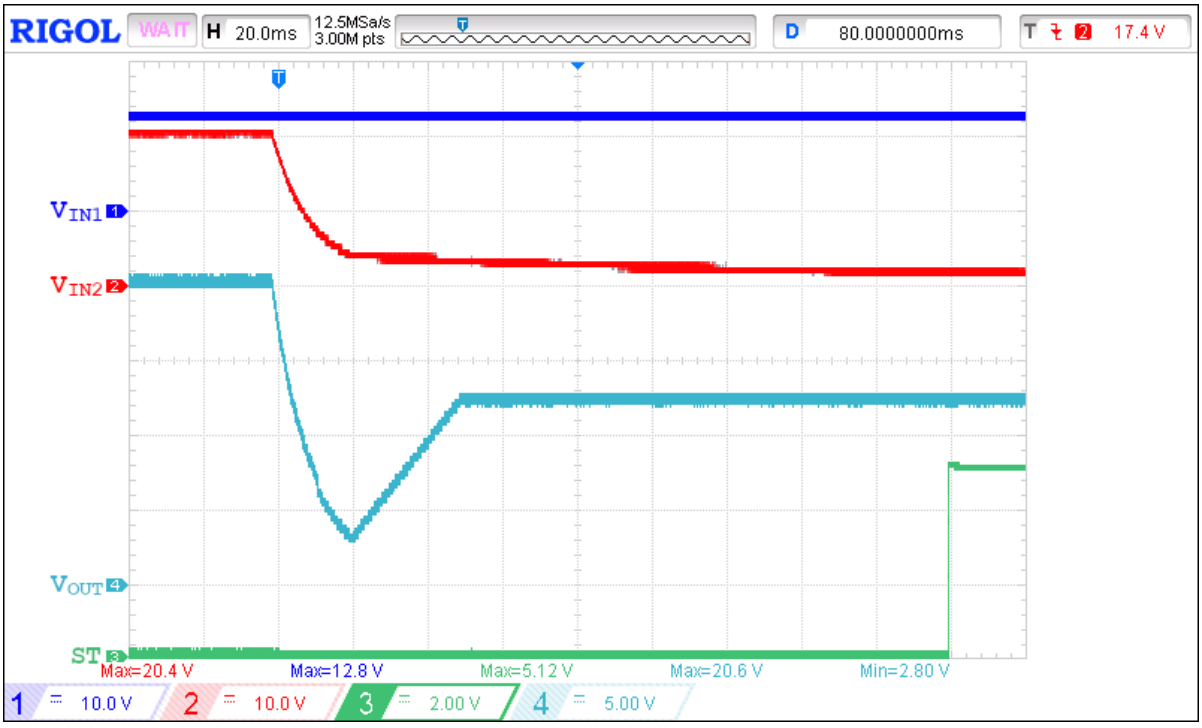

Figure 41: Higher voltage level priority operation waveform when V_{IN2} is falling from 20 V to 0V and V_{IN1} = 12 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

Like SLG59H1401C, the SLG59H1403C also has a big output voltage drop during switchover caused by the internal switching delay of the chip. To compensate for this droop, a larger output capacitor can be considered. As an example, a similar switchover operation diagram with increased C_{LOAD} to 300 µF is illustrated in Figure 42.

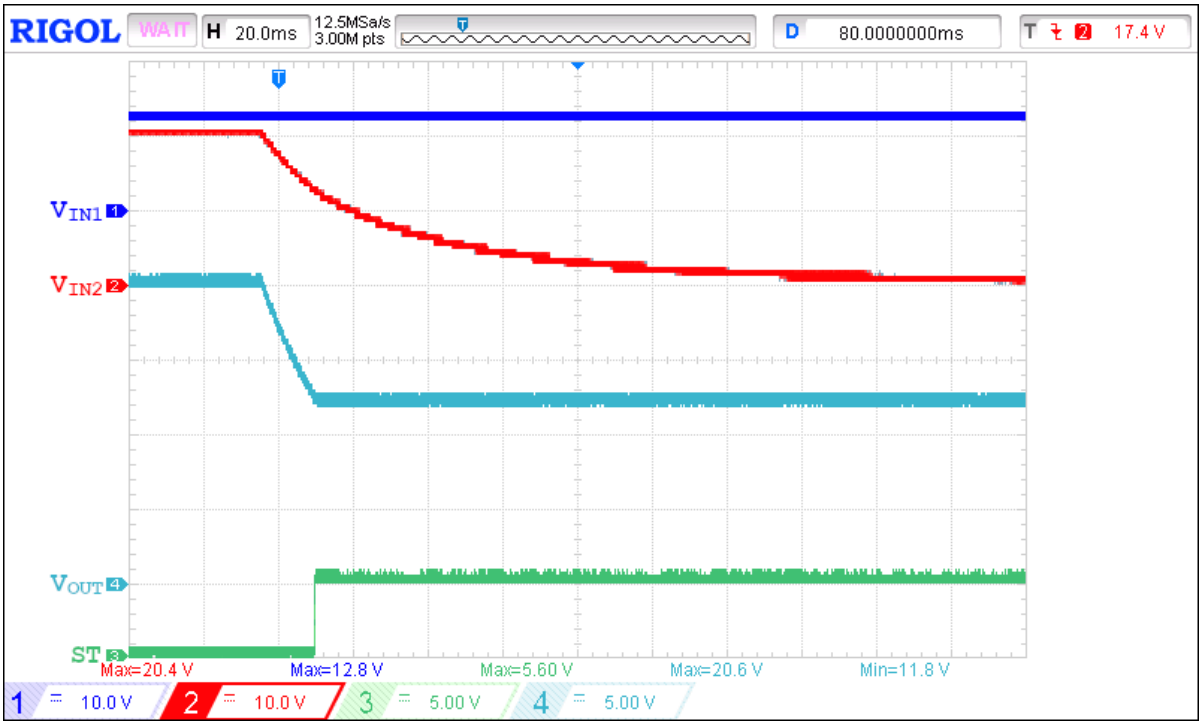

Figure 42: Higher voltage level priority operation waveform when V_{IN2} is falling from 20 V to 0V and V_{IN1} = 12 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 300 µF

6. Conclusions

PowerMux is an indispensable device developed for applications that use several input power supplies to a common output load. Using the Renesas' SLG59H1401C and SLG59H1403C devices specially designed for PowerMux and OR`ing applications, the process of controlling the switching between different sources will be easier and safer. Renesas' SLG59H1401C and SLG59H1403C ICs have protection against over and under voltages as well as overcurrent and overtemperature what significantly increases the system reliability.

Revision History

Revision	Date	Description
1.00	Sep 20, 2022	Initial release.