LX7169

3A Step-Down Converter

PRODUCTION DATASHEET

DESCRIPTION

LX7169 is a step-down PWM Switching regulator IC with integrated high side P-Channel and low side N-Channel MOSFETs. The IC operates using a hysteretic control topology with a full load operating frequency of 3MHz. This switching frequency allows for small output filter components while maintaining excellent dynamic load response.

The operational input voltage range of LX7169 is from 3V to 5.5V. The SYNC pin is tied low when not in use. A clock signal to this pin will synchronize the converter to an external source.

In the shutdown mode, the IC's current consumption is reduced to less than 1mA and the output capacitor is discharged.

Other features of the part are:

a) Cycle-by-cycle current limit followed by HICCUP mode which reduces the overall power dissipation of the internal MOSFETs

b) Thermal protection and internal digital soft start.

The LX7169 also provides a Power Good function. The LX7169 is available in a 12L 3mm x 3.5mm DFN package.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

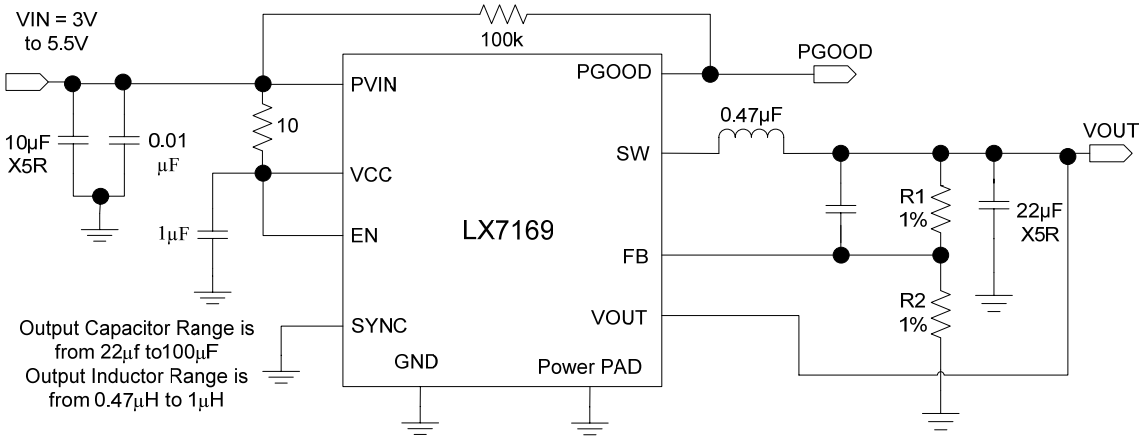
KEY FEATURES

- 3A Step-down Regulator
- Operational Input Supply Voltage Range: 3V-5.5V
- Integrated PMOS and NMOS
- Load Current from zero to 3A
- 3MHz Switching Frequency
- SKIP Pulse to Improve Light Load Efficiency
- Input UVLO Protection
- Enable Pin
- Power Good
- Internal Soft-start
- Cycle-by-Cycle Over Current Protection
- Hiccup Mode Operation Under OCP
- RoHS Compliant for Pb Free

APPLICATIONS

- HDD
- Set-Top Box
- LCD TV's
- Notebook/Netbook
- Routers
- Video Cards
- PC Peripherals
- PoE Powered Devices

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)		
	LD	**12L DFN (3.0 x 3.5 mm)**
	RoHS Compliant / Pb-free	
-10 to +85	**LX7169CLD**	

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX7169CLD-TR)

THERMAL DATA

θ_{JA} = 36°C/W

THERMAL RESISTANCE-JUNCTION TO AMBIENT

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. θ_{JA} number above is with 4-layer PCB board.

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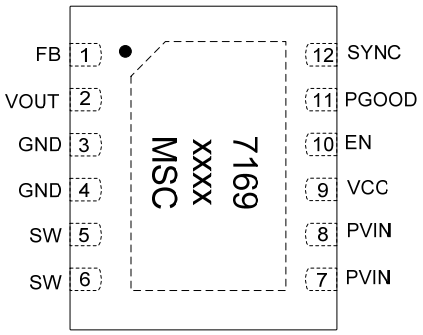
ABSOLUTE MAXIMUM RATINGS

PVIN, VCC, EN, FB, PGOOD, VOUT, MODE, SYNC ..... -0.3V to 7V
SW ..... -0.3V to 7V
SW (Shorter than 50ns) ..... -2V to 7V
Maximum Operating Junction Temperature .....-10°C to 150°C
Storage Temperature Range.....-65°C to 150°C
Peak Package Solder Reflow Temp. (40 seconds maximum exposure)..... 260°C (+0,-5)

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" are not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

PACKAGE PIN OUT



LD PACKAGE

(Top View)
Exposed Pad = GND
xxxx = Date/Lot Code
RoHS / Pb-free 100% Matte Tin Lead Finish

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of -10°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: VCC = PVIN = 5V. Typical parameter refers to T_J=25°C

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Recommended Operating Range						
VCC, PVIN			3		5.5	V
Operating Current						
Input Current	I_Q	I_{LOAD} = 0		12		mA
Input Current at Shut Down	I_{IN}	EN = GND		0.001	1	mA
VCC Input UVLO						
Under Voltage Lockout	VCC	VCC rising		2.4	2.8	V
UVLO Hysteresis				230		mV
Feedback						
Feedback Voltage Internal Reference	V_{REF}	T_A = 25°C	0.792	0.800	0.808	V
		Temperature range	0.788		0.812	V
FB Pin Input Current	I_{FB}				10	nA
Line Regulation		V_{IN} from 3V to 5.5V		0.30		%
Load Regulation		I_{LOAD} = 0.5 to 3A		-0.10		%/A
Vout Voltage Positioning	V_{REG}	Vout = 1.2V, Hysteretic Mode		1%		
Transient Response		Load from 0.1 to 1.5 amps, T_R =T_F = 100ns, V_{OUT} = 1.2V C_{OUT} = 44µF		+/-40		mV
FB UVLO						
FB UVLO Threshold	V_{FBULVO}			70%		V_{REF}

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Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
OUTPUT DEVICE						
R_{DSON} of High Side	R_{DSON_H}			60	90	mΩ
R_{DSON} of Low Side	R_{DSON_L}			40	60	mΩ
Current Limit	I_L		3.75	4.5	5.5	A
Thermal Shut Down Threshold	T_{SH}			150		°C
Hysteresis	T_H			20		°C
PVIN OVP						
Rising Threshold	OVP_R			6.5		V
Falling Threshold	OVP_F		5.5	6.3		V
OSCILLATOR FREQUENCY						
Switching Frequency	F	In Constant Frequency Hysteretic Mode	2.6	3	3.4	MHz
SOFT START						
Soft Start Time	T_{SS}	From EN high to PGOOD high.		500		µs
Hiccup Time	T_{HICCUP}	FB = 0.2V		1.5		ms
SYNC						
Input High	M_{VIH}		1			V
Input Low	M_{VIL}				0.4	V
EN INPUT						
Input High	EN_{VIH}		1			V
Input Low	EN_{VIL}				0.4	V
Hysteresis	EN_H			0.1		V
Input Bias	EN_{II}			0.01	1	µA
POWER-GOOD						
Power-good Transition High Threshold	V_{PG}	V_{FB} rising, In percentage of output voltage set-point. During startup, the PGOOD will not go high until the soft start cycle has finished.		83		%
Hysteresis	V_{PGHY}	Either V_{FB} rising or falling		40		mV
Power-good Internal FET R_{DSON}	PG_{RDSON}	VCC=5V		100	300	ohm
PGOOD FET Leakage Current				0.01	1	µA
Pgood Internal Glitch Filter				5		µSec
Output Discharge						
Internal Discharge Resistor			80	200	1400	ohm

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FUNCTIONAL PIN DESCRIPTION		
Name	**Pin #**	**Description**
FB	1	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired value.
VOUT	2	Attached to V_{OUT}.
GND	3,4	Ground pin for the power stage.
SW	5,6	Switch-node pin. Connect the output inductor between this pin and output capacitor. When the chip is DISABLED, the internal discharge resistor will be enabled to discharge the output capacitance. The current will flow into this pin.
PVIN	7,8	Input voltage terminal of the regulator. A minimum of 10µF, X5R type ceramic capacitor must be connected as close as possible from this pin to PGND plane to insure proper operation.
VCC	9	Analog input voltage terminal. Connect this pin to VIN with a 10ohm resistor and connect a 1µF ceramic capacitor from VCC to GND.
EN	10	Pull this PIN higher than 1V will enable the CHIP. When pulled low, the IC will turn off and the Internal discharge FETwill turn on to discharge the output capacitor through the SW pin.
PGOOD	11	Power-good pin. This is an open-drain output and should be connected to a voltage rail with an external pull-up resistor. During the power on, this pin switches from Low to Hi state when FB voltage reaches above the power good threshold and the internal soft start has finished its operation. It will be pulled low when the FB falls below the power good threshold minus the hysteresis.. It will turn back on when the pull FB rises above the threshold.
SYNC	12	This pin should be tied to ground when not in use. When a clock is connected. The IC will be in synchronous mode and switching frequency is synchronized to external CLOCK.
Power PAD		Ground pin for the power stage and analog circuit. For good thermal connection, this PAD must be connected using VIAs to the GND plane and to the LAND pattern of the IC.

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FUNCTIONAL BLOCK DIAGRAM

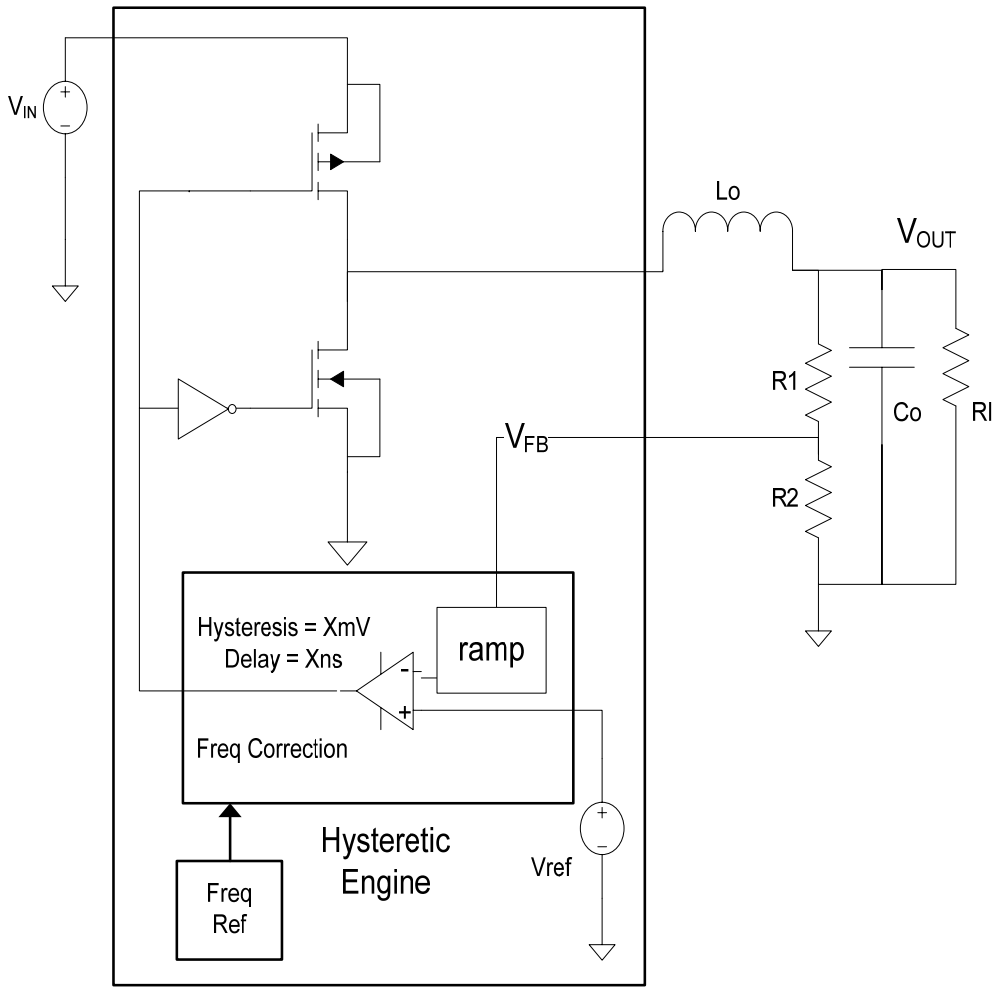

Figure. 1. Functional Block Diagram.

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OPERATION THEORY

Basic Operation

The operation of the controller consists of comparing the V_{fb} voltage to an internal reference. When the V_{fb} voltage is lower than the V_{ref}, the upper switch turns on. When the V_{fb} voltage is higher than V_{ref}, the upper switch turns off and the lower switch turns on. An internal ramp is used to stabilize the switching frequency and keep the V_{fb} immune to the output capacitor, Co, value or parasitic components (i.e. esr, esl). In addition, a frequency control loop ensures the switching frequency is constant under continuous conduction mode of operation.

At light load, the converter automatically reduces the switching frequency to optimize efficiency while ensuring the ripple voltage is low.

Setting of the Output Voltage

The values of R1 and R2 are chosen so according to the following equations:

$$V_{OUT} = \left(\frac{R_1}{R_2} + 1 \right) V_{ref}$$

Startup

The Reference is ramped up from zero voltage to 0.8V in 500µS. During this time, the PGOOD is pulled low. When the reference reaches 0.6V, signaling the end of the soft start cycle, the PGOOD pin will go high within 5µS.

Over Current Protection

The IC has the ability to protect against all types of short circuit protection. It has cycle by cycle short protection that turns off the upper mosfet and ends the cycle when the current exceeds the OCP threshold, when this occurs, the off time is at least 200ns before the upper fet is turned on again After startup, if the FB pin drops below the Feedback UVLO threshold, the chip will go into a hiccup mode of operation. This helps to protect against a crowbar short circuit. The FB UVLO Alarm is not active during startup.

Hiccup Mode of Operation

Hiccup mode of operation will protect the IC during a short of the output. After startup, it will be triggered when the FB UVLO is exceeded

TYPICAL APPLICATION

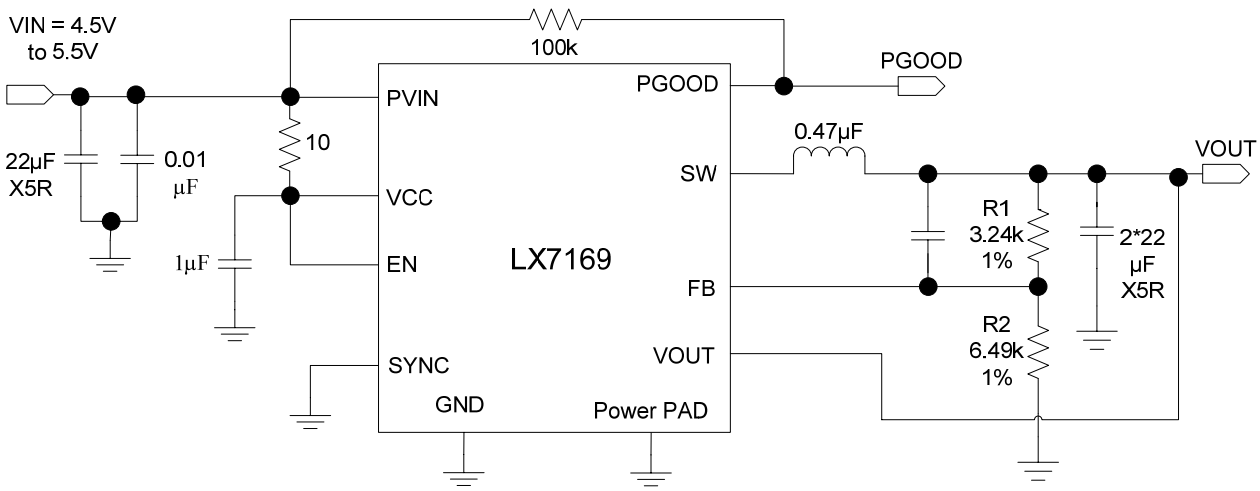
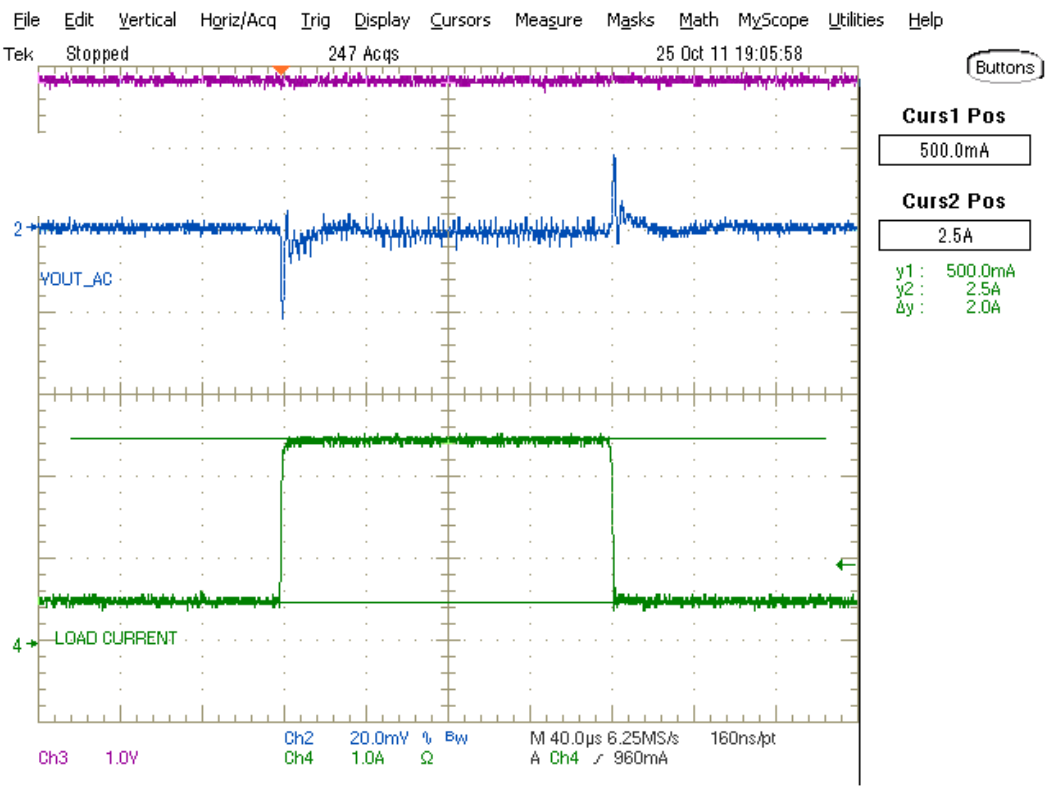


Figure. 2: LX7169 Application



2A Dynamic response (0.47µH, 2x22µF)

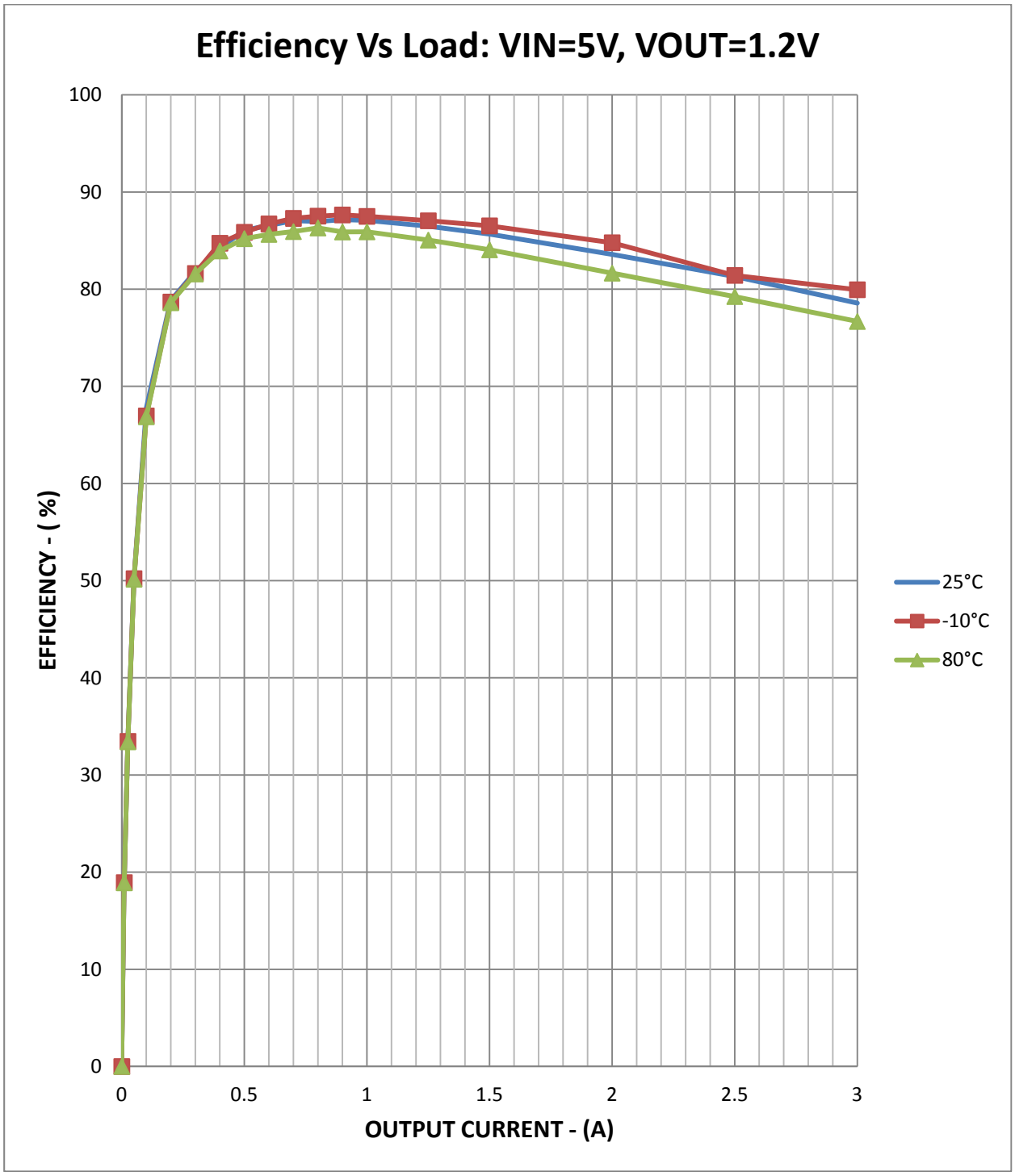


Figure 3. LX7169 Efficiency (Inductor part number: IHLP1616ABER47M01)

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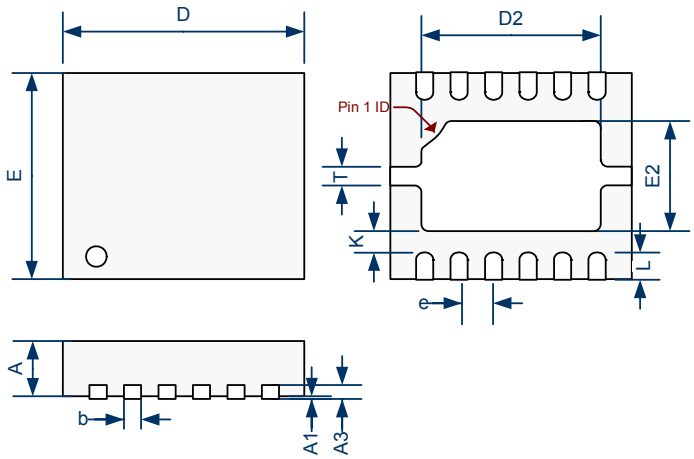
PACKAGE DIMENSIONS

LD 12 Pin Plastic DFN 3x3.5 mm Dual Exposed Pad



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.027	0.031
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.50 BSC		0.138 BSC	
D2	2.45	2.70	0.096	0.106
e	0.50 BSC		0.019 BSC	
E	3.00 BSC		0.118 BSC	
E2	1.45	1.70	0.057	0.067
L	0.35	0.55	0.014	0.022
T	0.20	0.30	0.008	0.012

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.
2. Dimensions are in mm, inches are for reference only.