CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX994
Direct Conversion Receiver

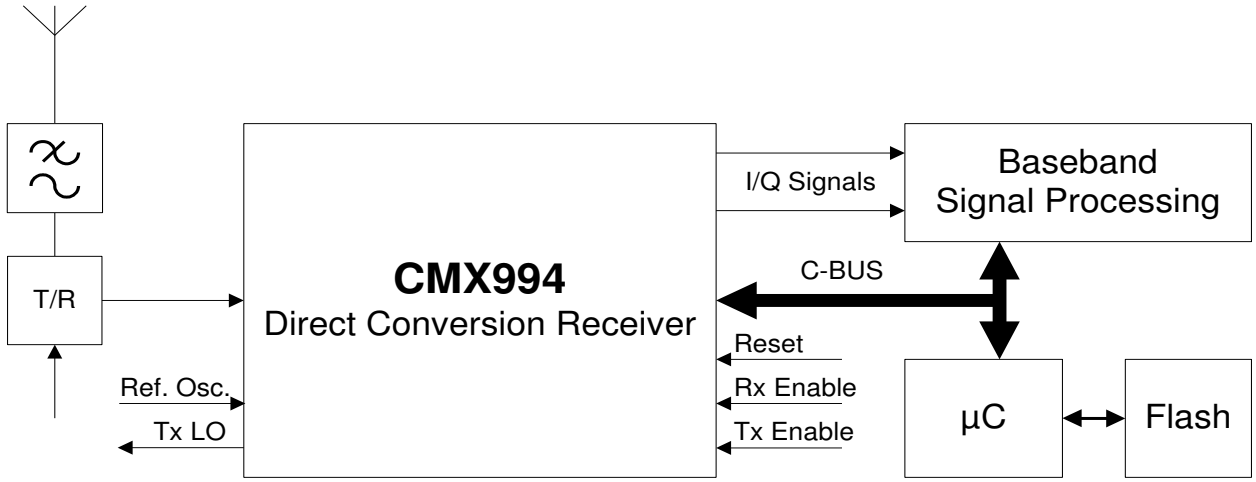
D/994/12 May 2012 Provisional Issue

Features

- **Rx Direct Conversion Receiver**
  - **Direct conversion eliminates image responses**
  - **LNA with gain control**
  - **100MHz to 940MHz I/Q demodulator**
  - **Extended low frequency operation – down to 50MHz**
  - **Precise filtering with bandwidth setting and 1:2:4 bandwidth modes**
- **Local Oscillator**
  - **LO synthesiser**
  - **VCO negative resistance amplifier**
  - **LO divide by 2, 4 or 6 modes**
  - **Tx LO Output**
- **3.0V – 3.6V Low-power Operation**
- **Small size 40-pin VQFN Package**
- **Low-power Mode**

Applications

- **Analogue/digital multimode radio**
- **Software Defined Radio (SDR)**
- **Data telemetry modems**
- **Satellite communications**
- **Constant envelope and linear Rx modulation**
- **Rx function compatible with CMX998 Cartesian Feedback Loop Transmitter**
- **Narrowband: e.g. 25kHz, 12.5kHz, 6.25kHz**
- **Wideband Data**



1 Brief Description

The CMX994 is a direct conversion receiver IC. It includes a broadband LNA with gain control followed by a high dynamic range I/Q demodulator. The receiver baseband section includes amplifiers and precise baseband filter stages. LO generation is provided by an integer-N PLL and a VCO negative resistance amplifier; an external LO may also be used. LO dividers are provided for flexible multi-band operation.

The device operates from a single 3.3V supply over a temperature range of –40°C to +85°C and is available in a small 40-pin VQFN (Q4) package.

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1.1 History

Version	Changes	Date
12	• Operation to 940 MHz and low frequency operation details added. S-Parameter data updated and corrected (Table 9). TBDs removed.	25th April 2012
11	• LO input rated to 2GHz, minor updates.	15th Feb 2012
10	• Operation to 600MHz	21st Dec 2011
9	• CMX994 Specification, 2nd update from evaluation	8th Dec 2011
8	• CMX994 Specification, updated from evaluation	21st Nov 2011
7	• IIP2 value corrected to show average value (section 8.1.3.2)	19th May 2011
6	• Preliminary CMX994 Specification	5th May 2011
5	• Document issued for CMX994	20th September 2010
4	• XX994 Version	1st March 2010
3	• XX994 Version	23rd February 2010
2	• XX994 Version	7th January 2010
1	• Original published document (XX994 Sample Devices)	2nd December 2009

It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

2 Block Diagram

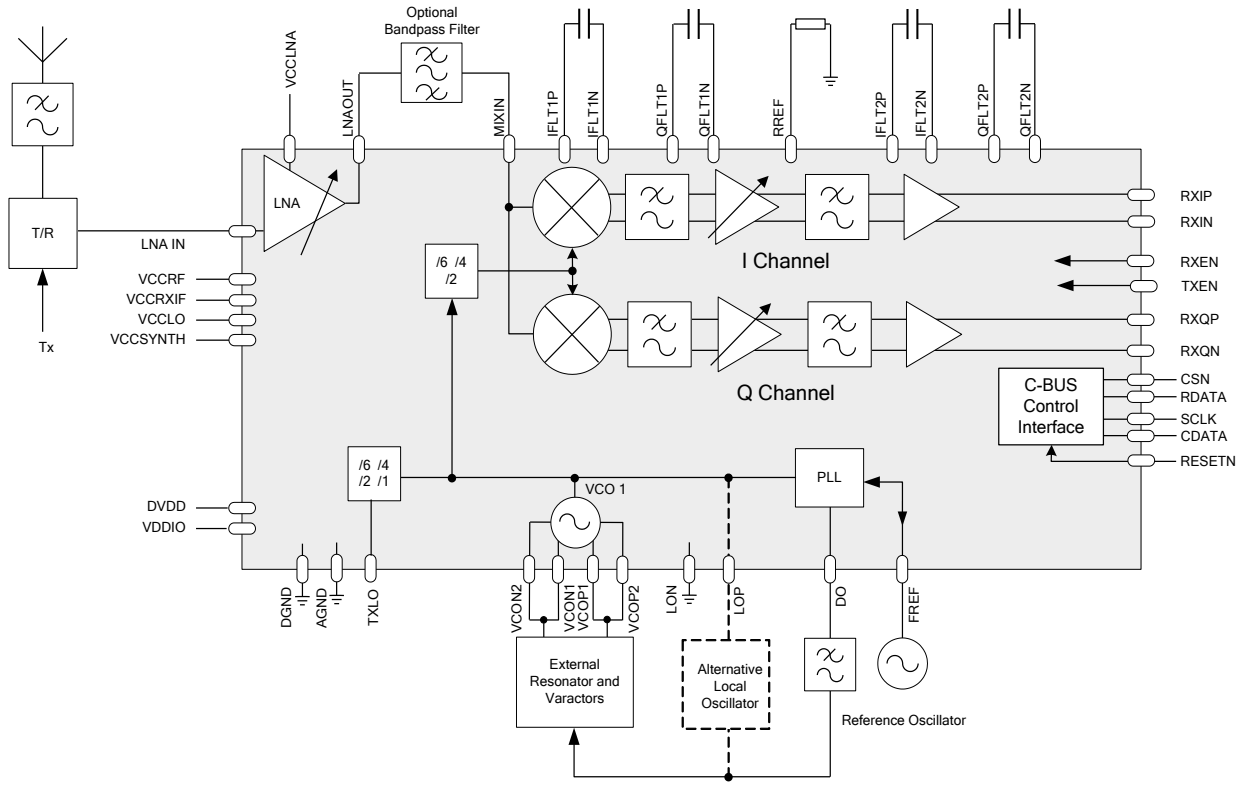


Figure 1 Block Diagram

3 Pin and Signal Lists

3.1 Pin List (40-pin (Q4) Package)

Pin No	Pin Name	Type	Pin Function
1	IFLT2N	IP	I channel 2nd filter capacitor negative
2	IFLT1P	IP	I channel 1st filter capacitor positive
3	IFLT1N	IP	I channel 1st filter capacitor negative
4	VCCRXIF	PWR	Supply for baseband circuits
5	VCCLNA	PWR	Supply for LNA
6	LNAIN	IP	LNA input
7	LNAOUT	OP	LNA output
8	VCCRF	PWR	Supply for RF circuits
9	MIXIN	IP	Rx mixer input
10	TXLO	OP	LO output for Tx
11	VCCLO	PWR	Supply for LO sections
12	LOP	IP	PLL LO positive input
13	LON	IP	PLL LO negative input
14	VCOP1	IP	PLL VCO positive input 1
15	VCOP2	IP	PLL VCO positive- input 2
16	VCON1	IP	PLL VCO1 negative input 1
17	VCON2	IP	PLL VCO1 negative input 2
18	VCCSYNTH	PWR	Supply to Integer N PLL
19	FREF	IP	Reference frequency input
20	DO	OP	PLL Charge Pump output
21	DGND	PWR	Digital ground
22	TXEN	IP	Tx Enable
23	RXEN	IP	Rx Enable
24	CSN	IP	C-BUS Chip Select
25	RDATA	TSOP	C-BUS Data output
26	SCLK	IP	C-BUS Clock input
27	CDATA	IP	C-BUS Data input
28	RESETN	IP	C-BUS/Device Reset (Reset when pin Low)
29	DVDD	PWR	Supply to digital circuits
30	VDDIO	PWR	Supply to C-BUS circuits
31	RREF	IP	Reference resistor for I/Q Filters
32	QFLT1N	IP	Q channel 1st filter capacitor negative
33	QFLT1P	IP	Q channel 1st filter capacitor positive
34	QFLT2N	IP	Q channel 2nd filter capacitor negative
35	QFLT2P	IP	Q channel 2nd filter capacitor positive
36	RXQP	OP	RXQ positive output
37	RXQN	OP	RXQ negative output
38	RXIP	OP	RXI positive output
39	RXIN	OP	RXI negative output
40	IFLT2P	IP	I channel 2nd filter capacitor positive
EXPOSED METAL PAD	AGND	PWR	The exposed metal pad must be electrically connected to analogue ground

Table 1 Definition of Pin Names and Functions

Total = 41 Pins (40 pins and central, exposed metal ground pad)

IP = Input
OP = Output
TSOP = Three-state Output
PWR = Power
NC = Not Connected

3.2 Signal Definitions

Signal Name	Pins	Usage
AV_{DD}	VCCRF, VCCRXIF, VCCSYNTH , VCCLO VCCLNA (see note)	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
VDD_{IO}	VDDIO	Power supply voltage for digital interface (C-BUS)
DV_{SS} (GND)	DGND	Ground for digital circuits
AV_{SS} (GND)	AGND	Ground for analogue circuits

Table 2 Definition of Power Supply and Reference Voltages

4 External Components

4.1 Power Supply and Decoupling

The CMX994 has separate supply pins for the analogue and digital circuitry; a 3.3V nominal supply is recommended for all circuits but the data interface can run at a lower voltage than the rest of the device by setting the VDD_{IO} supply to the required interface voltage, in the range 1.6V to 3.6V.

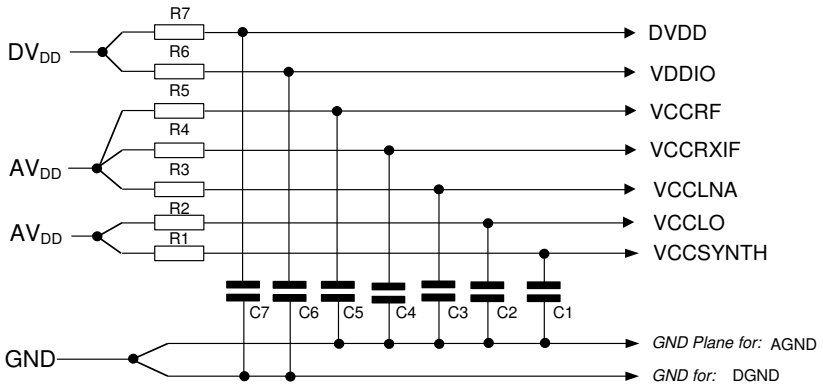


Figure 2 Recommended Power Supply Connections and Decoupling

C1	10nF	R1	10Ω
C2	10nF	R2	3.3Ω
C3	33pF//10nF	R3	3.3Ω
C4	10nF	R4	3.3Ω
C5	10nF	R5	3.3Ω
C6	10nF	R6	10Ω
C7	10nF	R7	10Ω

Table 3 Decoupling Components

Notes:

1. Maximum Tolerances: Resistors ±5%, capacitors ±20%.
2. It is expected that any low-frequency interference on the 3.3 Volt supply will be removed by active regulation; a large capacitor is an alternative but may require more board space and so may not be preferred. It is particularly important to ensure that there is no interference from the VDD_{IO} (which supplies the digital I/O) or from any other circuit that may use the DV_{DD} supply (such as a microprocessor), to sensitive analogue supplies (AV_{DD}). It is therefore advisable to use separate power supplies for digital and analogue circuits.
3. The supply decoupling shown is intended for RF noise suppression. It is necessary to have a small series impedance prior to the decoupling capacitor for the decoupling to work well. This may be achieved cost effectively by using the resistor and capacitor values shown. The use of resistors results in small dc voltage drops (up to approx 0.1V). Choosing resistor values approximately inversely proportional to the dc current requirements of each supply ensures the dc voltage drop on each supply is reasonably matched. In any case, the resultant dc voltage change is well within the design tolerance of the device. If higher impedance resistors are used (not recommended) then greater care will be needed to ensure the supply voltages are maintained within tolerance, even when parts of the device are enabled or disabled.
4. It is advisable to have separate ground planes for analogue and digital circuits.
5. Separate regulators for local oscillator sections (VCCLO, VCCSYNTH) may be beneficial depending on circuit noise and type of regulator and this is why two AV_{DD} connections are shown.

4.2 Receiver

4.2.1 LNA

The following sections show plots and tables of the LNA input (S_{11}) and output (S_{22}) impedance. Separate data is shown for the 50Ω and 100Ω output modes which are selected by $LNAZ_O$ bit in the Rx Gain Register (b3, $16, see section 6.6.1).

Note that at low frequencies capacitive loads on the LNA output are not recommended, a high-pass matching network is preferred.

4.2.1.1 50Ω Mode

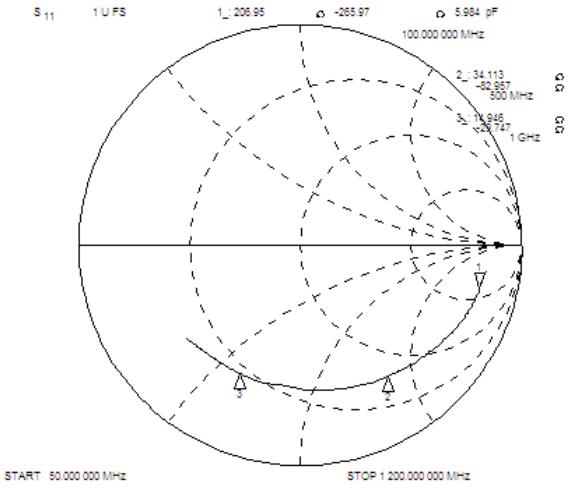


Figure 3 LNA S_{11}

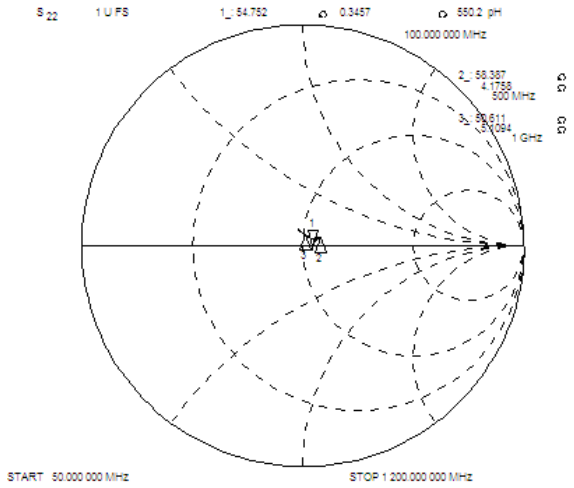


Figure 4 LNA S_{22}

	S_{11}		S_{22}	
Freq (MHz)	**Impedance (Ω-/+jΩ)**	**Equivalent Parallel Circuit (R//C)**	**Impedance (Ω-/+jΩ)**	**Equivalent Parallel Circuit (R//C)**
50	347 – j296	598.9R // 4.5pF	54.4 - j2.4	54.5R // 2.6pF
100	208 – j263	540.7R // 3.7pF	54.8 + j0.4	54.8R
150	129 – j217	496R // 3.6pF	55.3 + j1.7	55.4R
200	93 – j181	444.5R // 3.5pF	56.1 + j2.9	56.3R
250	72 – j154	401.1R // 3.4pF	56.9 + j3.5	57.1R
300	58 – j130	351R // 3.4pF	57.4 + j3.9	57.6R
350	49 – j114	318R // 3.4pF	57.7 + j4.0	58.0R
400	42 – j102	286.5R // 3.3pF	58.1 + j3.9	58.4R
450	37.7 – j91	256.3R // 3.3pF	58.4 + j4.0	58.7R
500	33.9 – j83	235.3R // 3.3pF	58.4 + j4.2	58.7R
550	29.7 – j74	211.8R // 3.4pF	58.3 + j4.1	58.6R
600	27.0 – j66	190.6R // 3.4pF	57.9 + j3.9	58.2R
650	24.7 – j61	173.1R // 3.5pF	57.3 + j3.8	57.6R
700	22.8 – j55	154.9R // 3.5pF	56.7 + j3.9	57.0R
750	21.3 – j50	136.7R // 3.6pF	55.9 + j3.7	56.1R
800	19.9 – j45	121.5R // 3.7pF	55.3 + j3.6	55.5R
850	18.7 – j41	107R // 3.8pF	54.3 + j3.6	54.5R
900	17.2 – j37.0	96.7R // 3.9pF	52.8 + j3.9	53.1R
950	15.7 – j32.9	84.6R // 4.1pF	51.5 + j4.7	51.9R
1000	14.8 – j29.1	72R // 4.3pF	50.7 + j5.1	51.2R

Table 4 LNA S_{11} and S_{22} Impedances and Parallel Equivalent Circuit in 50Ω mode.

4.2.1.2 100Ω Mode

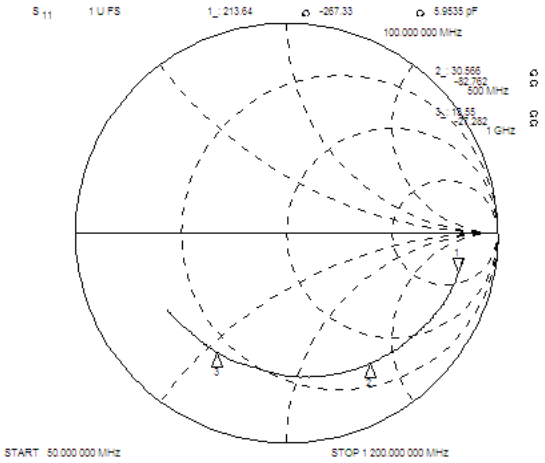


Figure 5 LNA S_{11}

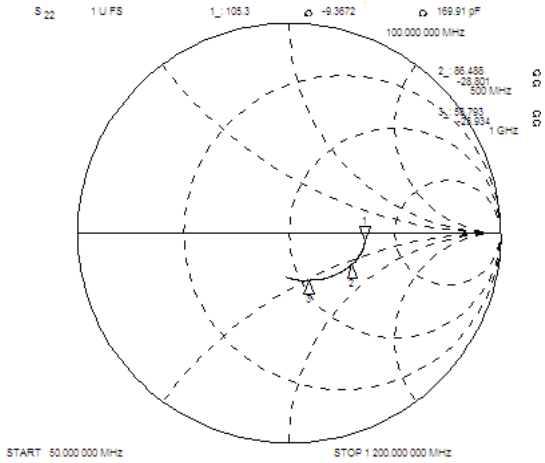


Figure 6 LNA S_{22}

	S_{11}		S_{22}	
Freq (MHz)	**Impedance (Ω-/+jΩ)**	**Equivalent Parallel Circuit (R//C)**	**Impedance (Ω-/+jΩ)**	**Equivalent Parallel Circuit (R//C)**
50	355 - j291	592.6R // 4.4pf	106 - j7.35	106.6R // 2.1pF
100	210 - j267	549.1R // 3.7pF	105 - j9.5	106R // 1.4pF
150	128 - j222	510.6R // 3.6pF	104 - j2.8	105.7R // 1.2pF
200	92 - j186	469.9R // 3.4pF	103 - j15.7	105.3R // 1.2pF
250	70 - j157	422.4R // 3.4pF	101 - j18.6	104.4R // 1.1pF
300	56 - j134	376.9R // 3.4pF	98 - j21.4	103R // 1.1pF
350	45 - j117	345.3R // 3.4pF	96 - j23.9	101.5R // 1.1pF
400	38 - j103	313.1R // 3.4pF	93 - j26.2	99.9R // 1.1pF
450	34.1 - j91	279.2R // 3.4pF	90 - j27.8	98.3R // 1.1pF
500	30.5 - j82	253R // 3.4pF	87 - j28.9	96.1R // 1.1pF
550	26.4 - j73	228.9R // 3.5pF	83 - j29.7	93.7R // 1.1pF
600	24.0 - j66	203.6R // 3.6pF	80 - j30.5	91.3R // 1.1pF
650	21.7 - j59	183.3R // 3.7pF	76 - j30.7	88.6R // 1.1pF
700	19.9 - j53	162.3R // 3.8pF	73 - j30.5	85.6R // 1.1pF
750	18.7 - j47.7	140.8R // 3.9pF	69 - j30.5	82.6R // 1.1pF
800	17.5 - j42.8	122.2R // 4pF	66 - j30.0	79.7R // 1.1pF
850	16.5 - j38.3	105.5R // 4.1pF	63 - j29.5	76.7R // 1.2pF
900	15.4 - j34.4	92.2R // 4.3pF	60 - j28.4	73R // 1.2pF
950	14.2 - j30.5	79.6R // 4.5pF	57 - j27.1	69.5R // 1.2pF
1000	13.4 - j26.7	66.6R // 4.8pF	54 - j26.0	66.3R // 1.2pF

Table 5 LNA S_{11} and S_{22} Impedances and Parallel Equivalent Circuit in 100Ω mode.

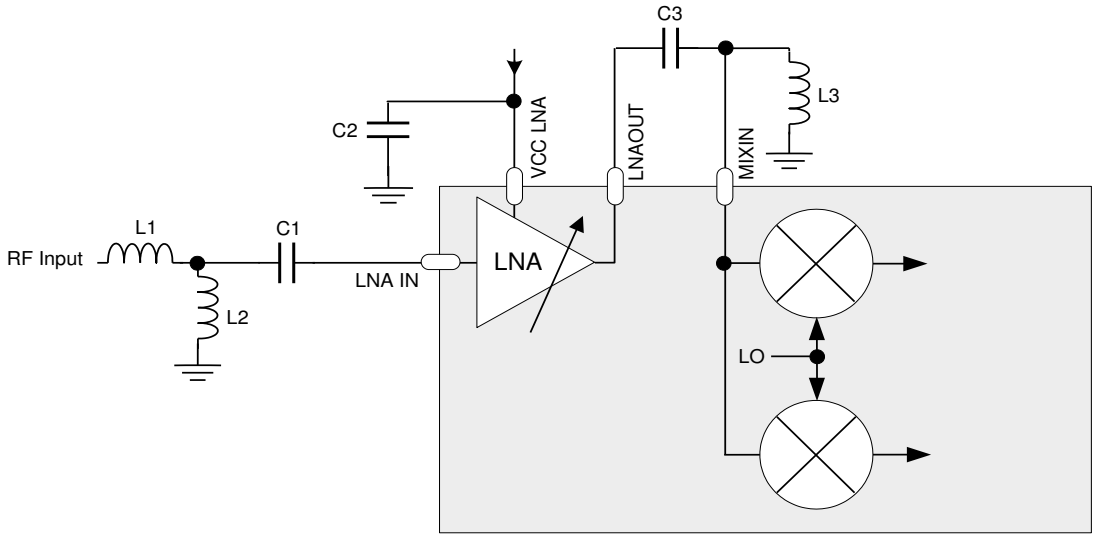


Figure 7 Recommended LNA Configuration and Inter-stage Match

C1	1nF	L1	150 nH
C2	33 pF // 10nF	L2	2.7 pF (capacitor)
C3	18 pF	L3	150 nH

Table 6 150MHz LNA and Inter-stage Components (100Ω output mode)

C1	1nF	L1	39 nH
C2	33 pF // 10nF	L2	82 nH
C3	10 pF	L3	27 nH

Table 7 450MHz LNA and Inter-stage Components (100Ω output mode)

C1	100pF	L1	12 nH
C2	33 pF // 10nF	L2	8.7 nH
C3	4.7 pF	L3	5.6 nH

Table 8 900MHz LNA and Inter-stage Components (50Ω output mode)

4.2.2 Mixers and Baseband Section

Figure 8 is a plot of the typical Rx Mixer input impedance; Table 9 gives the measured impedances and the equivalent parallel circuit at some particular frequencies.

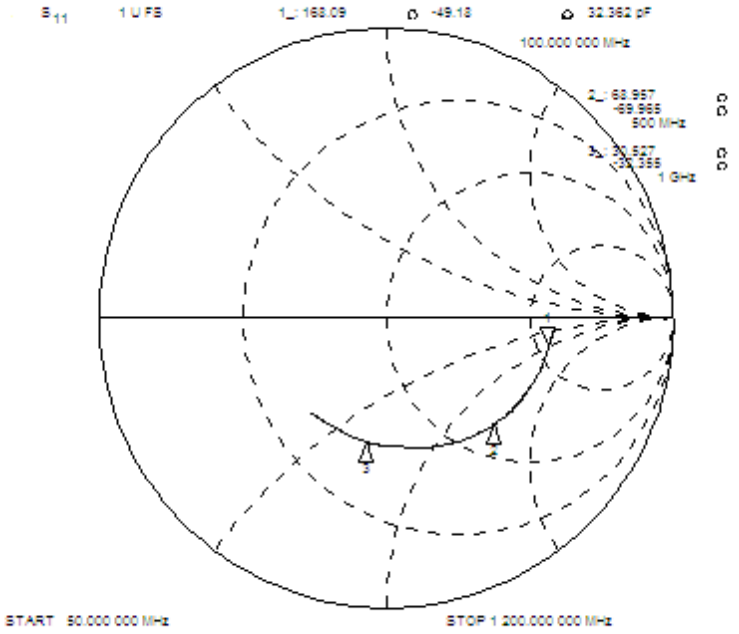


Figure 8 Rx Mixer Input Impedance

Frequency (MHz)	Impedance (Ω-/+jΩ)	Parallel Equivalent Circuit (R // pF)
50	180 - j35.2	186.6R // 3.34pF
100	168 - j49.1	182.4R // 2.6pF
150	153 - j64	180.1R/ / 2.5pF
200	138 - j73	176.4R // 2.4pF
250	124 – j77	171.4R // 2.3pF
300	108 - j79	165.8R // 2.3pF
350	96 - j79	160R // 2.3pF
400	85 - j77	154.1R // 2.3pF
450	76 – j74	147.3R // 2.3pF
500	69 – j70	139.8R // 2.3pF
550	61 - j66	131.5R // 2.4pF
600	55 - j62	124R // 2.4pF
650	50 - j58	116R // 2.4pF
700	46.1 - j53	107.1R // 2.4pF
750	42.7 - j48.9	98.9R // 2.5pF
800	39.8 - j45.3	91.4R // 2.5pF
850	37.2 - j41.6	83.7R // 2.5pF
900	34.8 - j38.1	76.6R // 2.5pF
950	32.3 - j34.9	70.2R // 2.6pF
1000	30.3 - j31.6	63.2R // 2.6pF

Table 9 Rx Mixer Input Impedances and Parallel Equivalent Circuit

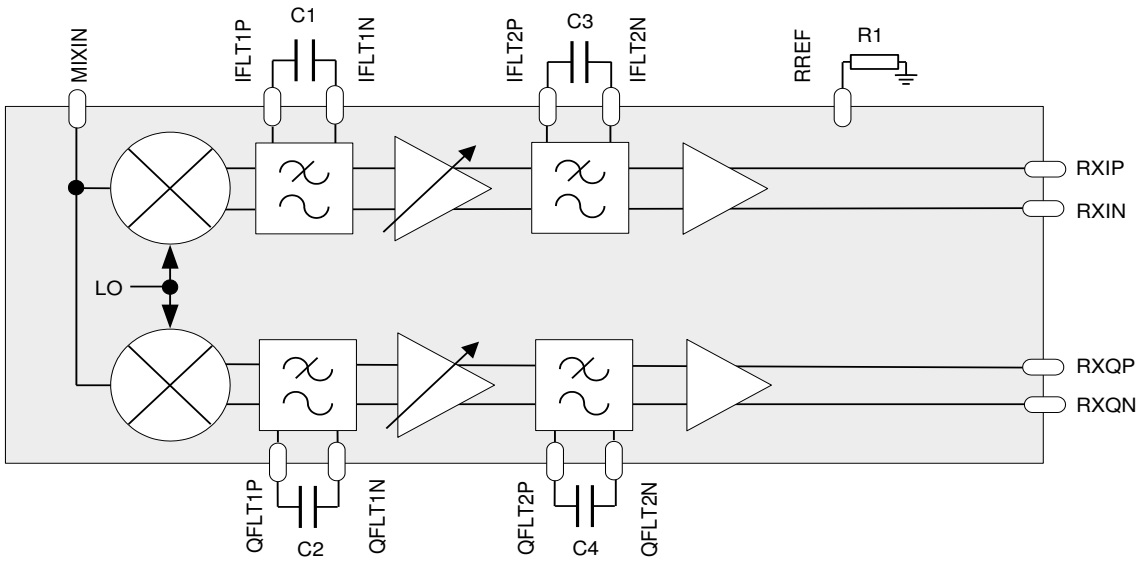


Figure 9 Recommended Receiver Circuit

C1	1.5nF	C4	3.9nF
C2	1.5nF	R1	10kΩ
C3	3.9nF		

Table 10 Receiver Components

The bandwidth of the first baseband filters are set by capacitors C1 and C2. Capacitors C3 and C4 together with the reference resistor R1 set the bandwidth of the second baseband filters. Component selection will vary depending on the desired filter bandwidths. For further details see sections 5.2.2 and 5.2.3.

4.3 Local Oscillator

4.3.1 Local Oscillator Input

LON and LOP signals form a differential signal pair however the LO input may be driven by a single-ended source, in which case pin LOP should be connected to the LO signal and LON may be connected directly to ground. The inputs have internal ac coupling, so external dc blocking capacitors are not required.

4.3.2 VCO and PLL

A typical configuration for using the internal VCO negative resistance amplifier at 440MHz is shown in Figure 10. The other external components required to complete the PLL are the loop filter components, see Figure 11 – which shows a third-order loop filter; typical values for a 500Hz bandwidth are given in Table 12.

VCOP1 should be shorted directly to VCOP2 and similarly VCON1 to VCON2 in order to form the negative resistance loop. It is recommended that the parallel LC tank (L1/C1) is situated as close to the package as possible, with the L closest to the device pins. Also the shorting of VCOP1 to VCOP2 and of VCON1 to VCON2 occurs as close as possible to the tank circuit – this minimises the effects of series inductance on the oscillator behaviour.

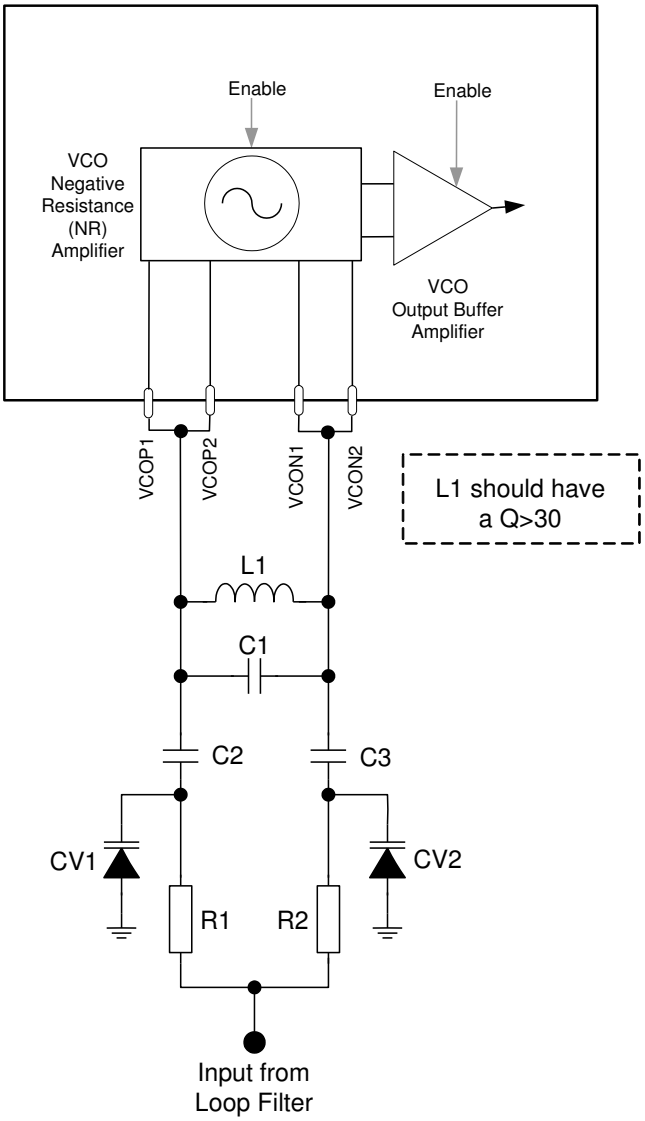


Figure 10 Example External Components – VCO External Tank Circuit

L1	8.2 nH (Note 1)	CV1	SMV1705-079LF
C1	8.2 pF (Note 2)	CV2	SMV1705-079LF
C2	22pF	R1	10kΩ
C3	22pF	R2	10kΩ

Note 1: Tolerance of 2% or better recommended
Note 2: Tolerance of 5% or better recommended

Table 11 Internal VCO Amplifier Tank Circuit for 440MHz Operation

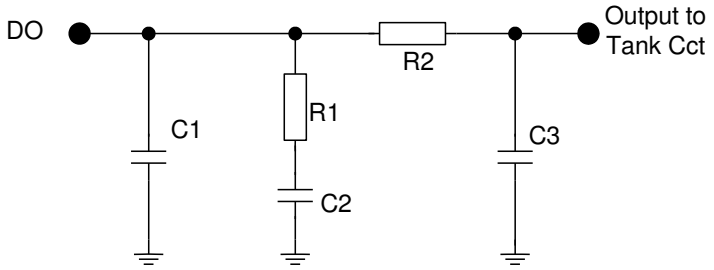


Figure 11 Example External Components – PLL Loop Filter

C1	150nF	R1	1.5kΩ
C2	1000nF	R2	2.4kΩ
C3	15nF		

Table 12 3rd Order Loop Filter Circuit Values

4.4 RESETN

The RESETN pin generates a reset signal when low. The RESETN pin has an internal pull-up resistor of 100kΩ connected to VDD_{IO}.

5 General Description

The architecture of the CMX994 integrated circuit and related system is shown in Figure 1.

The CMX994 is a receiver IC featuring I/Q demodulators intended for use as a direct conversion receiver. The device has flexible LO inputs integer-N PLL and an on-chip negative resistance amplifier which, with the addition of suitable external components, provides a VCO.

The receiver is fully integrated with a Low Noise Amplifier (LNA) preceding the down-converter section. The LNA may be configured with one of two possible output impedance settings (100Ω or 50Ω). With the 50Ω mode selected, there is more gain available but the circuit will consume an additional 2mA of current. The 50Ω mode has primarily been included for use at frequencies of 450MHz or higher. It should be noted that as the output impedance is not the same for each setting, the required matching components between the LNA and mixer will be different for each case.

The high-linearity down-converting mixers are immediately followed by a baseband filter stage. The bandwidth of this section is set by external capacitors. This first stage of filtering is designed to remove off-channel blocking signals prior to baseband amplification. Following these filters, gain is applied via a variable gain amplifier. Further filtering is then applied and again the bandwidth of the filters is determined by external capacitors. A reference resistor must also be fitted; this is used to calibrate the internal filter circuits to ensure the cut-off point of the filters is accurately controlled. This system allows effective correction for the analogue response to be applied in signal processing following the CMX994. The output of the CMX994 is differential I/Q signals; these may be applied to analogue-to-digital converters such as those in the CMX981, CMX910, CMX7163 or the CMX7164 ICs.

The receiver I/Q chain includes the facility to correct for inherent dc offsets in the hardware. This process is intended to optimise the dynamic range of the system and must be controlled by the microprocessor or DSP that processes the I/Q signals from the CMX994. DC offsets are a well known issue with direct conversion receivers. In dynamic signal environments dc offset removal algorithms will be required to track and remove dc offsets generated by off-channel signals.

The receiver sections have a low-power mode which reduces the current drawn by the device. This mode may be used where degraded intermodulation performance can be accepted.

The Local Oscillator section features an integer-N Phase Locked Loop (PLL). This may be used with the on-chip VCO or with an external VCO. The on-chip VCO consists of a negative resistance amplifier and buffers, which allows an external inductor together with external varactor diodes to determine the operating frequency and tuning range. The use of external components allows optimum phase noise to be achieved. The Rx LO signal may be divided by 2, 4 or 6. There is also a Tx LO output provided and the Tx LO signal may be divided by 1, 2, 4 or 6. Alternatively the on-chip PLL and VCO can be disabled and an external LO source supplied.

All the features of the CMX994 may be controlled by the C-BUS control interface.

The following sections describe specific features of the CMX994.

5.1 General Operation

5.1.1 Rx/Tx Enable

The CMX994 has Tx Enable and Rx Enable pins and the same function can be accessed via C-BUS using the General Control Register (section 6.2). The logical signals 'Tx ON' and 'Rx ON' are a combination of the C-BUS signal and the hardware signals as shown in Table 13. Thus either C-BUS or hardware enable signals may be used, with the unused mode being set to '0'.

Tx (or Rx) Enable Pin	C-BUS Tx or Rx Enable	'Tx ON' or 'Rx ON'
0	0	0
1	0	1
0	1	1
1	1	1

Table 13 Tx (or Rx) Enable Operation

'Tx ON' enables the following sections of the device:

- Tx divider (see also Figure 1 and section 6.9.1)

'Rx ON' enabled the following sections of the device:

- LNA
- Down-converters and I/Q baseband amplifiers
- Rx LO divider

5.2 Receiver Operation

5.2.1 DC Offset Correction

Digitally-controlled dc offset correction is provided which is capable of reducing the offset to 25mV or less for errors of up to +/-200mV[1]. This represents a reduction in dynamic range of about 0.1dB for a typical ADC input signal range (2Vp-p) and is therefore negligible. The required correction must be measured externally as such measurements are application specific. The correction is applied close to the start of the I/Q baseband chain and therefore maximises dynamic range in the analogue sections.

The correction is applied in a differential manner so positive and negative corrections are possible, see Figure 12. This allows the dc to be corrected to the nominal dc bias level. The voltage sources are scaled in a binary fashion so multiple sources can be added to provide the desired correction. The same arrangement applies independently on both I and Q channels.

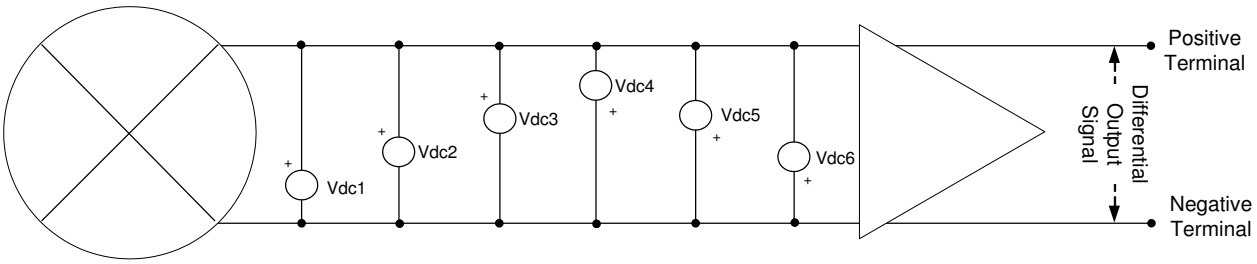


Figure 12 Simplified Schematic of How DC Offset Corrections are Applied

[1] This can be doubled to 400mV using bit 2 of the Rx Control Register (see section 6.3) although this also halves the resolution available.

Source	Voltage Correction at Output for Maximum Gain in Baseband Amplifiers	Correction Polarity
Vdc1	25mV	Positive terminal increase, Negative terminal decrease
Vdc2	50mV	Positive terminal increase, Negative terminal decrease
Vdc3	100mV	Positive terminal increase, Negative terminal decrease
Vdc4	25mV	Negative terminal increase, Positive terminal decrease
Vdc5	50mV	Negative terminal increase, Positive terminal decrease
Vdc6	100mV	Negative terminal increase, Positive terminal decrease

Table 14 DC Offset Correction Adjustments

5.2.2 Receiver Filters and Bandwidth Options

The I and Q channels incorporate two stages of filtering to reduce blocking signals and to attenuate nearby channels. This allows the wanted signal to be maximised without significant distortion being introduced as a result of unwanted larger signals saturating the later amplification stages.

The CMX994 supports multiple channel bandwidths, providing scalable filtering in the baseband (I/Q) chain. Two filter stages are provided. The post mixer filter provides rejection of large off-channel signals such as those typically used in blocking tests. With this protection in place some gain is provided before narrower filters that provide rejection of the adjacent channel. Following this filter, the remainder of the receiver gain is provided. Both filter stages have single-pole characteristics, having -3dB frequency points set by separate external capacitors.

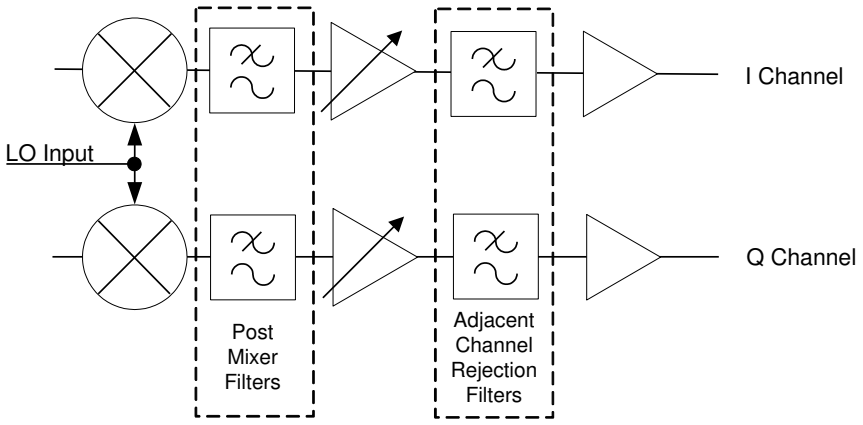


Figure 13 Baseband I/Q Filtering

The bandwidths of the second filter stage can be scaled to allow multiple channel bandwidths to be supported by the CMX994. A typical requirement is to support 6.25kHz, 12.5kHz and 25kHz channels, so the scaling of the Adjacent Channel Rejection (ACR) filter is 1 : 2 : 4 via a bandwidth mode control. Using the recommended external capacitors for a 6.25kHz design (see section 4.2.2), the ACR filter bandwidth (-3dB) is 2kHz. This provides 9dB rejection of the adjacent channel and 15dB rejection at 12.5kHz. Using the bandwidth scaling control, the 2kHz filter bandwidth can then be changed to 4kHz or 8kHz (see Rx Control Register, section 6.3), without changing external components. See also section 7.3.6.

The ACR filter will introduce some deterministic distortion in the signal passband, this distortion can be compensated by using filters external to the CMX994. Example coefficients for external compensation filters can be provided by CML (see section 7.2).

The scaling of the post-mixer filter is less critical. The bandwidth (-3dB), using the recommended values, is approximately 88kHz. This should be suitable for all the channel bandwidths up to 25kHz, so no scaling is provided.

5.2.3 Baseband Filter Design and Required Correction

The pole frequencies of the filter stages are set by the addition of external capacitors (see also section 4.2.2); the resistors are internal to the chip and those on the second filter stage are trimmed so as to match the external 10kΩ reference resistor[2].

First stage filter.
Resistors have 20% tolerance

Second stage filter.
Resistors are matched to external 10k, 1% resistor

Figure 14 Schematic Representation of Filters used in the I and Q Paths

Filtering close to the passband distorts the signal and increases the BER, so it is necessary to provide correction for the filter distortion in subsequent external digital filtering.

Both filter stages are single-pole filters. The first filter stage is designed to reduce blocking signals and it will typically be set at 4 x the maximum required channel spacing. As a result, tolerance is not particularly critical and it is usually not necessary to compensate the wanted signal for this filter. The second filter is designed to operate close to, or within, the passband. It is therefore important that compensation is provided for the wanted signal.

Different modulation schemes occupy different bandwidths within a channel, so optimisation of the filter positioning will vary depending on the modulation scheme. Some experimentation may be required to get the best results but, as a guide, the second filter stage should have its frequency set to between 30% and 40% of the channel spacing. The aim is to reduce adjacent and close-in channels as much as possible. Provided the filter effects are compensated for later, the lowering of the signal amplitude at the band edges is usually well tolerated, although the extent of this will depend on the modulation scheme used.

The CMX994 allows up to three different channel spacings to be selected via the C-BUS interface. So if, for example, the three channel spacings required are 6.25kHz, 12.5kHz and 25kHz, then the first filter should be set at a nominal desired frequency to ensure large blocking signals are rejected, typically a cut off frequency around 100kHz would be suitable. If only two channel spacings are required, of 6.25kHz and 12.5kHz for example, then it would be slightly beneficial to set the post mixer filter bandwidth to 50kHz.

Note that the three channel spacings are always in a 1:2:4 ratio relative to the smallest channel spacing, which is set by external components.

[2] The external resistor should be 1% tolerance or better.

The second stage filter capacitor should be selected for the smallest bandwidth requirement. The calculation for the capacitor value is as follows:

$$C = \frac{1}{2 \bullet \pi \bullet f \bullet 20{,}000}$$

Where f = filter pole frequency (-3dB point).

So a capacitor of 4nF would yield a frequency pole of 1989Hz. This may be a typical figure when using a channel spacing of 6.25kHz. To maintain the accuracy of the compensation the capacitor must have a low temperature coefficient and tolerance better than or equal to 2%.

A compensation filter would need to be applied in the digital domain having the inverse characteristic. This would be:

$$H(s) = 1 + \frac{s}{2 \bullet \pi \bullet f}$$

This would normally be implemented as a FIR filter. It should be followed with another non-critical FIR that rolls off the signal when out of band. This second filter may be part of a required channel filter.

Selecting 2x or 4x bandwidth will require the compensation filter to be adjusted in proportion.

The first stage filter capacitor may be calculated in a similar way:

$$C = \frac{1}{2 \bullet \pi \bullet f \bullet 1200}$$

Where f = filter pole frequency (-3dB point).

So a capacitor of 1.5nF would yield a frequency pole of 88.4kHz. This may be a typical figure if the maximum channel spacing required were 25kHz. There is a wider tolerance on this, as the internal resistors are not trimmed. Consequently it is not required to have a low tolerance value on the first stage filter capacitor.

Should it be required to have this closer to the passband then a correction filter may be required. This would have the same form as for the correction filter for the second stage.

Because both filter stages are handling large dynamic signals, the linearity of the external capacitors is important. Use of good dielectric materials is recommended; poor linearity could result in a degradation of the on-channel signal in the presence of large off-channel interferers.

Examples of filter coefficients for a typical application are given in section 7.2.

5.2.4 Operation at Wider Bandwidths

It is possible to use a much wider channel bandwidth than those used as examples elsewhere in this document, for example circa 800kHz channels. For maximum I/Q bandwidth capacitors C1, C2, C3 and C4 in Figure 9 should be removed. In this case the filter calibration circuit should be disabled using b7 of the VCO Control Register ($25), see section 6.9.1.

5.3 Local Oscillator Operation

The CMX994 can use either an external Local Oscillator (LO) source or the on-chip VCO and PLL. The on-chip integer-N PLL can also be used with an external VCO connected to the LO input.

5.3.1 PLL

The CMX994 provides an integer-N PLL that can be used to create the local oscillator, see Figure 15. The CMX994 provides a VCO negative resistance amplifier, so only a tank circuit needs to be implemented externally. Alternatively, this amplifier can be bypassed and an external VCO can be used.

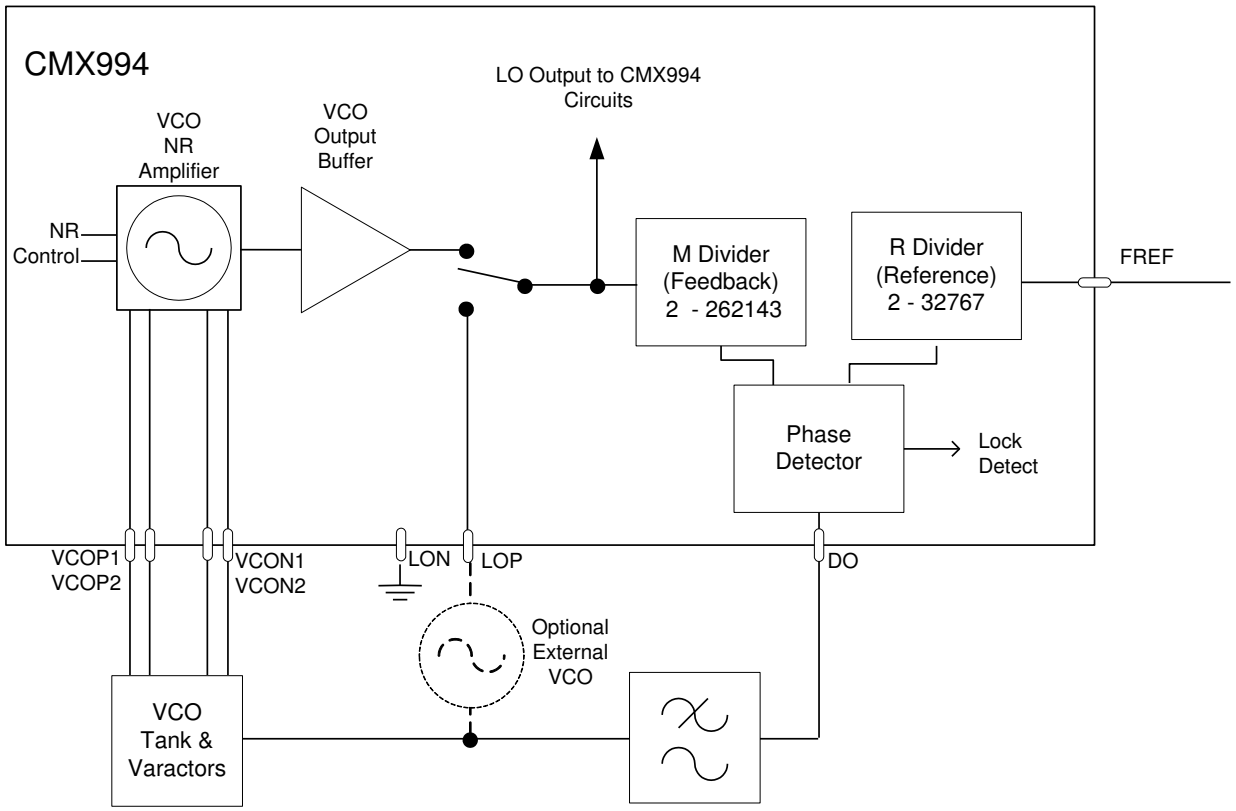


Figure 15 CMX994 Local Oscillator

The integer-N PLL has programmable M and R dividers as shown in Figure 15. The phase detector provides a charge pump output which requires a suitable loop filter to convert this signal into a control voltage for a VCO. The phase detector can be turned off (high impedance mode) and the PLL section disabled if an external LO is to be used, see section 5.3.2 and 6.7 for control details.

The output frequency of the PLL is set by the following calculation:

$$f_{out} = f_{ref} \times (M / R)$$

where

f_{out} = The desired output frequency in MHz
f_{ref} = The reference frequency supplied to the PLL on pin FREF in MHz
M = Divider value programmed in the M divider register (see section 6.7.1)
R = Divider value programmed in the R divider register (see section 6.8.1)

The PLL only supports VCOs with a positive tuning slope, i.e. a higher tuning voltage from DO results in a higher oscillation frequency from the VCO.

The PLL has a lock-detect function that can be evaluated using register $D2, b6 (section 6.7.2).

The VCO amplifier is a negative resistance amplifier requiring an external tank circuit (see section 4.3). The amplifier has two control bits available in the VCO control register (section 6.9.1, register $25, b2 – b3). These bits can be used to optimise performance for a particular tank circuit depending on its Q value.

5.3.2 PLL Enable

The PLL block can be enabled from the General Control Register $11, b2 (section 6.2.1) and the PLL M Divider Register $22, b7 (section 6.7.1). An AND function is performed on these two bits (Table 15).

General Control Register $11, b2	PLL M Divider Register $22, b7	PLL Enable
0	0	No
0	1	No
1	0	No
1	1	Yes

Table 15 PLL Control

With the PLL disabled an external local oscillator may be supplied to the CMX994.

6 C-BUS Interface and Register Descriptions

The C-BUS serial interface supports the transfer of data and control or status information between the CMX994's internal registers and an external host. Each C-BUS transaction consists of the host sending a single Register Address byte, which may then be followed by zero or more data bytes that are written into the corresponding CMX994 register, as illustrated in Figure 16.

Data sent from the host on the Command Data (CDATA) line is clocked into the CMX994 on the rising edge of the Serial Clock (SCLK) input. The C-BUS interface is compatible with common µC/DSP serial interfaces and may also be easily implemented with general purpose I/O pins controlled by a simple software routine. Section 8.1.3.6 gives the detailed C-BUS timing requirements.

Whether a C-BUS register is of the read or write type, it is fixed for a given C-BUS register address thus one cannot both read and write the same C-BUS register address. The CMX994 supports several pairs of C-BUS register addresses in order to read and write the same information.

In order to provide ease of addressing when using this device with the CMX998 (Cartesian Feed-back Loop Transmitter IC), the C-BUS addresses below are arranged so as not to overlap those used on the CMX998. Thus, a common chip select (CSN) signal can be used, as well as common CDATA (SDI on CMX998), RDATA (SDO on CMX998) and SCLK signals. Also note that the General Reset ($10) command on the CMX994 differs from other CML devices (such as CMX998), which use $01 for this General Reset function. This allows the CMX994 and CMX998 to be connected to the same interface pins, including chip select, assuming the drive capabilities of the host are adequate.

The following C-BUS register addresses are:

Write Only register;

General Reset Register (Address only, no data)	Address $10
General Control Register, 8-bit write only	Address $11
Rx Control Register, 8-bit write only	Address $12
Rx Offset Register, 8-bit write only	Address $13
IM Control Register, 8-bit write only	Address $14
Rx Gain Register, 8-bit write only	Address $16
PLL M Divider Register, 8-bit write only	Address $20-$22
PLL R Divider Register, 8-bit write only	Address $23-$24
VCO Control Register, 8-bit write only	Address $25

Read Only register;

General Control Register, 8-bit read only	Address $E1
Rx Control Register, 8-bit read only	Address $E2
Rx Offset Register, 8-bit read only	Address $E3
IM Control Register, 8-bit read only	Address $E4
Rx Gain Register, 8-bit read only	Address $E6
PLL M Divider Register, 8-bit read only	Address $D0-$D2
PLL R Divider Register, 8-bit read only	Address $D3-$D4
VCO Control Register, 8-bit read only	Address $D5

Notes:

- All registers will retain data if DVDD and VDDIO pins are held high, even if all other power supply pins are disconnected.
- If clock and data lines are shared with other devices, DVDD and VDDIO must be maintained in their normal operating ranges otherwise ESD protection diodes may cause a problem with loading the signals connected to SCLK, CDATA and RDATA pins, preventing correct programming of other devices. Other supplies may be turned off and all circuits on the device may be powered down without causing this problem.

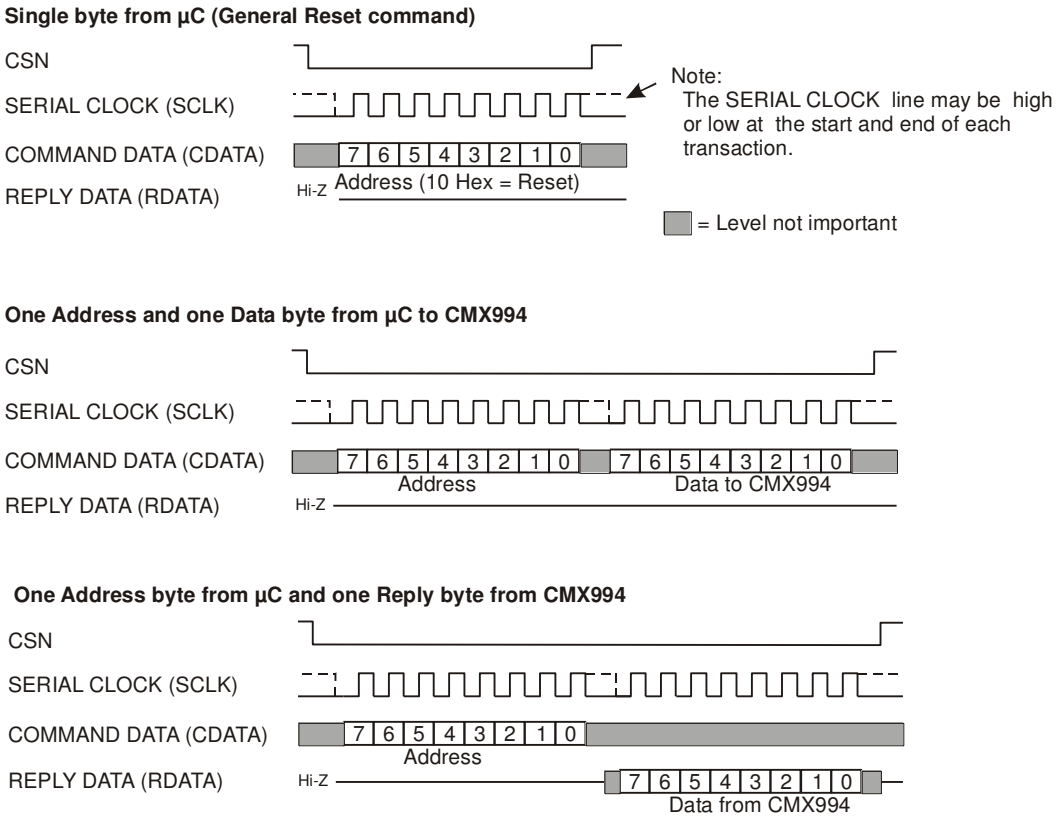


Figure 16 C-BUS Transactions

6.1 General Reset Register

6.1.1 General Reset Register: C-BUS address $10 (no data)

A command to this register resets the device and clears all bits of all registers. The General Reset command places the device into Powersave mode.

Whenever power is applied to the DVDD pin, a built-in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. The RESETN pin on the device will also reset the device to the same state.

6.2 General Control Register

6.2.1 General Control Register: C-BUS address $11
8-bit write-only

This register controls general features such as Powersave.

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	En Bias	Freq2	Freq1	LP	VCOEN	PLLEN	RXEN	TXEN

General Control Register b7 and b4 – b0

These bits control power up/power down of the various blocks of the IC.
In all cases '1' = power up, '0' = power down.

B7	Enable bias generator
b4	Enables low power mode. When b4 = '0' the device is operating normally, when b4= '1' the device will have reduced power consumption and reduced intermodulation performance, see also section 7.3.4.
b3	Enable VCO: When b3 ='1' the setting of the VCO Control Register ($25) take effect. For details of VCO Control Register see section 6.9.
b2	PLL Enable: This bit enables the PLL and is ANDed with PLL M-Divider Register ($21) b7 – section 6.7. See also section 5.3.2.
b1	C-BUS Rx Enable, See section 5.1.1
b0	C-BUS Tx Enable, See section 5.1.1

General Control Register b6 – b5

These bits optimise the amplitude of the local oscillator path within the IC in order to maintain phase balance and noise performance of the receiver mixers over the full range of operating frequencies.

Bit:	b6	b5	
	0	0	Operation 100MHz – 150MHz
	0	1	Operation 150MHz – 300MHz
	1	0	Operation 300MHz – 700MHz
	1	1	Operation 700MHz – 940MHz

6.2.2 General Control Register: C-BUS address $E1
8-bit read-only

This register reads the value in register $11, see section 6.2.1 for details of bit functions.

6.3 Rx Control Register

6.3.1 Rx Control Register: C-BUS address $12
8-bit write-only

This register controls general features of the receiver such as Powersave.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	Mix Pwr	IQ Pwr	LNA Pwr	ACR Flt2	ACR Flt1	DC Range	DIV2	DIV1

Rx Control Register b7 – b5
These bits control power up/power down of the various blocks of the IC.
In all cases '0' = power up, '1' = power down.

B7	Disable receiver mixers and divider (see note)
b6	Disable baseband amplifier and filters (see note)
b5	Disable LNA (see note)

Note: These control signals disable the appropriate blocks of the receiver when 'Rx ON' is active. If 'Rx ON' is not active all receiver circuits will be in powersave mode.

Rx Control Register b4 – b3
The baseband I/Q chain provides a narrow filter for rejecting adjacent channel signals. The bandwidth of this filter may be scaled using these bits. For further details see sections 5.2.2 and 5.2.3 and 7.3.6.

Bit:	b4	b3	
	0	0	Minimum bandwidth
	0	1	Intermediate bandwidth
	1	0	Maximum bandwidth
	1	1	Reserved, do not use

Rx Control Register b2
When b2 ='0' the range of DC correction of the I/Q output is nominal (see sections 5.2.1 and 6.4). With b2 ='1' the total correction range is twice the nominal specified in section 6.4 with all steps doubled in value.

Rx Control Register b1 – b0
Receiver LO divider control.

Bit:	b1	b0	
	0	0	LO divided by 2
	0	1	LO divided by 4
	1	0	LO divided by 6
	1	1	Reserved, do not use

6.3.2 Rx Control Register: C-BUS address $E2
8-bit read-only

This read-only register mirrors the value in register $12; see section 6.3.1 for details of bit functions.

6.4 Rx Offset Register

6.4.1 Rx Offset Register: C-BUS address $13
8-bit write-only

All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	QDC3	QDC2	QDC1	QDC0	IDC3	IDC2	IDC1	IDC0

Rx Offset Register b7 – b0
I/Q DC offset correction, see section 5.2.1 for further details.

The step size can be doubled using the Rx Control Register ($12), b2 (see section 6.3.1).

The values in the table below are the effects of the offset at the maximum VGA gain (minimum attenuation) setting. They are proportionately lower for lower gain settings (as set by the Rx Gain Register (b2 – b0). The aim of this Rx Offset Register is to allow output offsets to be reduced sufficiently (typically <25mV) to avoid any significant reduction in the dynamic range of any subsequent ADC. It is expected that demodulation software in the baseband processor would be required to correct for the remaining offset as part of the demodulation process.

See also section 7.3.2.

Bit: b3 b2 b1 b0	b7 b6 b5 b4	I Channel at maximum gain / Q Channel at maximum gain
1 1 1 1	1 1 1 1	-175mV
1 1 1 0	1 1 1 0	-150mV
1 1 0 1	1 1 0 1	-125mV
1 1 0 0	1 1 0 0	-100mV
1 0 1 1	1 0 1 1	-75mV
1 0 1 0	1 0 1 0	-50mV
1 0 0 1	1 0 0 1	-25mV
1 0 0 0	1 0 0 0	No correction
0 1 1 1	0 1 1 1	+175mV
0 1 1 0	0 1 1 0	+150mV
0 1 0 1	0 1 0 1	+125mV
0 1 0 0	0 1 0 0	+100mV
0 0 1 1	0 0 1 1	+75mV
0 0 1 0	0 0 1 0	+50mV
0 0 0 1	0 0 0 1	+25mV
0 0 0 0	0 0 0 0	No correction

6.4.2 Rx Offset Register: C-BUS address $E3
8-bit read-only

This read-only register mirrors the value in register $13; see section 6.4.1 for details of bit functions.

6.5 Intermodulation Control Register

6.5.1 IM Control Register: C-BUS address $14
8-bit write-only

This register controls features of the receiver that support Intermodulation optimisation.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	0	0	IM5	IM4	IM3	IM2	IM1	IM0

IM Control Register b7 – b6
Reserved, set to '0'.

IM Control Register b5 – b0
These bits allow the user to adjust the intermodulation performance of the LNA. The default value is '0' for all the bits. Improved intermodulation can be achieved with a particular value in these bits. For further details see section 7.3.4.

6.5.2 IM Control Register: C-BUS address $E4
8-bit read-only

This read-only register mirrors the value in register $14; see section 6.5.1 for details of bit functions.

6.6 Rx Gain Register

6.6.1 Rx Gain Register: C-BUS address $16
8-bit write-only

This register controls receiver Gain Control.
All bits of this register are cleared to '0' by a General Reset command.

Bit:	7	6	5	4	3	2	1	0
	GS1	GS0	LNA Gain2	LNA Gain1	LNA Z_0	G2	G1	G0

Rx Gain Register b7 – b6
LNA Gain Control Step: These bits control the LNA gain steps; the nominal step is 6dB however the actual step size can be adjusted by+0.7dB, +1.4dB or +2.8dB, as shown in the table below. For further information see section 7.3.3.

Bit:	b7	b6	
	0	0	Nominal step size of 6dB
	0	1	Nominal step size + 0.7dB
	1	0	Nominal step size+1.4dB
	1	1	Nominal step size +2.8dB

Rx Gain Register b5 – b4
LNA Gain Control: These bits control the LNA gain in nominal 6dB steps, as shown in table below (see also b7 – b6).

Bit:	b5	b4	
	0	0	LNA gain = Nominal
	0	1	LNA gain = Nominal -6dB
	1	0	LNA gain = Nominal -12dB
	1	1	LNA gain = Nominal -18dB

Rx Gain Register b2 – b0
I/Q Baseband VGA Control.

Bit:	b2	b1	b0	VGA value
	1	1	1	VGA = -42dB
	1	1	0	VGA = -36dB
	1	0	1	VGA = -30dB
	1	0	0	VGA = -24dB
	0	1	1	VGA = -18dB
	0	1	0	VGA = -12dB
	0	0	1	VGA = -6dB
	0	0	0	VGA = 0dB (Maximum gain)

Rx Gain Register b3
Sets LNA output impedance.

The LNA output impedance is approximately 100Ω if this bit is set to '0' and approximately 50Ω if this bit is set to '1'. If set to 50Ω the gain will be increased, but with an additional current consumption in the LNA of about 2mA.

6.6.2 Rx Gain Register: C-BUS address $E6
8-bit read-only

This read-only register mirrors the value in register $16, see section 6.6.1 for details of bit functions.

6.7 PLL M Divider Register

6.7.1 PLL M Divider Register: C-BUS Address $22-$20
8-bit write-only

These registers set the M divider value for the PLL (Feedback Divider). The PLL dividers are not updated until all registers ($22, $21 and $20) have been written. The order of writing these registers is not important. Bits 7 and 5 also control the PLL and charge-pump blocks and these control bits are active as soon as $22 is written. (Note: To enable the PLL, b2 of the General Control Register ($11) must also be used, see section 6.2. See also section 5.3.2).

	$22								**$21**							
Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	E	LD_PLL	CP	0	0	0	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8

$20							
7	6	5	4	3	2	1	0
M7	M6	M5	M4	M3	M2	M1	M0

M17:M0
Phase Locked Loop M divider value.

CP
$22, b5 = '1' enables the charge pump, $22 b5 = '0' puts the charge pump into high impedance mode.

LD_PLL
Only write '0' to b6 of $22 (when read via $D2, this shows the integer N PLL lock status).

E
$22, b7 = '1' enables the PLL; b7 = '0' disables the PLL –This bit enables the PLL and is ANDed with General Control Register ($11) b2 – section 6.2. See also section 5.3.2.

6.7.2 PLL M Divider Register: C-BUS Address $D2-$D0
8-bit read-only

These registers read the respective values in registers $20, $21 and $22 ($D0 reads back $20 and $D1 reads back $21 etc.); see section 6.7.1 for details of bit functions.

Note: $D2 b6 indicates the Synth lock detect status.

6.8 PLL R Divider Register

6.8.1 PLL R Divider Register: C-BUS Address $24-$23
8-bit write-only

These registers set the R divider value for the PLL (Reference Divider). The PLL dividers are not updated until both registers ($24 and $23) have been written. The order of writing these registers is not important.

	$24								$23							
Bit:	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
	0	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0

R14:R0
Phase Locked Loop R divider value.

$24, b7
Reserved, set to '0'.

6.8.2 PLL R Divider Register: C-BUS Address $D4-$D3
8-bit read-only

These registers read the respective values in registers $23 and $24 ($D3 reads back $23 and $D4 reads back $24); see section 6.8.1 for details of bit functions.

6.9 VCO Control Register

6.9.1 VCO Control Register: C-BUS address $25
8-bit write-only

This register controls the operation of the VCO and LO input. Operation is only enabled when b3 = '1' in the General Control Register ($11), as detailed in section 6.2.
All bits of this register are cleared to '0' by a General Reset command.

Note: It is not recommended that the LO input and the VCO are enabled simultaneously.

Bit:	7	6	5	4	3	2	1	0
	FILT_ CAL	TXDIV1	TXDIV0	LO Input EN	VCO_N R2	VCO_ NR1	VCO_ NR En	VCO_ Buf En

VCO Control Register b7
This bit, if set to '1', will disable the Filter Calibration System.
The default value is '0'.

VCO Control Register b6 – b5
These bits control the output division of the Tx LO signal available at pin TXLO. The LO signal is divided by the factor as shown in the following table.

Bit: b6	b5	
0	0	Divide by 2
0	1	Divide by 4
1	0	Divide by 6
1	1	No division

VCO Control Register b4, b1 and b0

These bits control power up/power down of the various blocks of the IC.
In all cases '1' = power up, '0' = power down.

B4	Enable LO input
b1	Enable VCO NR Amplifier. When disabled the amplifier is bypassed to support the application of an external LO signal.
B0	Enable VCO Buffer

VCO Control Register b3 – b2

VCO amplifier Negative Resistance (NR) control bits optimise phase noise performance. These bits control the Negative Resistance (magnitude of the negative transconductance) of the on-chip VCO NR amplifier. The NR minimum mode would thus be used with the lowest Q external tank circuit and NR maximum with the highest Q value.

Bit:	b3	b2	
	0	0	NR maximum
	0	1	NR intermediate value
	1	0	NR intermediate value
	1	1	NR minimum

6.9.2 VCO Control Register: C-BUS address $D5 8-bit read-only

This register reads the value in register $25, see section 6.9.1 for details of bit functions.

7 Application Notes

7.1 General

The CMX994 integrated circuit is designed for digital wireless applications.

7.2 Receiver Compensation

Please contact CML technical support for more information:
(email: techsupport@cmlmicro.com).

7.3 Typical Receiver Performance

7.3.1 System Performance

This information is intended as a general guide of what can be expected from a CMX994 receiver design using the on-chip LNA and I/Q down-conversion stages. The measurement circuit uses the component values given in section 4.2. The results are based on measurements from evaluation of the CMX994 operating at 450MHz. Results are also given for Low Power (LP) mode operation, i.e. General Control Register ($11) b4 = '1', see section 6.2.1.

- Gain 63dB (62.5dB in LP mode)
- Noise Figure: 4.5dB (also 4.5 dB in LP mode)
- Input Third Order Intercept Point: -3dBm (-9 dBm in LP mode)
- Input Second Order Intercept Point: 62dBm (60dBm in LP mode)

Notes:
- Common settings: max gain, max filter bandwidth, freq control bits = 300 to 700MHz, LNA output impedance = 100Ω, LO at x2 (900MHz, level -10dBm), IM Control Register = 0x3F
- Gain is measured from RF input (assumed to be 50 Ohm source /load) to differential voltage measured at output of I or Q channels.
- Second Order Intercept Point is the average of values measured from differential signals on I and Q; measured at 1MHz offset.

Using the CMX994 operating at 448MHz combined with the CMX7164FI-2 modem IC gives the following typical system performance using 19.2kbps 4-FSK modulation, alpha =0.2, deviation =3kHz (based on a 25kHz RF channel).

- Sensitivity for 1% BER -116dBm (see Figure 17)
- Blocking >90dB
- Adjacent channel rejection 73dB
- Intermodulation 65dB

(Measurement methods based on EN 300 113-1).

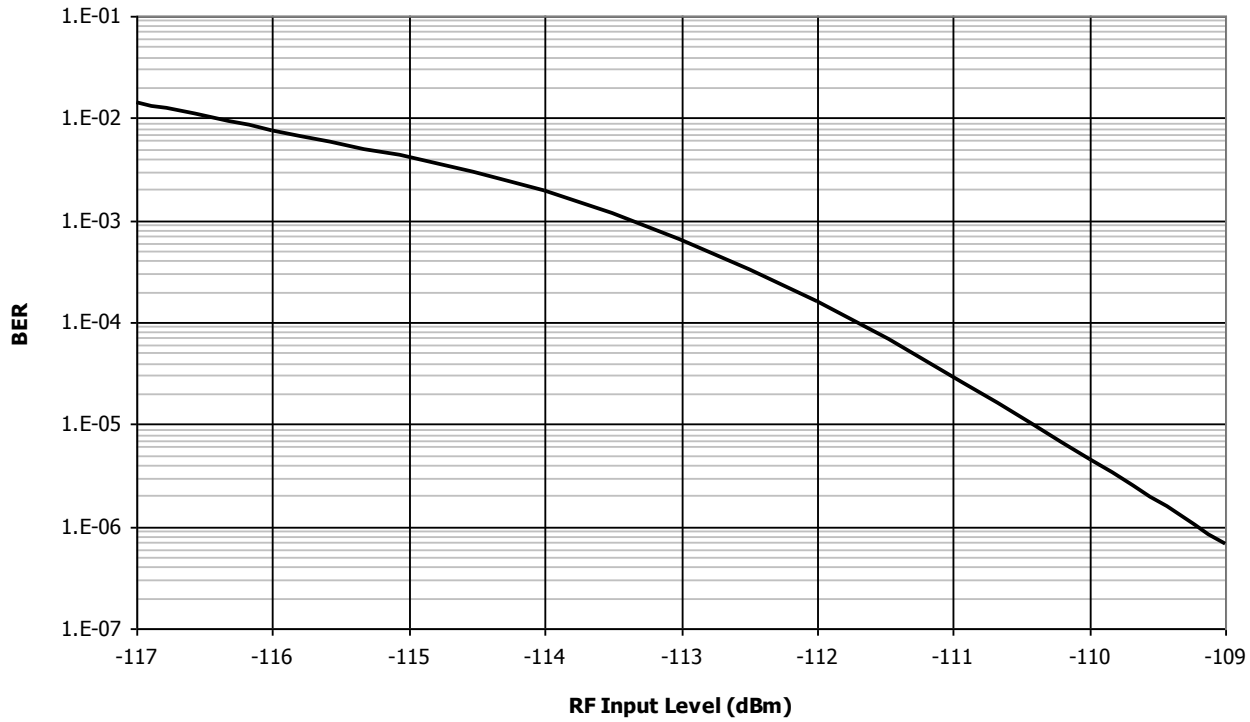


Figure 17 CMX994 and CMX7164FI-2 Typical 4-FSK Sensitivity (19.2kbps)

7.3.2 DC Offsets

To provide approximate correction of offsets for a particular attenuation setting, measure the offset at the CMX994 output, (V_{offset}). If the attenuation is set at minimum, the table gives the required offset correction. For other attenuation settings, set the offset register so as to correct for this offset ($V_{correction}$). The value will be given by:

$V_{correction}$ = - V_{offset} x Atten

Where Atten = 10^{(VGA value)/20}

This is more simply 2^-G, where G is the binary value of the Rx Gain Setting bits. So the correction value is easily calculated with binary shifts.

This will correct for offsets to leave a residual offset that will typically be less than 25mV.

Example 1:

Measured offset in the Q channel is –78mV and the VGA is set at –6dB

$V_{correction}$ = -V_{offset} x Atten

$V_{correction}$ = 78 x 2^{-1} = 39mV

The nearest correction value is +50mV so set $13 (b7, b6, b5, b4) = 0, 0, 1, 0

Example 2:

Measured offset in the I channel is +42mV and the VGA is set at –6dB

$V_{correction} = -V_{offset} \times Atten$

$V_{correction} = -42 \times 2^{-1} = -21mV$

The nearest correction value is -25mV so set $13 (b3, b2, b1, b0) = 1, 0, 0, 1

Correction factors calculated at each gain setting will remove offsets to <+/-25mV.

It may be preferred to just measure the offset at one of the lower attenuation settings and then to use the calculated correction factor for all attenuation settings. In this case, at high attenuation settings there may be an additional error due to residual offsets from within the VGA; this is expected to be <+/-40mV.

7.3.3 Gain Control

The CMX994 has gain control mechanisms in the LNA and the baseband (see Figure 18) with a total control range of 60dB. The gain can be controlled using the Rx Gain Control Register, $16, see section 6.6.1.

The LNA gain control steps can be adjusted to achieve the required accuracy using the step size control bits in the Rx Gain Control Register. The effect of the step size control varies with frequency, as shown in Table 16, Table 17 and Table 18, so for optimum accuracy it is necessary to access the control and select the best settings for a particular application.

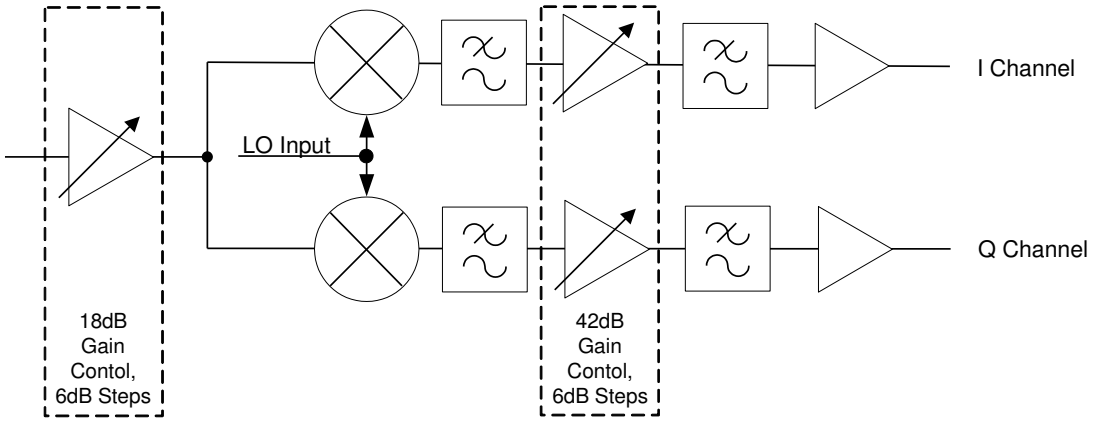


Figure 18 CMX994 Gain Control

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.9	-6.9	-0.9
-12 dB	-5.4	-12.3	-0.3
-18 dB	-4.2	-16.5	1.5
Nominal +0.7 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-6.7	-13.7	-1.7
-18 dB	-4.1	-17.8	0.2
Nominal +1.4 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-7.9	-14.9	-2.9
-18 dB	-4.1	-18.9	-0.9
Nominal +2.8 dB			
Max		0.0	
-6 dB	-7.0	-7.0	-1.0
-12 dB	-9.2	-16.2	-4.2
-18 dB	-4.0	-20.2	-2.2

Table 16 Typical LNA Gain Step Sizes at 100MHz, Z_O=100Ω

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.2	-6.2	-0.2
-12 dB	-4.5	-10.7	1.3
-18 dB	-3.7	-14.5	3.6
Nominal +0.7 dB			
Max		0.0	
-6 dB	-6.2	-6.2	-0.2
-12 dB	-5.5	-11.8	0.3
-18 dB	-3.9	-15.6	2.4
Nominal +1.4 dB			
Max		0.0	
-6 dB	-6.3	-6.3	-0.3
-12 dB	-6.6	-12.9	-0.9
-18 dB	-4.0	-16.9	1.1
Nominal +2.8 dB			
Max		0.0	
-6 dB	-6.3	-6.3	-0.3
-12 dB	-7.6	-13.9	-1.9
-18 dB	-4.4	-18.3	-0.3

Table 17 Typical LNA Gain Step Sizes at 450MHz, Z_O=100Ω

Gain Setting	Gain Cntrl Step Size (dB)	Cumulative Gain Change (dB)	Variation from Nominal (dB)
Nominal step size			
Max		0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-5.6	-12.0	0.0
-18 dB	-5.2	-17.2	0.8
Nominal +0.7 dB			
Max	0.0	0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-7.1	-13.5	-1.5
-18 dB	-5.6	-19.1	-1.1
Nominal +1.4 dB			
Max		0.0	
-6 dB	-6.4	-6.4	-0.4
-12 dB	-8.6	-15.1	-3.1
-18 dB	-5.7	-20.7	-2.7
Nominal +2.8 dB			
Max		0.0	
-6 dB	-6.5	-6.5	-0.5
-12 dB	-10.3	-16.8	-4.8
-18 dB	-5.5	-22.3	-4.3

Table 18 Typical LNA Gain Step Sizes at 940MHz, Z_O=50Ω

7.3.4 LNA Intermodulation Optimisation

The intermodulation (IMD) performance of the LNA can be optimised using the IM bits in the IM Control register ($14), see section 6.5.1.

At higher frequencies, typically 400MHz and above, optimum IMD performance is with the IM bits set to maximum, i.e. 0x3F. The improved IMD performance comes with a reduction in gain of approximately 0.5dB, see Figure 19.

At minimum frequency (circa 100MHz) the IM bits should be set to minimum i.e. 0x00.

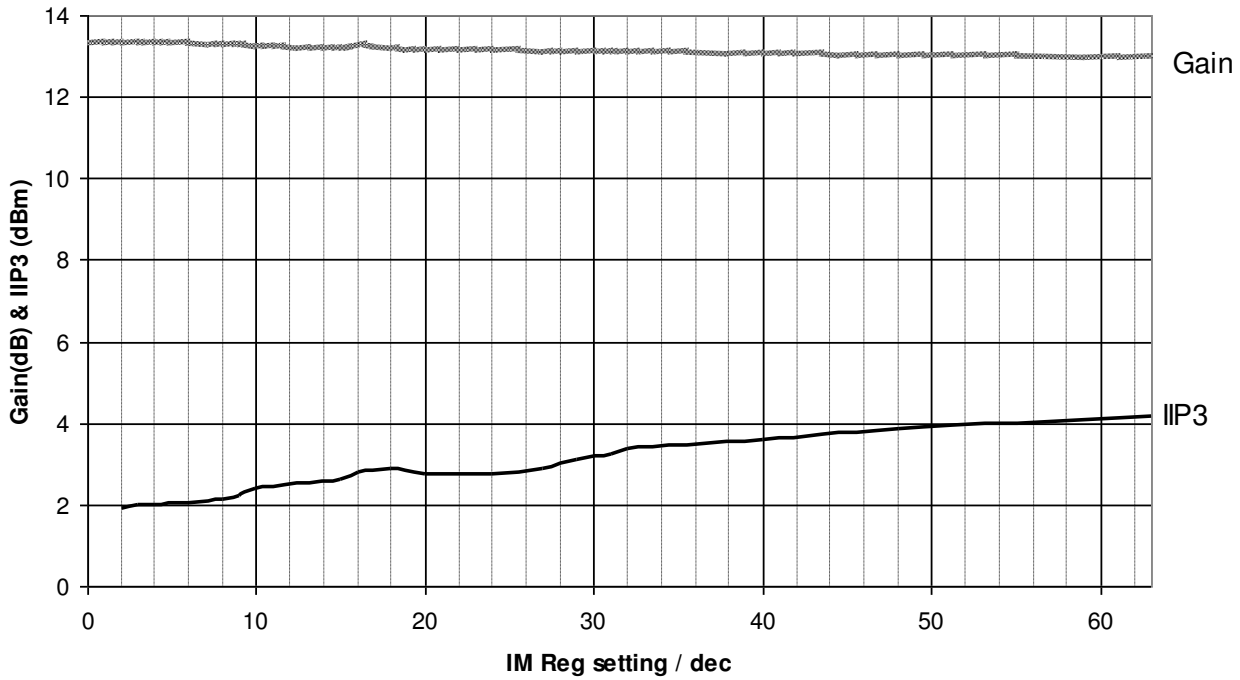


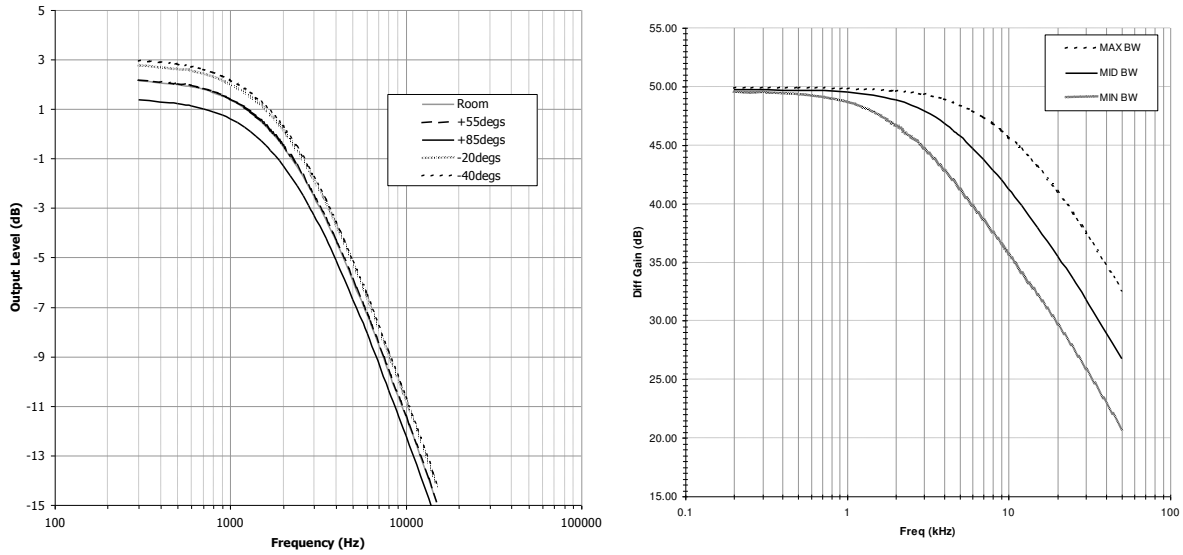
Figure 19 Variation of LNA Gain and IMD with IM register setting, 450 MHz

7.3.5 Low Power Mode

If the low-power mode is enabled, General Control Register ($11), b4 = 1, the total current drawn in the receiver section reduces by approximately 10 mA. For indications of the performance changes in low-power mode, see section 7.3.1.

7.3.6 I/Q Filter Response

The I/Q filter has a well-defined response and an internal calibration scheme makes it very stable with temperature. The response with temperature, measured through the entire receiver, is shown in Figure 20(a). It will be observed that, apart from a small change in overall gain, the filter response does not vary. The scaling with ACR Flt bits (Rx Control Register ($12), b4-b3) is shown in Figure 20(b).



(a) **(b)**

Figure 20 I/Q Filter Response

7.4 Operation below 100MHz

The CMX994 can be safely used below 100MHz, down to at least 30MHz, however performance will degrade at lower frequencies and will fall particularly rapidly below 50MHz.

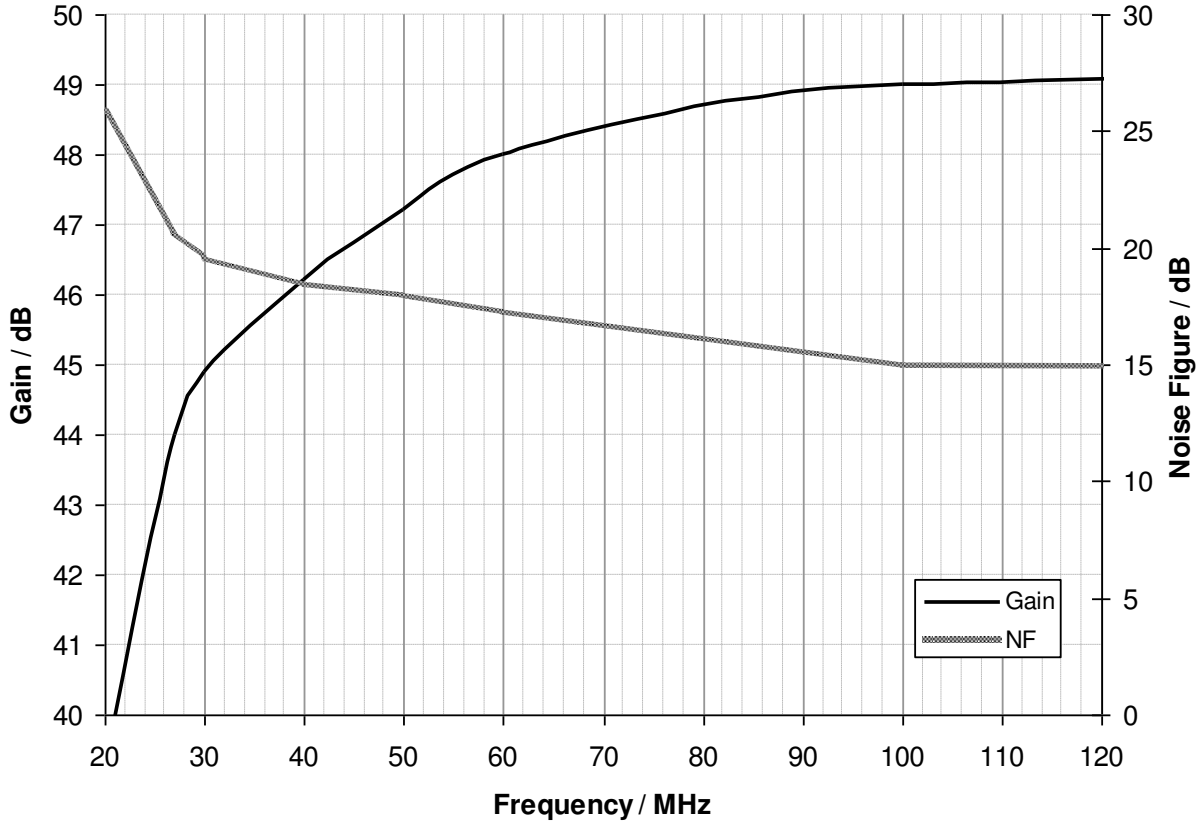


Figure 21 Typical Gain and NF variation of demodulator stages at low frequencies

The LNA can be matched for 30MHz giving a gain of 15.5dB and noise figure of 5dB. Intermodulation is typically +3.5dBm.

For a 50MHz application, typical circuit values are shown in Table 19 using the circuit of Figure 7. Typical results using this configuration are shown in Table 20.

C1	1nF	L1	560 nH
C2	33 pF // 10nF	L2	12 pF (capacitor)
C3	1nF	L3	Not Fitted

Table 19 50MHz LNA and Inter-stage Components (100Ω output mode)

Parameter	Result
Gain	63.5dB
Noise Figure	5dB
IIP3	-0.5dBm

Table 20 Summary of Results for the Complete Rx Chain at 50MHz

7.5 Transmitter LO Output

The transmitter LO output is taken from the CMX994 LO source and is independently buffered or divided to the TXLO pin. The division ratio is selected with the TXDIV0 and TXDIV1 bits in the VCO Control register ($25, b5-b6, see section 6.9.1). The output level variation with frequency of the TXLO output is shown in Figure 22.

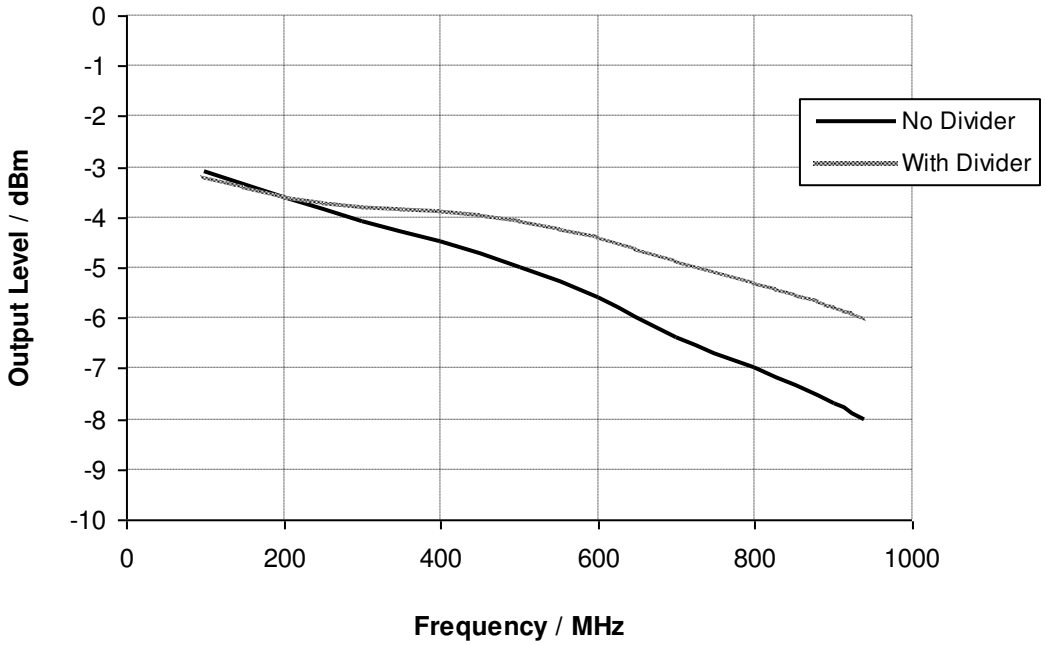


Figure 22 Tx Output Level vs. Frequency

8 Performance Specification

8.1 Electrical Performance

For a definition of voltage and reference signals, see section 3.2.

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

ESD Warning: This high performance RF integrated circuit is an ESD sensitive device which has unprotected inputs and outputs. Handling and assembly of this device should only be carried out at an ESD protected workstation.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin to AGND or DGND pins	-0.3	V_{DD} + 0.3	V
Voltage between AGND and DGND pins	-50	+50	mV
Current into or out of DGND, VDDIO, VCCRXIF, VCCRF, VCCLNA, VCCSYNTH, VCCLO or DVDD pins	-75	+75	mA
Current into or out of AGND (exposed metal pad)	-200	+200	mA
Current into or out of any other pin	-20	+20	mA

Q4 Package	Min.	Max.	Units
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1820	mW
... De-rating	–	18.2	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Analogue Supply (AV_{DD}) and Digital Supply (DV_{DD})		3.0	3.6	V
IO Supply (VDD_{IO})		1.6	3.6	V
Operating Temperature		-40	+85	°C

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = VDD_{IO} = 3.0V to 3.6V; V_{SS} = AV_{SS} = DV_{SS}, T_{AMB} = +25°C; registers in default condition except were otherwise specified or as necessary to enable the relevant sections of the device.

8.1.3.1 DC Parameters

DC Parameters	Notes	Min.	Typ.	Max.	Units
Total Current Consumption					
Powersave Mode	1, 2	–	25	–	µA
V_{BIAS} Only	4	–	1.7	3.5	mA
Operating Currents					
Rx Only	5	–	66	80	mA
Rx Only, Low Power Mode	5a	–	56	–	mA
Tx Only	5	–	22	30	mA
Stage currents					
LNA Only	5	–	9	15	mA
LNA in 50Ω Output mode	5b	–	11	–	mA
I/Q Demodulator	5	–	41	53	mA
Baseband I/Q	5	–	13	15	mA
VCO & Buffer	5	–	10	13	mA
LO Input	5	–	5	7	mA
PLL	5	–	5.5	–	mA
Current from VDD_{IO}	3	–	–	600	µA
Logic “1” Input Level		70%	–	–	VDD_{IO}
Logic ‘0’ Input Level		–	–	30%	VDD_{IO}
Output Logic ‘1’ Level (I_{OH} = 0.6 mA)		80%	–	–	VDD_{IO}
Output Logic ‘0’ Level (I_{OL} = -1.0 mA)		–	–	+0.4	V
Power-up time					
Internal Bias Supplies	6, 7	–	–	0.5	ms
All Blocks Except Internal Bias	6	–	–	10	µs

Notes:
1. Powersave mode current applies to both the following operating cases: (a) after a General Reset command has been issued and with all analogue and digital supplies applied and also (b) with V_{DD} applied but with all analogue supplies disconnected. For case (b), V_{DD} current will not exceed the specified value and is independent of the state of the registers.
2. T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
3. Assumes 30pF on each C-BUS interface line and an operating serial clock frequency of 5MHz.
4. The stated current drawn here is with the bandgap reference and accompanying bias current generators enabled only (General Control Register – $11), all other circuitry is disabled.
5. Not including any current drawn from the device pins by external circuitry or the bias current.
   Rx Only – Rx Circuitry as enabled: Rx Gain Register = 0x00, General Control Register = 0xC2, Rx Control Register = 0x10 and Intermodulation Control Register = 0x3F;
   TX Only – General Control Register = 0x81, divide by 2 mode;
   LNA Only – 0x82 is written to the General Control Register and 0xC0 to the Rx Control register;
   I/Q Demodulator – 0x60 is written to the Rx Control register;
   Baseband I/Q – 0xA0 is written to the Rx Control register;
   VCO and Buffer – 0x88 is written to the General Control Register and 0x03 to the VCO Control Register;
   LO Input – 0x84 is written to the General Control Register and 0x10 to the VCO Control Register;
   PLL – 0x00 is written to the VCO Control Register, 0x82 is written to the General Control Register and 0x80 to PLL M register ($22).

5a. As note 5 except General Control Register ($11) b4 = '1', see section 6.2.1, see also section 7.3.5.

5b. As note 5 except Rx Gain Register ($16) b3 = '1', see section 6.6.1.

6. As measured from the rising edge of CSN.
7. Bias is enabled by General Control Register ($11) b7, see section 6.2.1.

8.1.3.2 AC Parameters – Low Noise Amplifier Section

LNA	Notes	Min.	Typ.	Max.	Units
Gain					
100MHz	14	–	15	–	dB
450MHz	12,14	–	12.5	–	dB
940MHz	17	–	11	–	dB
Reverse Isolation (S_{12})					
100MHz	14	–	-40	–	dB
450MHz	14	–	-27	–	dB
940MHz	17	–	-19	–	dB
Gain Control Range	16	–	18	–	dB
Gain Control Step Size	16	4	6	8	dB
Noise Figure	14				
100MHz	14	–	2	–	dB
450MHz	14	–	2	–	dB
940MHz	17	–	3.5	–	dB
Third Order Intercept Point (input)					
100MHz	14	–	8	–	dBm
450MHz	11,14	–	8	–	dBm
940MHz	11,14,17	–	0.5	–	dBm
1dB Gain Compression Point (input)					
100MHz	14	–	-11	–	dBm
450MHz	14	–	-12	–	dBm
940MHz	17	–	-10	–	dBm
Input Impedance	10	–	–	–	Ω
Output Impedance	10, 13	–	100R // 1.2pF	–	Ω
Operating Frequency Range	15	100	–	940	MHz
LO Leakage at LNA Input		–	<-90	–	dBm

Notes:
10. For further details see section 4.2.1.
11. Intermodulation optimised using Intermodulation Control Register, for further details see section 6.5.
12. The gain is approximately 2dB higher if the LNA Z_0 (Rx Gain Register b3) is set to '1'.
13. The impedance is approximately 50Ω if the LNA Z_0 (Rx Gain Register b3) is set to '1'.
14. Measured at maximum gain with the LNA Zo (Rx Gain Register b3) set to '0'.
15. For extended operation down to 50MHz see section 7.4.
16. See section 7.3.3 for further details
17. LNA Z_0 = 50Ω (Rx Gain Register b3 set to '1')

8.1.3.3 AC Parameters – Direct Conversion Receiver Sections

I/Q Demodulator (combined performance of receiver sections, excluding LNA)	Notes	Min.	Typ.	Max.	Units
Gain					
450MHz		–	49	–	dB(V/V)
940MHz		–	49	–	dB(V/V)
Noise Figure					
450MHz		–	14.5	–	dB
940MHz		–	16	–	dB
Third Order Intercept Point (Input)					
450MHz		–	11	–	dBm
940MHz		–	9.5	–	dBm
Second Order Intercept Point (Input)					
100MHz to 600 MHz	25	–	79	–	dBm
600MHz to 940 MHz	25a	–	73	–	dBm
Image Rejection (I/Q Gain/Phase matching)		30	40	–	dB
I/Q Amplitude Balance		–	± 0.03	± 0.15	dB
I/Q Phase Balance		–	± 0.5	± 2.0	deg.
I/Q DC offset correction steps	22	17	25	33	mV
I/Q Output Bandwidth	23	–	–	1.6	MHz
LO Divider Ratios (selectable)		–	2, 4 or 6	–	
I/Q Differential Output Voltage Swing	20	–	–	4.0	Vp-p
Blocking	21	87	90	–	dB

Notes:

20. This is the maximum swing to guarantee meeting the third order distortion characteristics under the specified conditions and is not the maximum limiting value. For clarity, this means that the device has the capability to produce +/-1V on each of the differential outputs. The outputs are capable of driving a load resistance across the differential outputs of 1kΩ. This voltage output capability provides easy interfacing to other CML devices, like the CMX981, which has a maximum input signal amplitude of 2.4Vp-p.
21. Test method based on EN 300 166; including operation of selectable dividers.
22. Register $12, b2 = '0'
23. This is the maximum bandwidth of the I and Q output signals with no external capacitors fitted and with the filter calibration circuit disabled. The bandwidth of the I/Q output can be adjusted to suit the application by use of the I/Q filters. This bandwidth can be set by using external capacitors (see sections 5.2.2 and 5.2.3). Note that a 25kHz bandwidth on the I/Q filters supports a modulation signal bandwidth of 50kHz.
24. Measured at 450MHz.
25. Average value of IIP2 measurements at ±1MHz, ±5MHz and ±10MHz offsets using differential signals on I and Q channels, measurements every 100MHz over the range 100MHz to 600MHz.

25a Average value of IIP2 measurements at ±1MHz, ±5MHz and ±10MHz offsets using differential signals on I and Q channels, measurements at 600MHz and every 50MHz over the range 700MHz to 950MHz.

Rx Direct Conversion Mixers	Notes	Min.	Typ.	Max.	Units
Gain					
450MHz	26	–	15	–	dB(V/V)
940MHz		–	15	–	dB(V/V)
Noise Figure					
450MHz	27	–	13.5	–	dB
Third Order Intercept Point (Input)					
450MHz	27, 24	–	11	–	dBm
Input Frequency Range	15	100	–	940	MHz
LO Frequency Range	15	200	–	2000	MHz
Input Impedance	29	–	–	–	Ω
Zero-IF Signal Bandwidth		1	–	–	MHz
LO Leakage at Input	28	–	-80	–	dBm

Notes:
26. Measured from matched input source.
27. This is an indicative specification only as the parameter cannot be independently measured other than as part of the complete Rx Path.
28. Measured at input to mixers with 100 Ohm termination.
29. For further details see section 4.2.2.

Zero IF Amplifiers and Filters	Notes	Min.	Typ.	Max.	Units
Gain	26, 30	–	34	–	dB(V/V)
Noise Figure	27	–	–	10	dB
Third Order Intercept Point (Input)	27	–	-20	–	dBm
Output Impedance		–	20	–	Ω
1dB Compression Point	27	-30	–	–	dBm
VGA Control Range	31	–	42	–	dB
VGA Step Size		4	6	8	dB
I/Q Output Bandwidth		–	–	1.6	MHz
I/Q Differential Output Voltage Swing	20	–	–	4.0	Vp-p
I/Q Output Common Mode		–	$AV_{DD}/2$	–	V
Post Mixer Filter					
Bandwidth (-3dB)	32, 37	–	88	–	kHz
Adjacent Channel Rejection					
Bandwidth (-3dB)	32	–	2	–	kHz
Scaling Factors		–	1 : 2 : 4	–	
Bandwidth Variation	33	–	–	5	%
Third Order Intermodulation	34				
Post Mixer Filter	27, 35	–	90	–	dBc
1st Amplifier	27, 35	85	–	–	dBc
2nd Amplifier	27, 36	85	–	–	dBc

Notes: 30. The first amplifier stage has nominal gain of 15dB, the second stage has nominal gain of 22dB.
31. Eight VGA steps.
32. Assumes the recommended external capacitors are used (see section 4.2.2).
33. Assuming external resistors with 1% tolerance and external capacitors with 5% tolerance.
34. Tested at maximum gain setting of VGA.
35. Assuming two 200mVp-p tones at 25kHz and 50kHz.
36. Assuming two 60mVp-p tones at 25kHz and 50kHz.
37. The post mixer filter bandwidth will vary with VGA setting. This may typically be 40%, with the bandwidth reducing at lower gain settings.

8.1.3.4 AC Parameters – Tx Output

Tx Divider	Notes	Min.	Typ.	Max.	Units
Input Frequency Range		100	–	2000	MHz
Output Frequency Range		100	–	1000	MHz
Divider ratio		–	1, 2, 4 or 6	–	
Output Level	39	–	-5	–	dBm

Notes: 39. See section 7.5.

8.1.3.5 AC Parameters – Integer N PLL and VCO

	Notes	Min.	Typ.	Max.	Unit
Phase Locked Loop					
Reference Input					
Frequency		5	–	30	MHz
Level	40	0.5	–	–	Vp-p
Divide Ratios (R Counter)		2	–	32767	
Synthesiser					
Comparison Frequency ($f_{comparison}$)		–	–	500	kHz
Input Frequency Range		200	–	1100	MHz
Input Level		-10	-4	–	dBm
Divide Ratios (M Counter)		2	–	262143	
Charge Pump Current		–	±2.5	–	mA
1Hz Normalised Phase Noise Floor	43	–	-216	–	dBc/Hz
VCO Negative Resistance Amplifier					
Frequency Range	42	200	–	1100	MHz
Phase Noise at 10kHz Offset	41	–	-96	–	dBc/Hz
Phase Noise at 100kHz Offset	41	–	-116	–	dBc/Hz
VCO Buffer					
Frequency Range		200	–	1100	MHz
LO Input					
Input Level	44	–	-10	–	dBm
Frequency Range		100	–	2000	MHz

Notes:
40. Sinewave or clipped sinewave.
41. With external components forming an 750 MHz VCO and its LO divider value set to 4.
42. Operation will depend on the choice and layout of external resonant components.
43. 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop bandwidth by: Measured Phase Noise (in 1Hz) = -PN1Hz - $20\log_{10}(M)$ - $10\log_{10}(f_{comparison})$
44. Single-ended input as described in section 4.3.1.

8.1.3.6 AC Parameters – C-BUS

C-BUS Timings (See *Figure 23*)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-enable to clock-high time		100	–	–	ns
t_{CSH}	Last clock-high to CSN-high time		100	–	–	ns
t_{LOZ}	Clock-low to reply output enable time		0.0	–	–	ns
t_{HIZ}	CSN-high to reply output 3-state time		–	–	1.0	µs
t_{CSOFF}	CSN-high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	Clock-cycle time		200	–	–	ns
t_{CH}	Serial clock-high time		100	–	–	ns
t_{CL}	Serial clock-low time		100	–	–	ns
t_{CDS}	Command data set-up time		75.0	–	–	ns
t_{CDH}	Command data hold time		25.0	–	–	ns
t_{RDS}	Reply data set-up time		50.0	–	–	ns
t_{RDH}	Reply data hold time		0.0	–	–	ns

Maximum 30pF load on each C-BUS interface line.

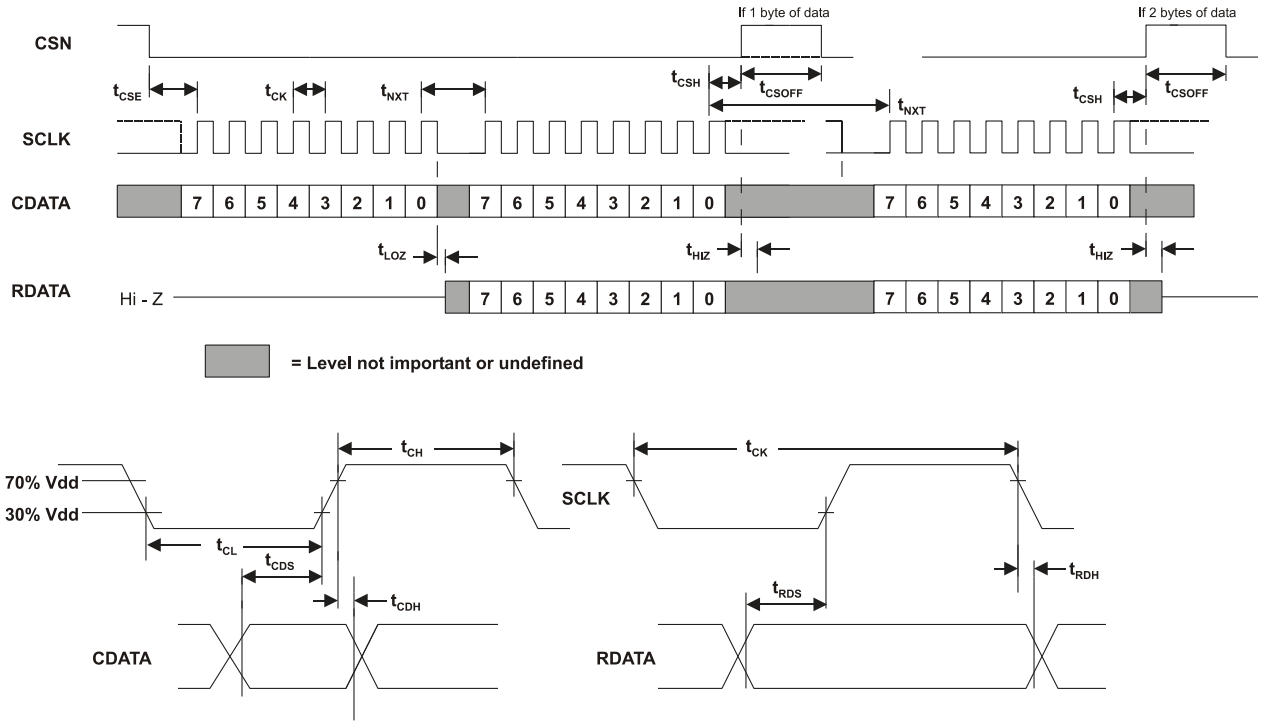
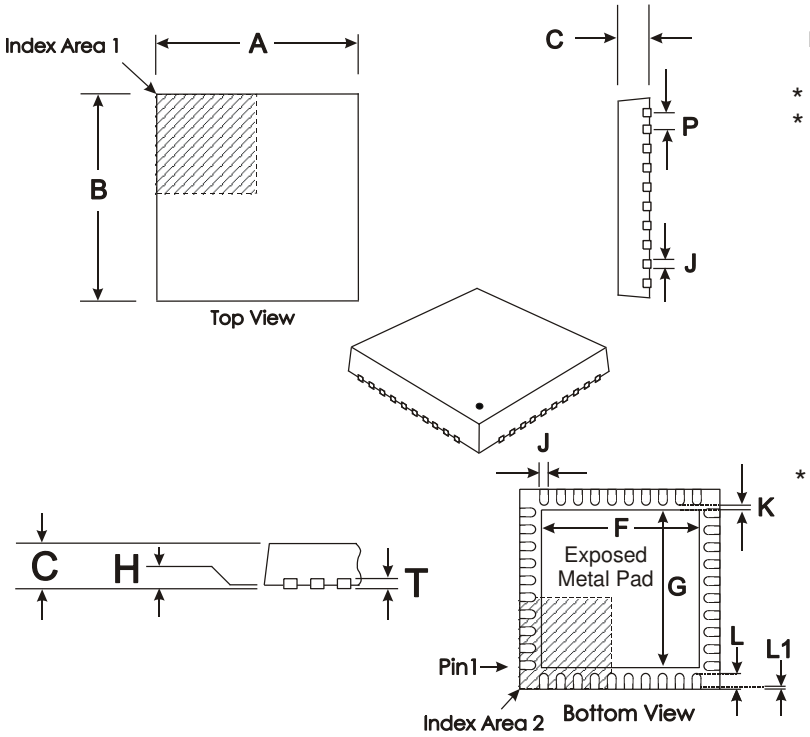


Figure 23 C-BUS Timing

8.2 Packaging



	DIM.	MIN.	TYP.	MAX.
*	A		6.00 BSC	
*	B		6.00 BSC	
	C	0.80	0.90	1.00
	F	4.00		4.30
	G	4.00		4.30
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Notes:

1. In this device, the underside of the Q4 package should be electrically connected to the analogue ground. The circuit board should be designed so that no unwanted short circuits can occur.
2. As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

Figure 24 Q4 Mechanical Outline:

Order as part no. CMX994Q4

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